CBC3 front end design progress

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systems meeting, 4th June, 2015.

CBC3 front end specs, requirements and simulation constraints

simulation (design) constraints

- VDDA = 1V minimum operation
  - VDDA provided by LDO
- operating temperature ~0 deg. C
  - simulate performance @ -20 and +30
- process corners

sensor constraints

- n-in-p (electrons)
  - can scrap dual polarity requirement (helps with $VDDA_{min}$ = 1.0V)
- AC coupled
  - no need to source leakage current (also helps with $VDDA_{min}$ = 1.0V)
- 5 cm length
  - C_{tot} ~ 7.5 pF (C_{is}~2.5pF, C_{bp}~2.5pF)
- 8 cm length
  - provision to increase input FET current to cope with

performance contraints

- pulse shape
  - peaking time <20nsec, pulse return to baseline within 50 nsec
- overload recovery
  - normal response resumed 2.5 usec following 4pC hip signal
- noise
  - target ENC < 1000e

CBC2 issues to address (in CBC3)

- leakage current in pipeline at low ionizing doses
  http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_TID_Davide_Nov_14.pdf
  enclosed NMOS devices now implemented

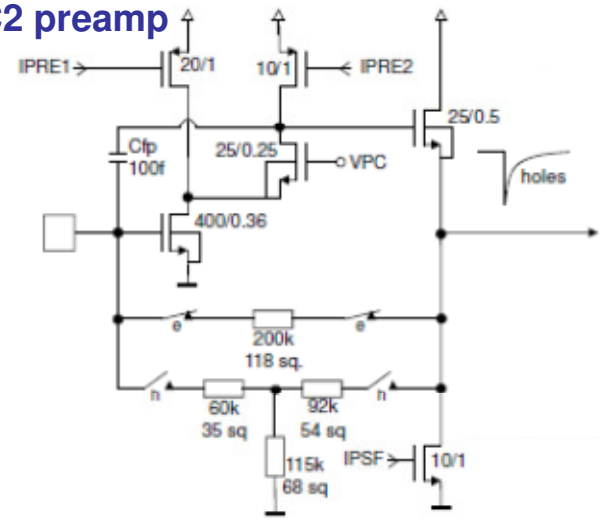
- I2C register SEU immunity could be better
  http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/Phase_2_SEU_Kirika_Nov_14.pdf
  now plan to use Whitaker cells for registers

- CM effect in electrons polarity mode
  shows up when threshold low and many channels firing
  traced to postamp feedback FET biasing
  http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC2_CM_systems_Jan2015.pdf
  a new method for biasing the feedback FET is required

- so-called “shadow effect”
  when signal injected into many channels, other channels fire, but ~50ns later
  traced to coupling through preamp cascode bias
  http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC2_shadow_effect_Apr_2015.pdf
  preamp cascode now individually biased using regulated cascode circuit

CBC3 Preamp modifications

CBC2 preamp



design changes reported last time

increase I/P device bias transistor width (last time)
(allows to run more current if necessary)

scrap T-network for holes polarity

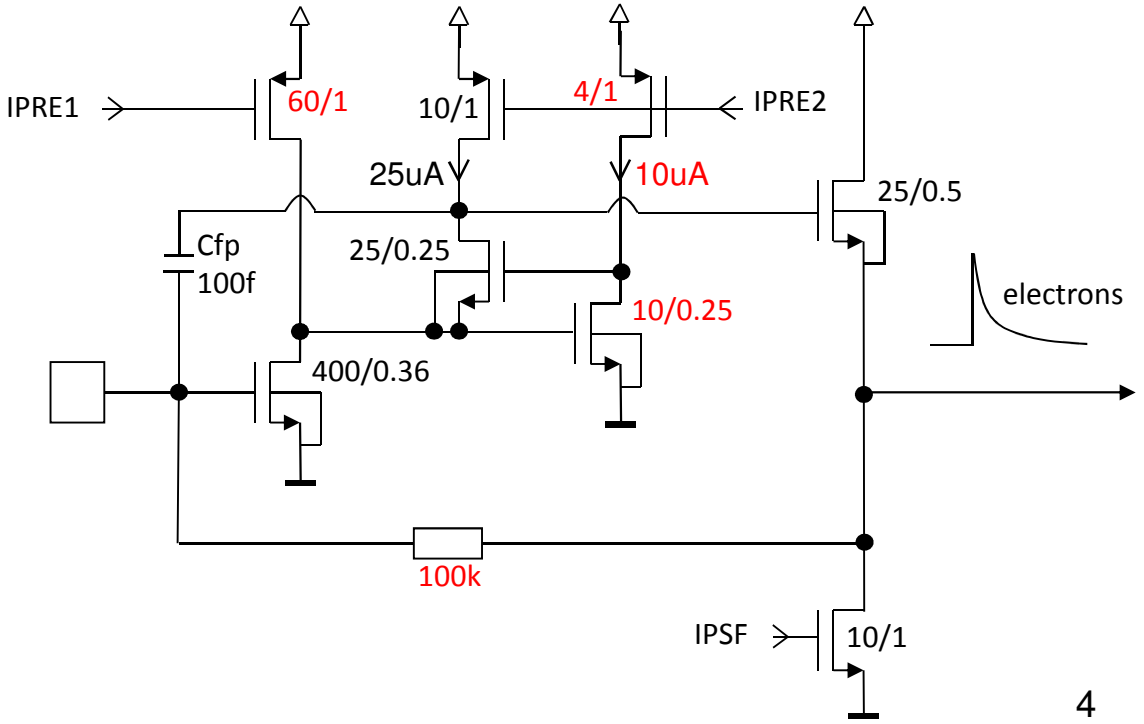
reduce Rf to **100k**
(needed for reduced pulse peaking time)

regulated cascode circuit

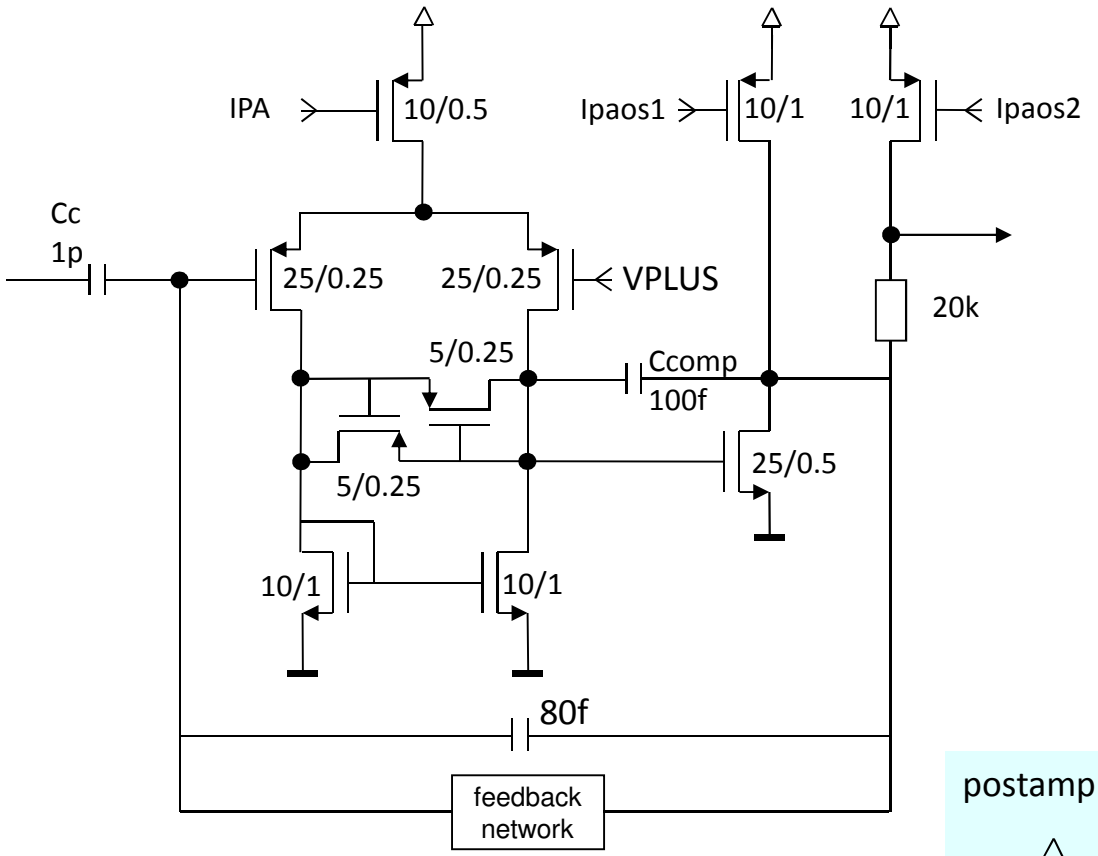
bigger open loop gain

self biasing so no need for common global bias
(fix for “shadow effect”)

small power penalty



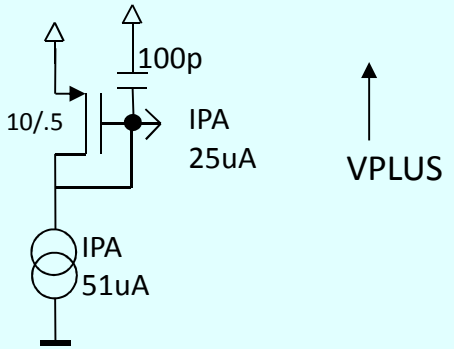
CBC2 Postamp



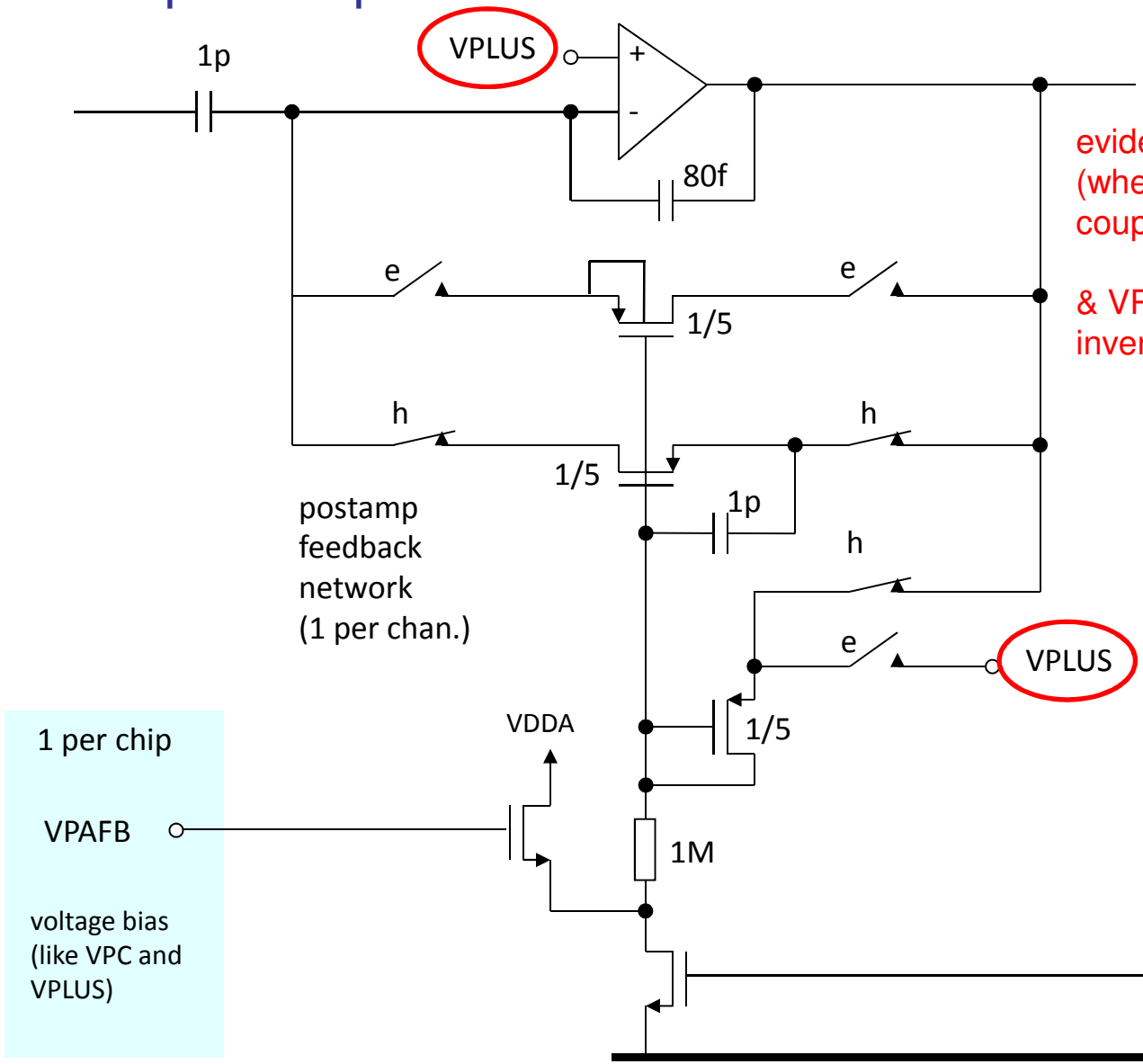
no reason to change the op-amp itself

the feedback network is another matter

postamp bias (1 per chip)



CBC2 postamp feedback

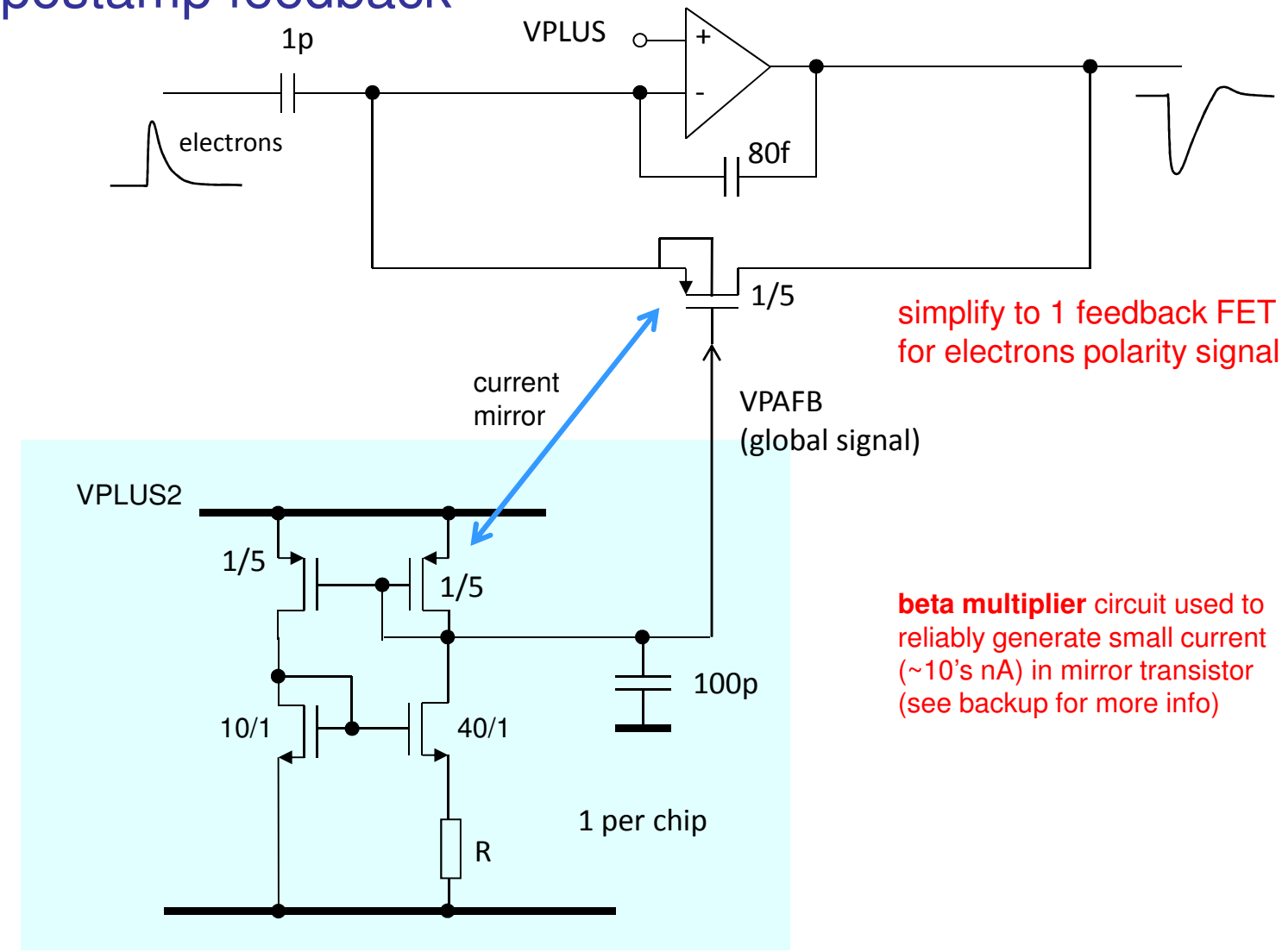


evidence that disturbance on VPAFB (when many comparators fire) couples to VPLUS in electrons mode*

& VPLUS also feeds opamp non-inverting input

* http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC2_CM_systems_Jan2015.pdf

CBC3 postamp feedback

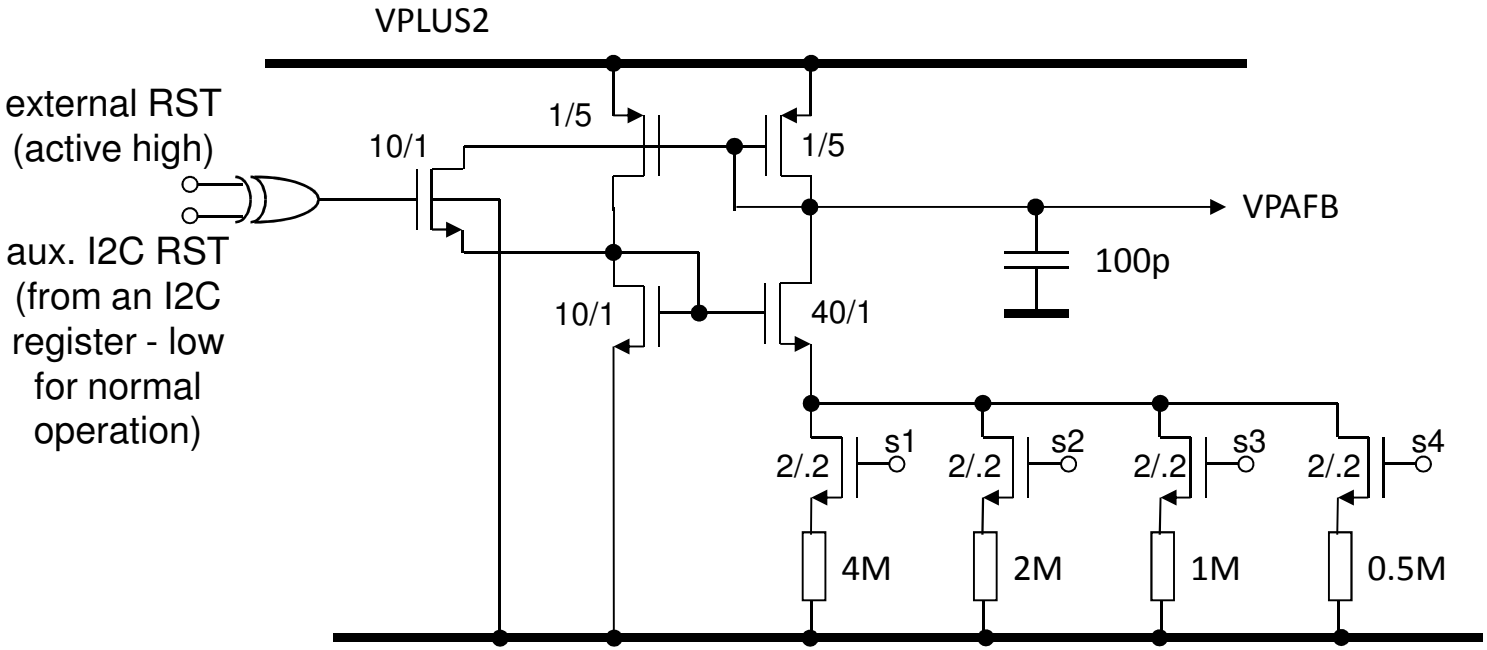


simplify to 1 feedback FET
for electrons polarity signal

beta multiplier circuit used to reliably generate small current (~10's nA) in mirror transistor (see backup for more info)

extra precaution: VPLUS2 = copy of VPLUS, independently generated => no possibility of cross-coupling between bias network and postamp opamp +ve input
would like to use resistor ladder DAC approach for VPLUS and VPLUS2

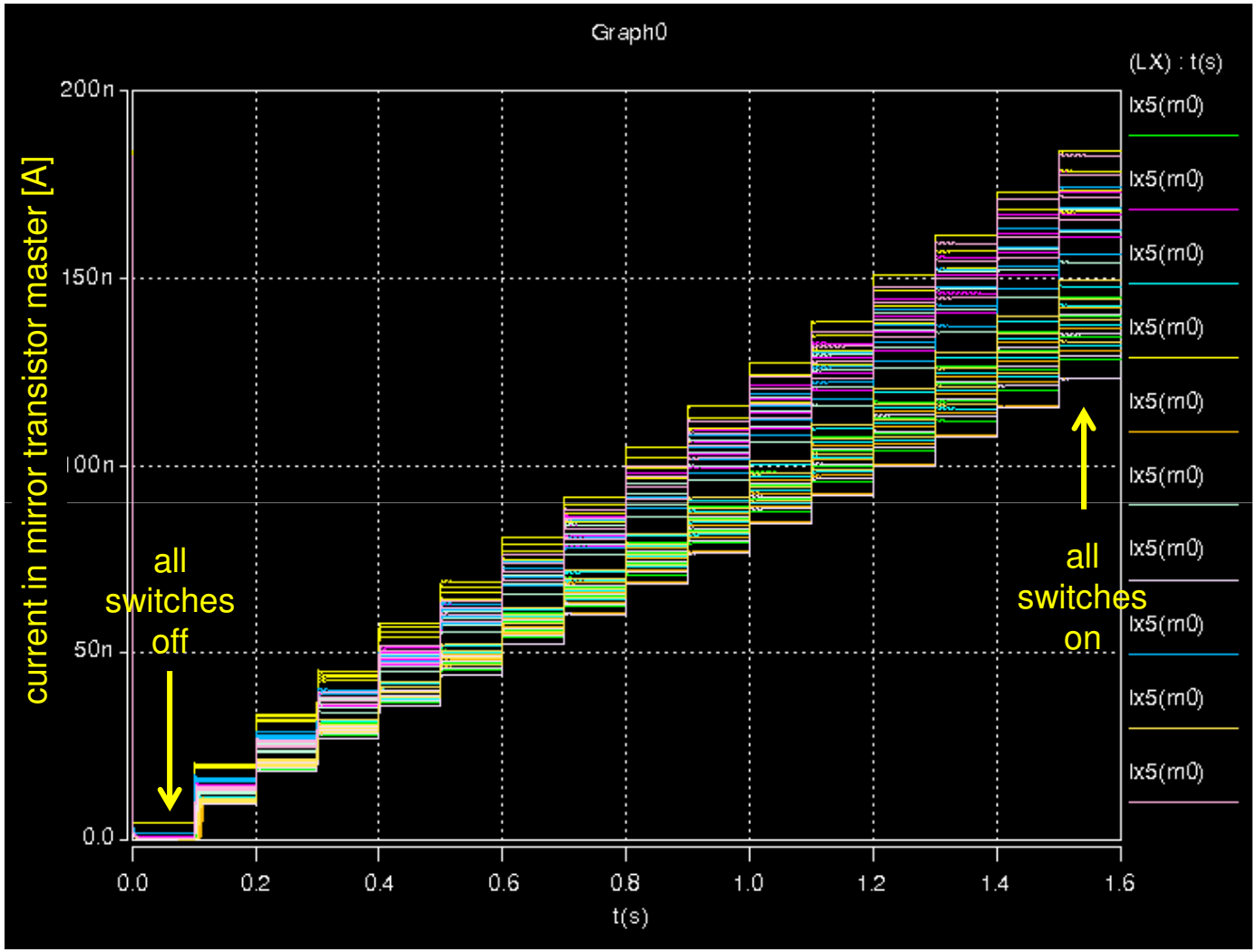
beta multiplier plus start-up and adjustable R



all NMOS enclosed (leakage currents would mess things up)

exclusive OR of RST (startup) lines ensures we can't have a disaster (i.e. get polarity wrong and get stuck in permanent reset!!)

beta multiplier performance vs. adjustable R



cycling through all possible resistor switch combinations

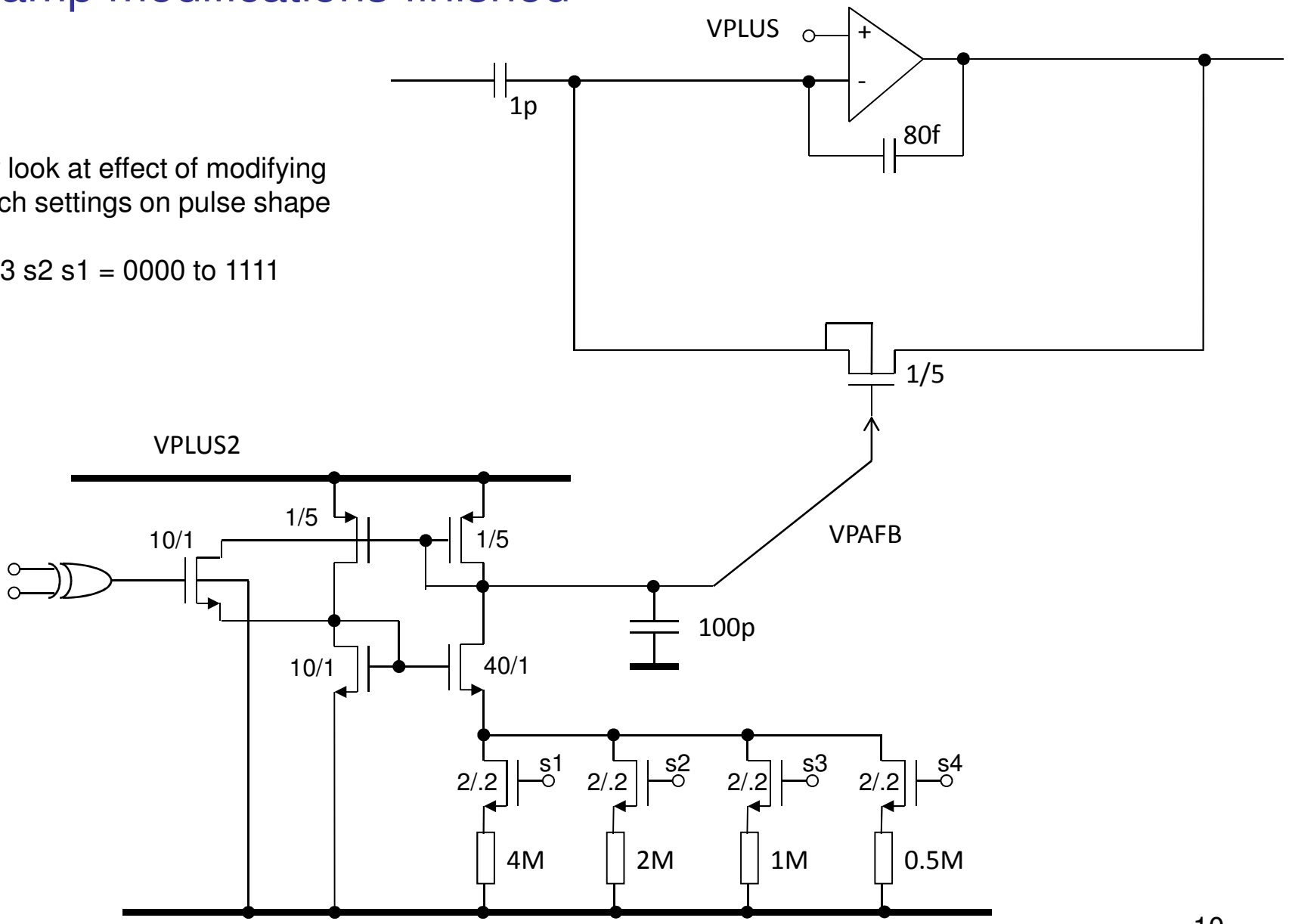
all process corners
T=-20 & +30
VPLUS=0.45, 0.5, 0.55

strongest effect is T
lower family -20
upper family +30

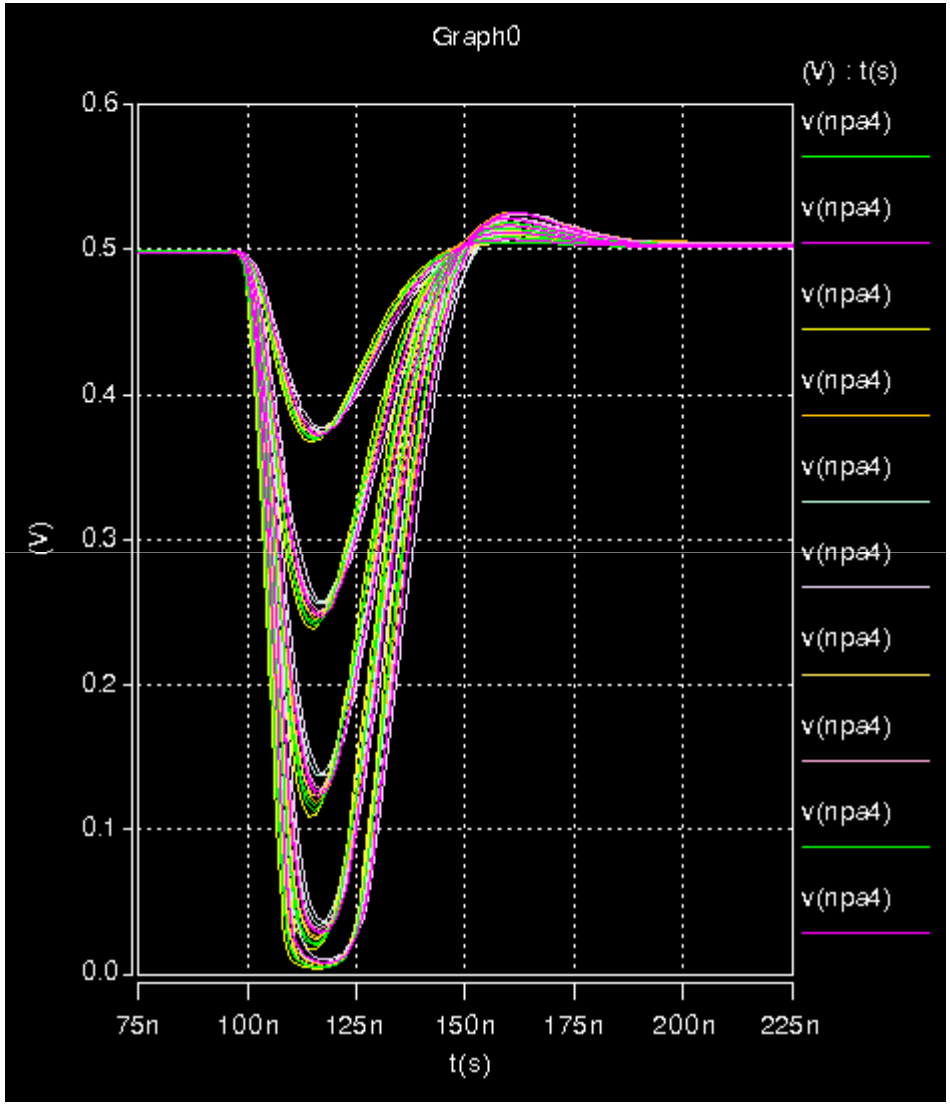
postamp modifications finished

now look at effect of modifying
switch settings on pulse shape

s4 s3 s2 s1 = 0000 to 1111



normal behaviour (1 to 5 mips)



2.5 fC to 12.5 fC, 2.5 fC steps
(one to five mips)

all process corners, T = -20 & +30

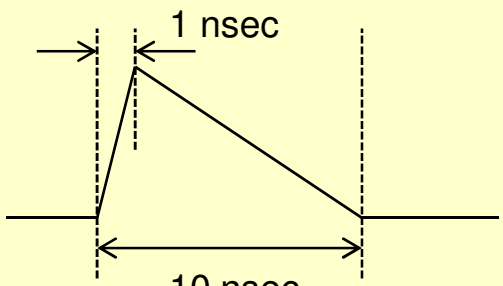
least significant postamp fb current setting - 0001

Cin = 8p, Cstray = 2p, IPRE1 = 30
IPRE2 = 25, IPSF=25, IPA=20

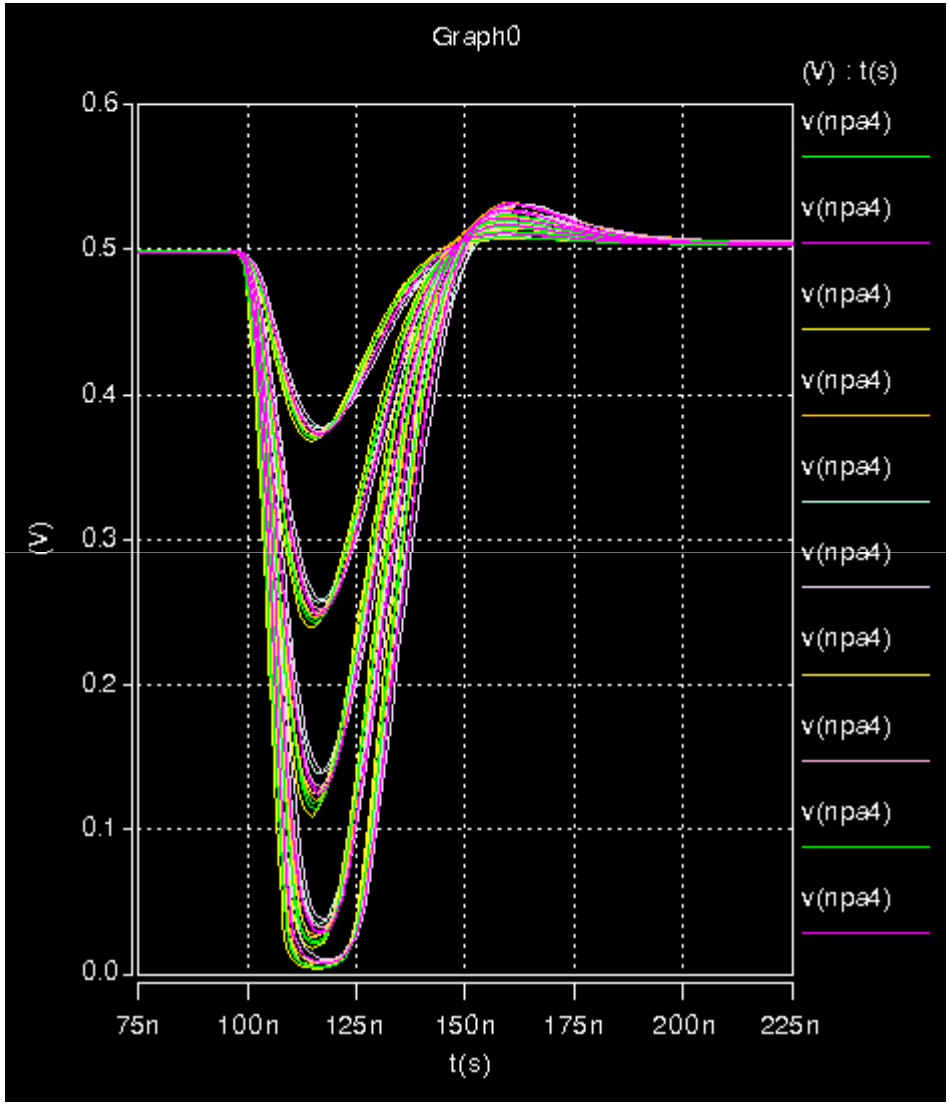
preamp feedback 100k

VDDA = 1V

sensor current pulse model



normal behaviour (1 to 5 mips)



2.5 fC to 12.5 fC, 2.5 fC steps
(one to five mips)

all process corners, T = -20 & +30

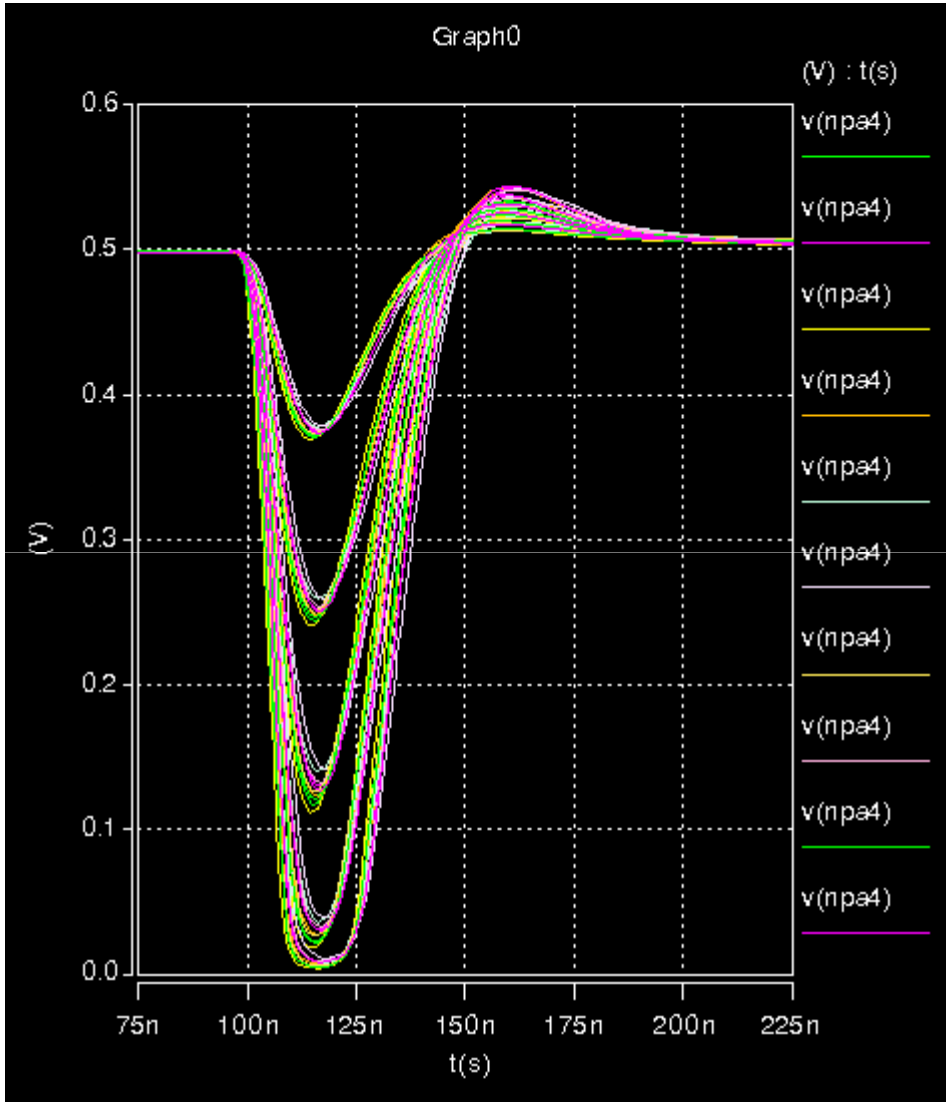
least significant postamp fb current setting - 0010

Cin = 8p, Cstray = 2p, IPRE1 = 30
IPRE2 = 25, IPSF=25, IPA=20

preamp feedback 100k

VDDA = 1V

normal behaviour (1 to 5 mips)



2.5 fC to 12.5 fC, 2.5 fC steps
(one to five mips)

all process corners, T = -20 & +30

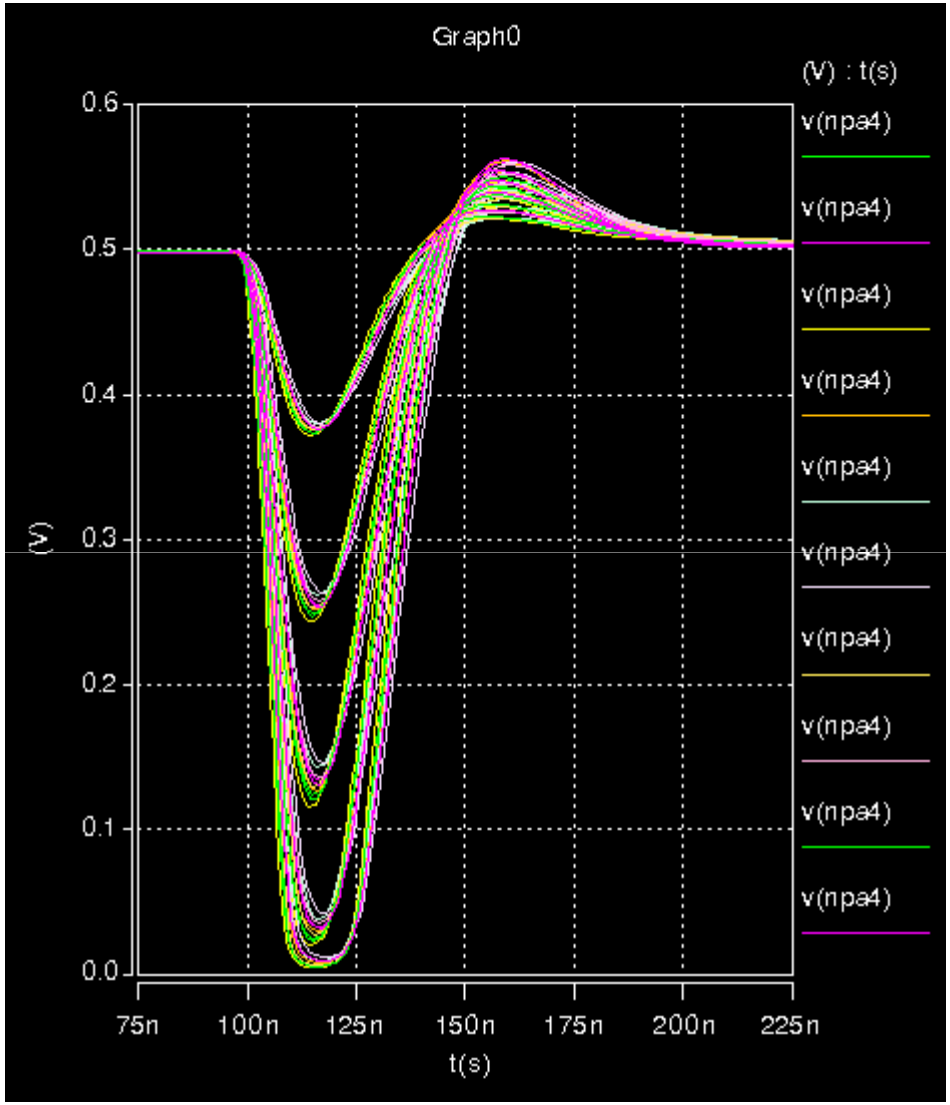
least significant postamp fb current setting - 0100

Cin = 8p, Cstray = 2p, IPRE1 = 30
IPRE2 = 25, IPSF=25, IPA=20

preamp feedback 100k

VDDA = 1V

normal behaviour (1 to 5 mips)



2.5 fC to 12.5 fC, 2.5 fC steps
(one to five mips)

all process corners, T = -20 & +30

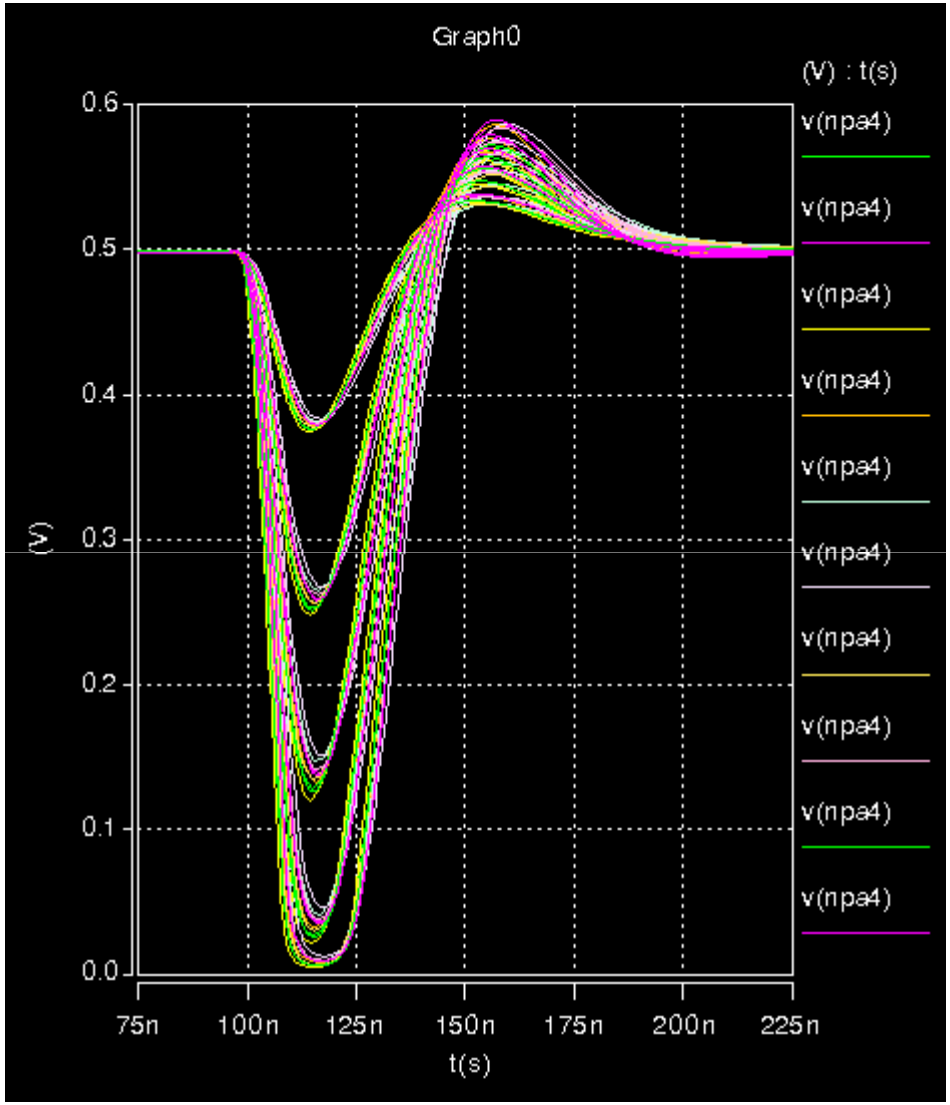
least significant postamp fb current setting - 1000

Cin = 8p, Cstray = 2p, IPRE1 = 30
IPRE2 = 25, IPSF=25, IPA=20

preamp feedback 100k

VDDA = 1V

normal behaviour (1 to 5 mips)



2.5 fC to 12.5 fC, 2.5 fC steps
(one to five mips)

all process corners, T = -20 & +30

least significant postamp fb current setting - 1111

Cin = 8p, Cstray = 2p, IPRE1 = 30
IPRE2 = 25, IPSF=25, IPA=20

preamp feedback 100k

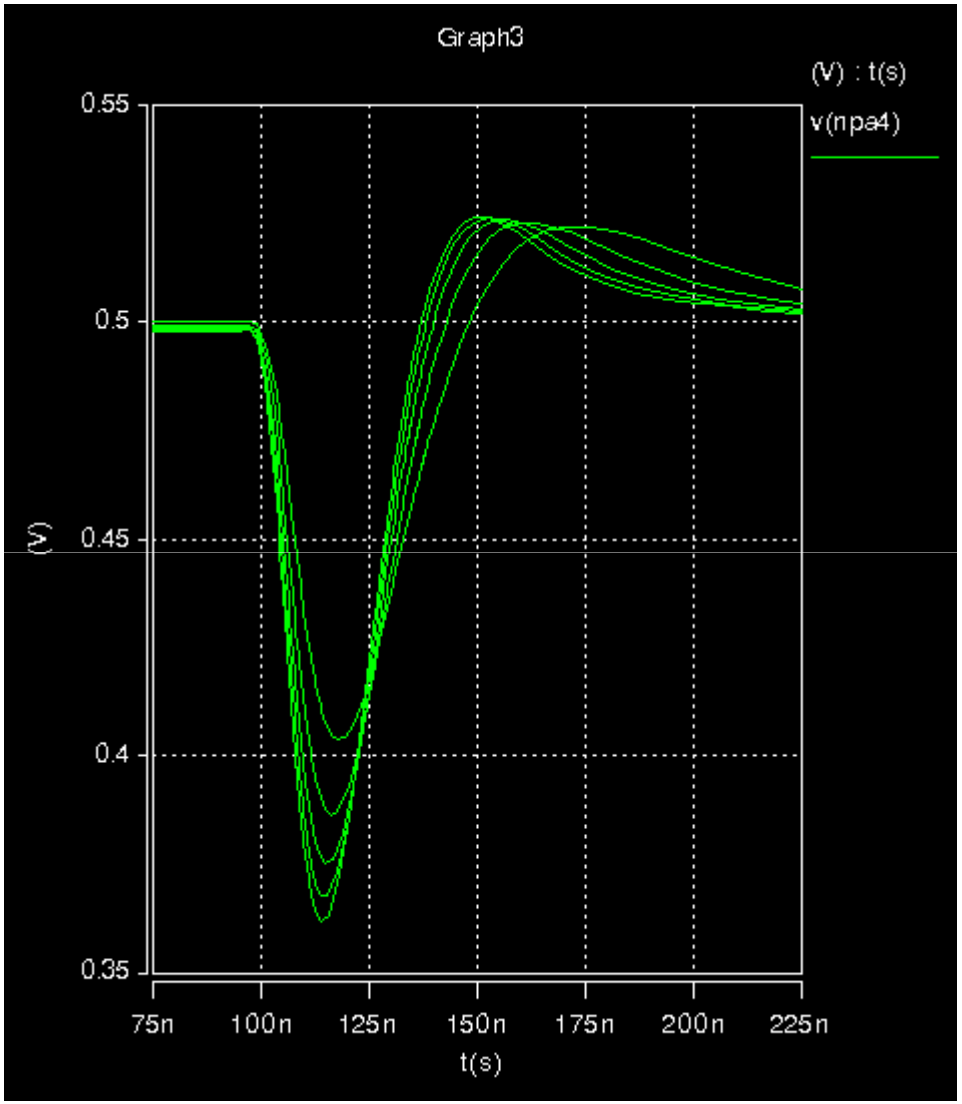
VDDA = 1V

conclusion

pulse shape robust to process and T

some tunability of postamp pulse shape achievable using feedback FET bias

effect of IPA



2.5 fC signal (1 mip)

typical process params, T = 0 deg.

postamp fb current setting - 1000

Cin = 8p, Cstray = 2p, IPRE1 = 30
IPRE2 = 25, IPSF=25, IPA=20

IPA 10u -> 30u , 5u steps

VPLUS = VDDA/2

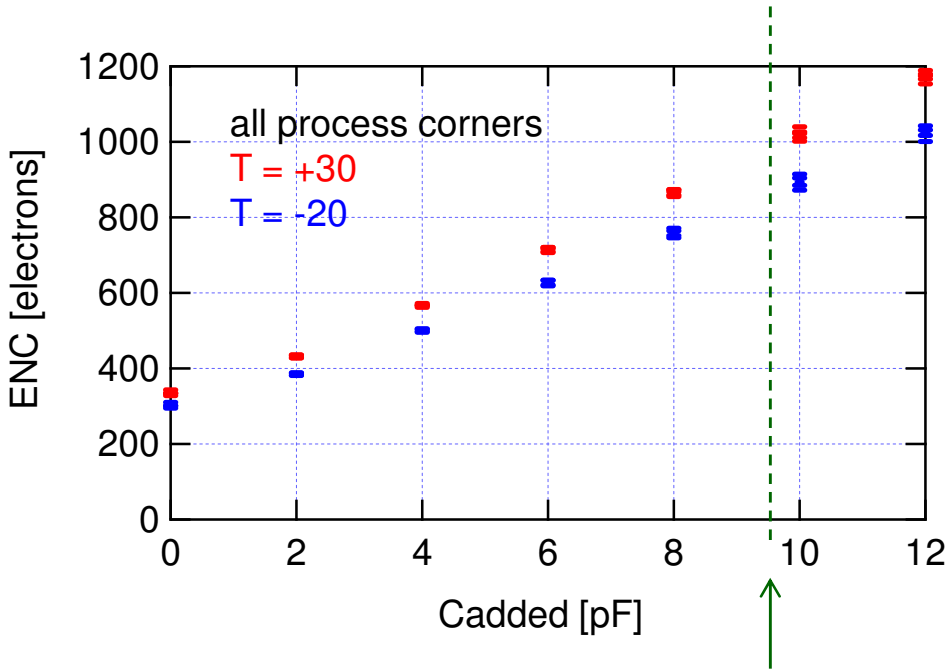
conclusion

varying IPA gives extra handle on pulse shape tunability

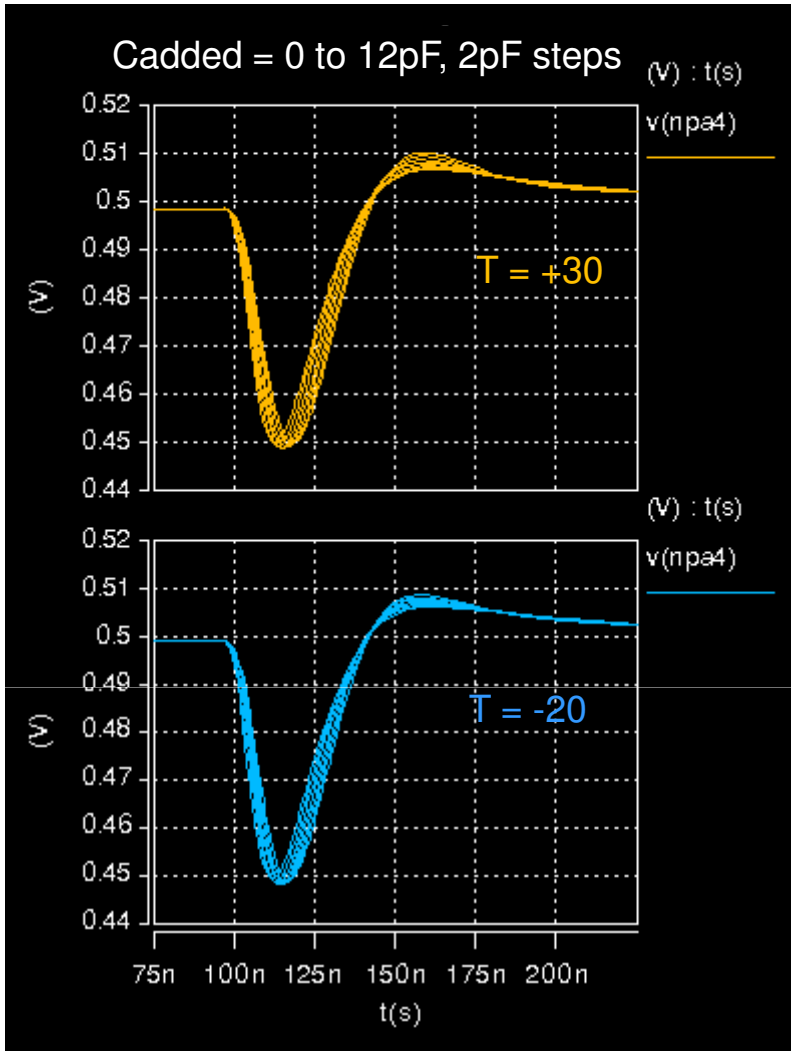
noise performance vs C

dependence on Cadded for fixed 200uA current in I/P FET

total front end power ~350uW (preamp+postamp+comp)



(5cm x 1.5pF/cm) + Cstray~2pF



=> ~1000e achievable for target power consumption

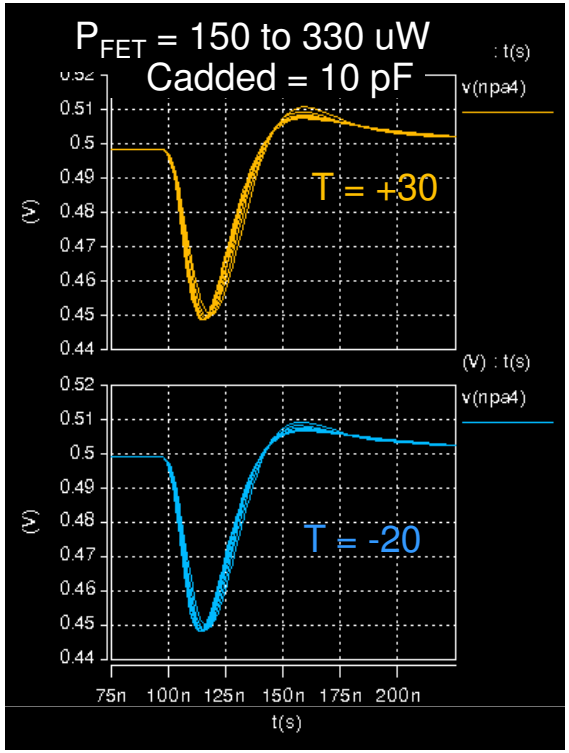
noise vs power

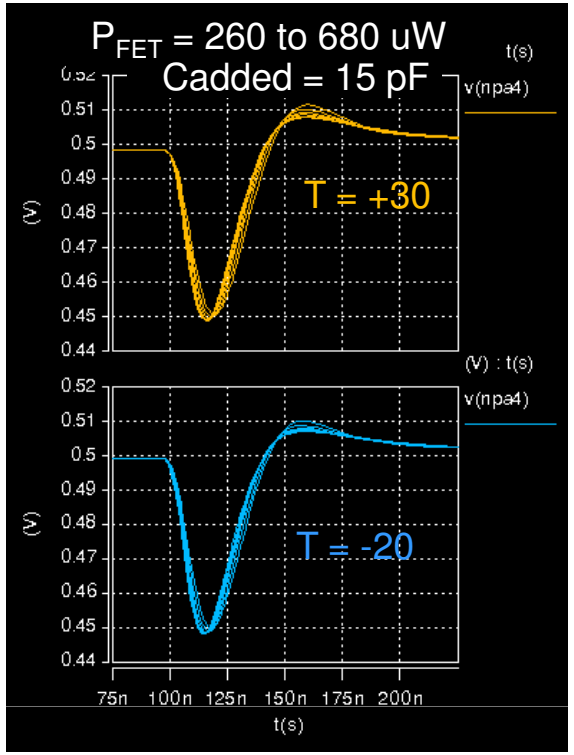
dependence on power for fixed values of Cadded

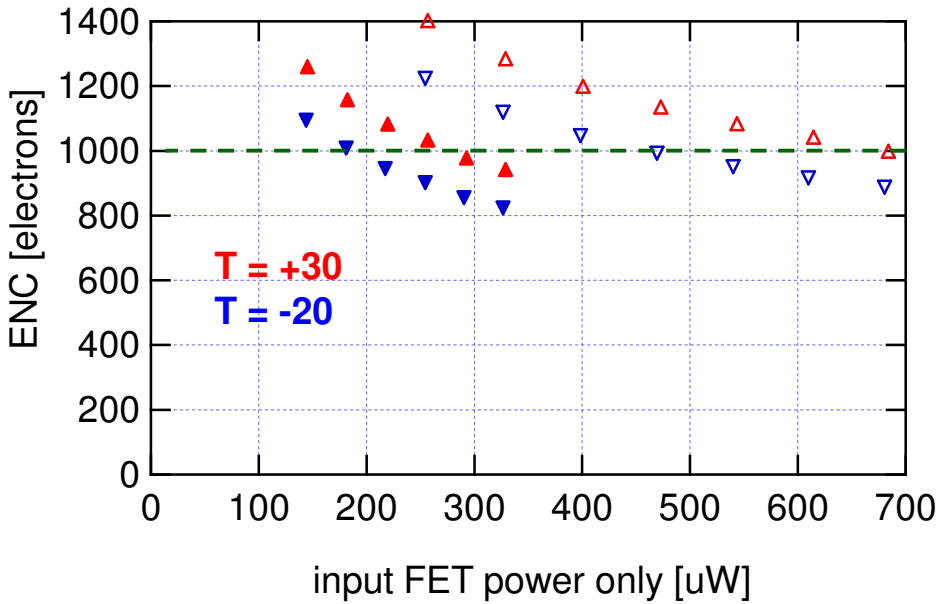
varying current in input FET
($P_{FET} = I_{FET} \times 1.2$)

choose 2 input capacitance values

simulations for typical process params only, T = +30 and -20







closed symbols
Cadded = 10 pF total (2 stray + 8 sensor)
<1000e for ~250uW in I/P FET for T~0

open symbols
Cadded = 15 pF total (2 stray + 13 sensor)
<1000e for ~600uW in I/P FET for T~0

must add ~100uW for rest of front end
+ digital

front end conclusions

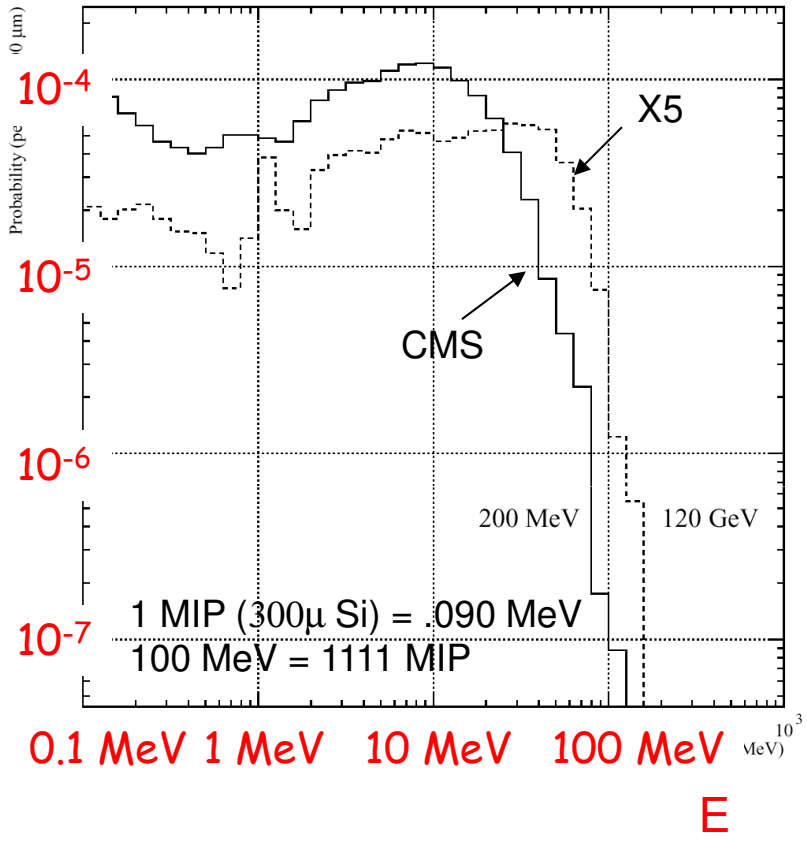
preamp/postamp **pre-layout** design modifications now well advanced

- core amplifier circuits mostly left alone
- specifications met
- design robust to temperature and process variations
  - minimal pulse shape variations
- CBC2 shortcomings addressed (preamp cascode and postamp feedback)

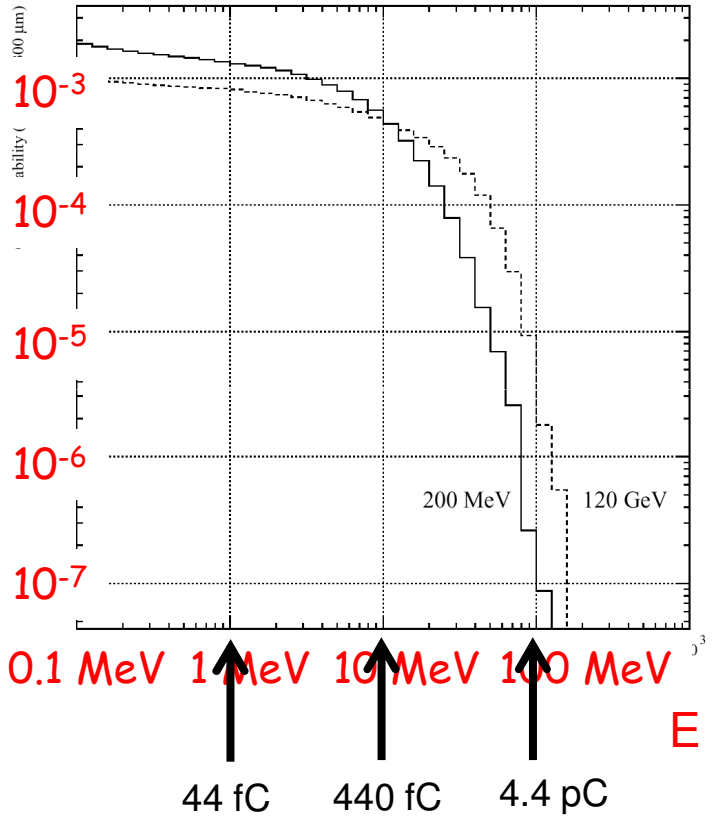
comparator still needs looking at to achieve neutral current consumption

now look at hips behaviour - M.Huhtinen simulations

Differential Energy spectrum: Probability/incident pion of depositing energy E in 300µm Si layer



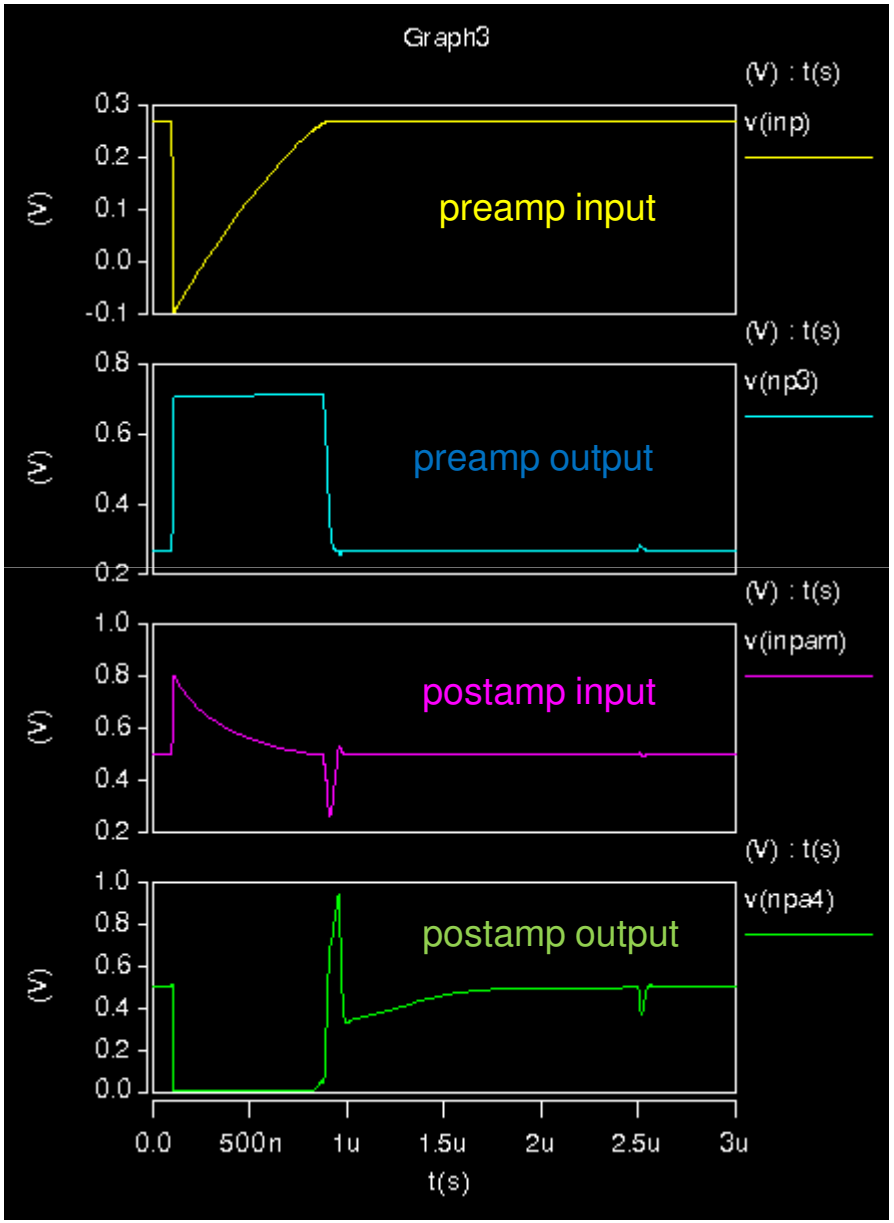
Integral spectrum: total prob. of pion depositing energy > E



spec. based on what is achievable

channel receiving 4 pC signal should be sensitive to normal signals after 2.5 usec

hips behaviour



single channel response

4 pC injected at t=100ns, 2.5 fC injected at t=2.5us

preamp can't "swallow" 4 pC
=> voltage builds up at input and discharges away through feedback resistance

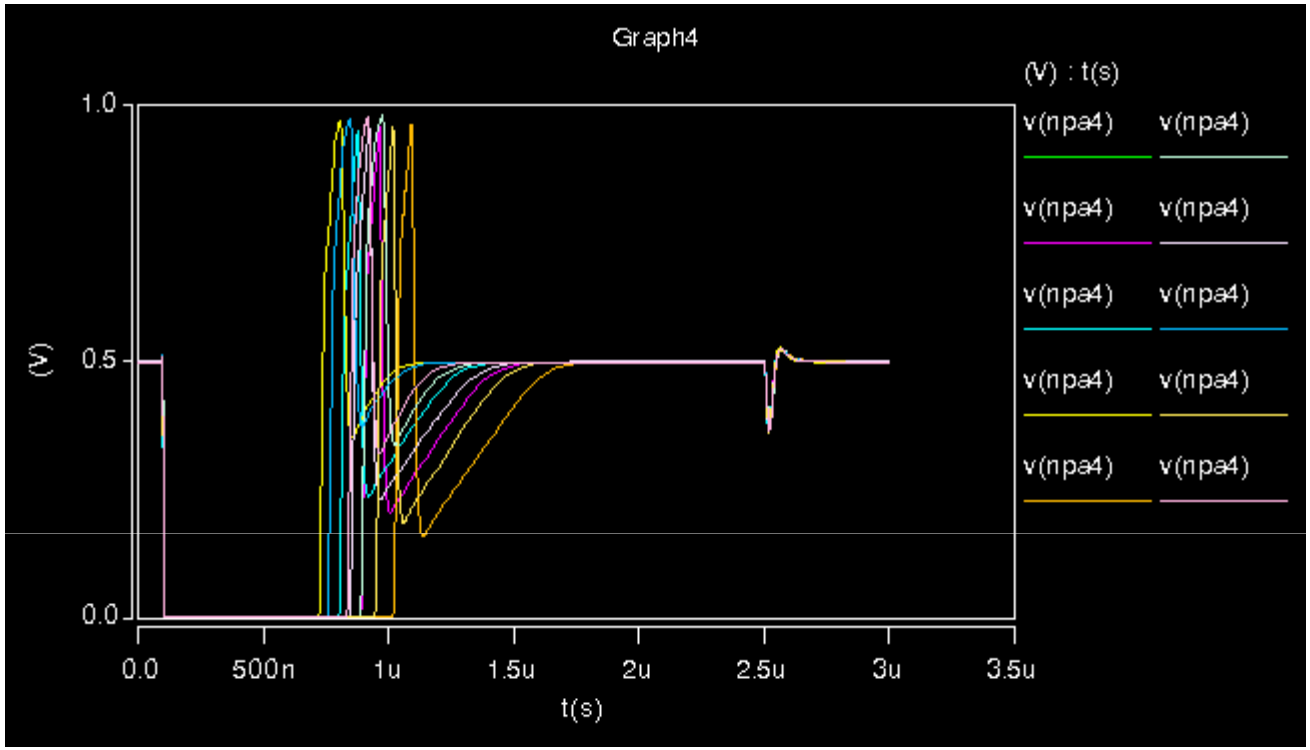
preamp output saturates until charge has decayed away, then returns quickly to baseline

preamp output injects signal into postamp input via 1pF coupling capacitance. +ve signal discharges slowly (postamp feedback in high resistance region) -ve signal discharges quickly (postamp feedback in low resistance region)

postamp output initially saturates -ve
when preamp output recovers postamp output initially saturates +ve, recovers quickly but overshoots then recovers more slowly to baseline

back to normal sensitivity within 2.5 usec

hips behaviour - single channel response

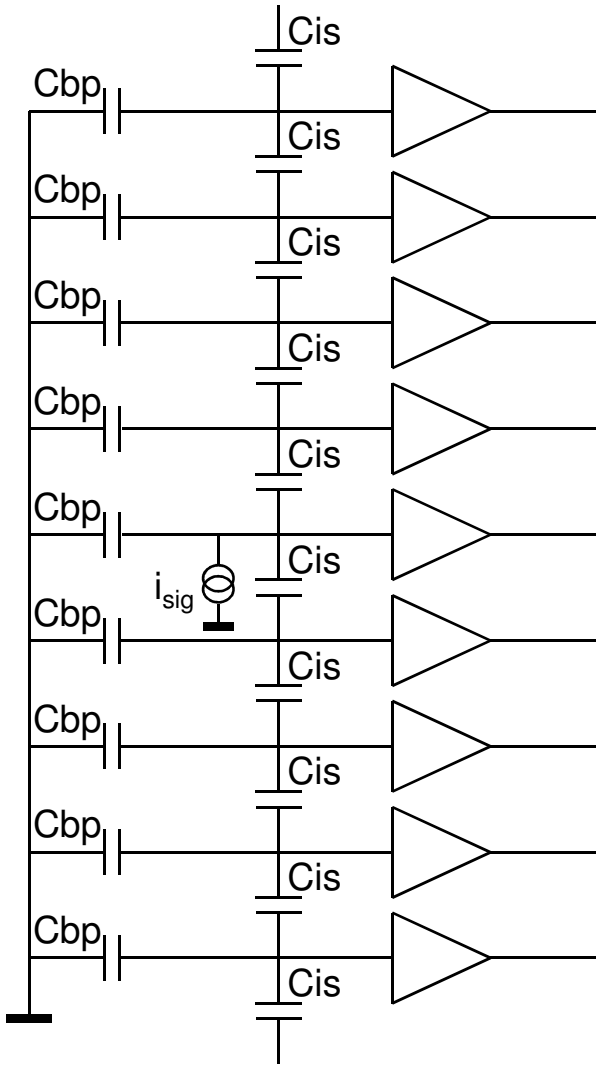


single channel postamp output response

4 pC injected at t=100ns, 2.5 fC injected at t=2.5us
all process corners, T=- 20 and +30

longest recovery for slow N & slow P corner at T= -20

multi-channel behaviour

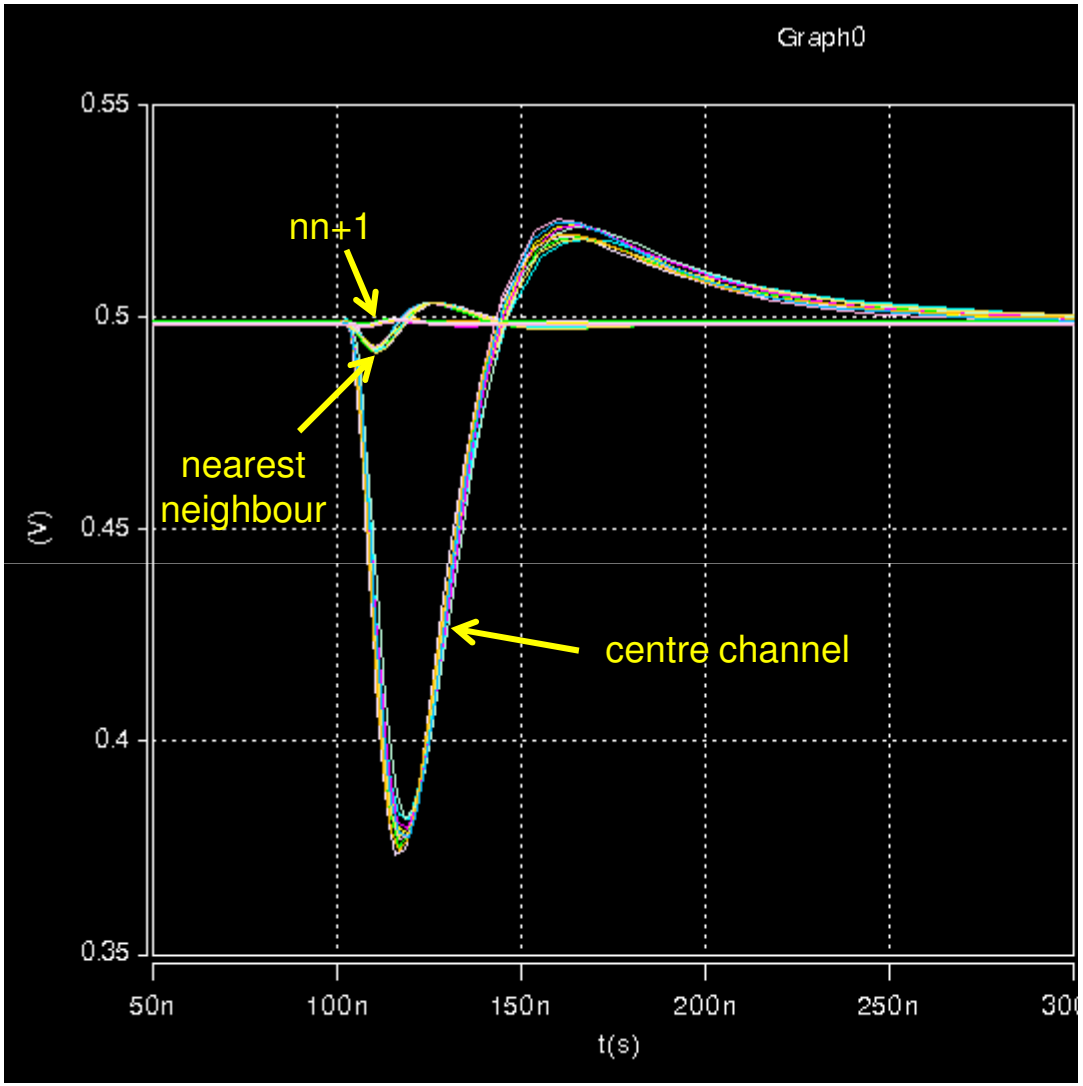


simulations here for Cis = 2.5pF, Cbp = 2pF, Cstray = 2pF
=> Ctot = 9 pF

inject charge into central channel

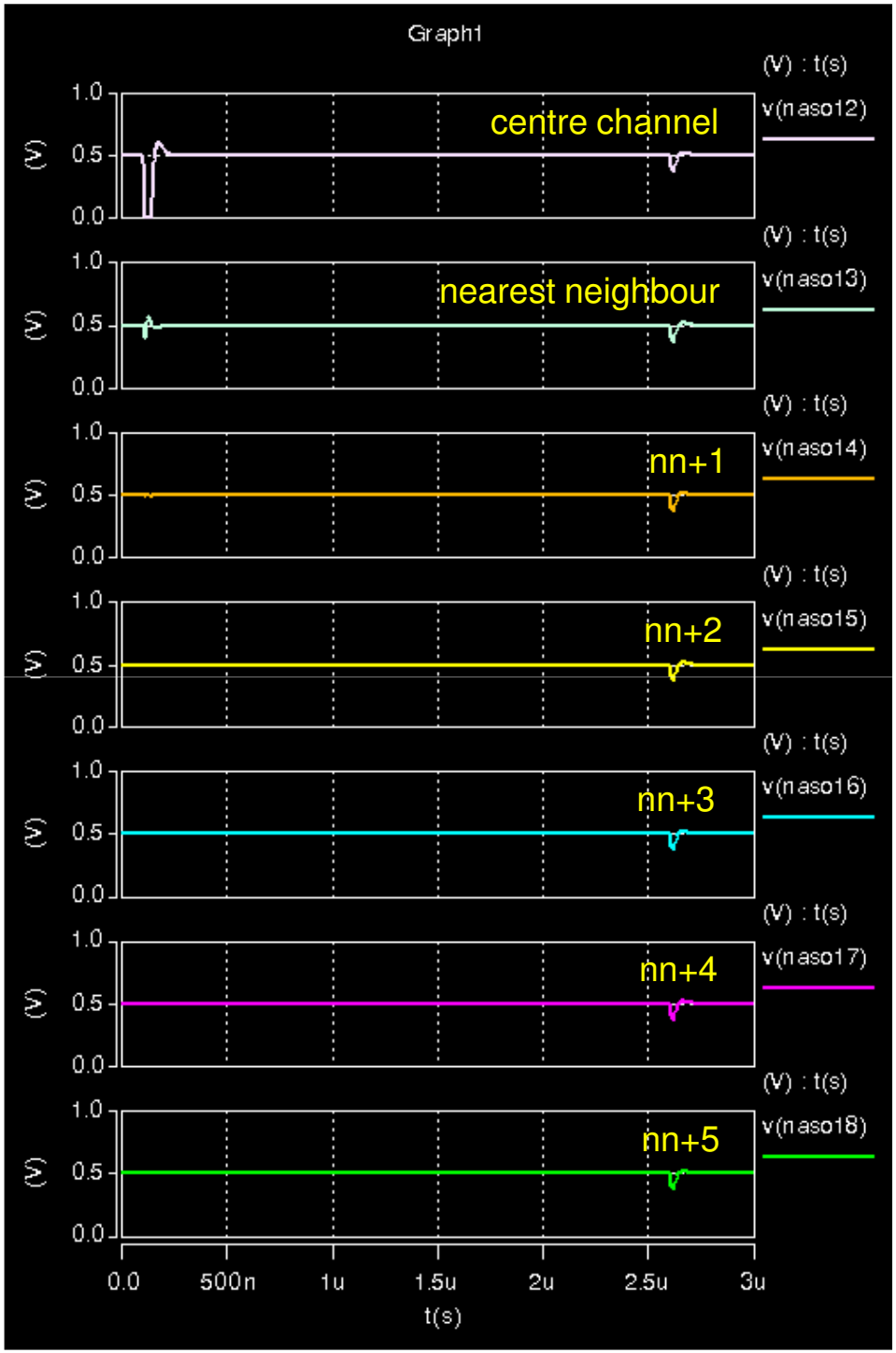
look at postamp output for
central channel
nearest neigbour,
nearest neighbour +1
….

interstrip crosstalk



2.5 fC charge injected
T=-20/+30
all corners
nominal biases

nearest neighbour peak
crosstalk ~ 5 %

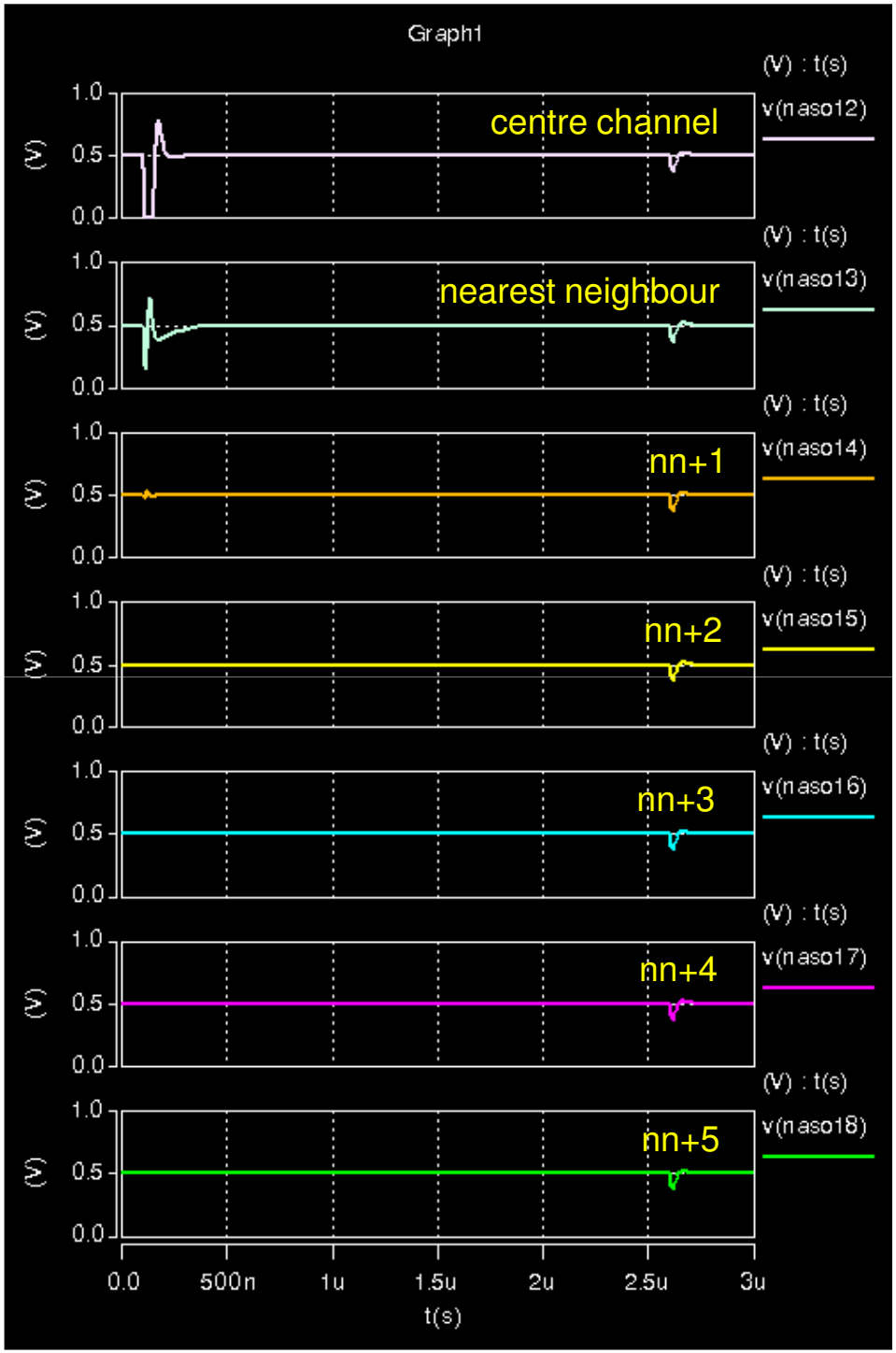


hips

40fC injected on centre channel at t = 100 nsec
(nominal bias conditions, typical process params)

2.5 fC injected on all channels at t = 2.5 usec

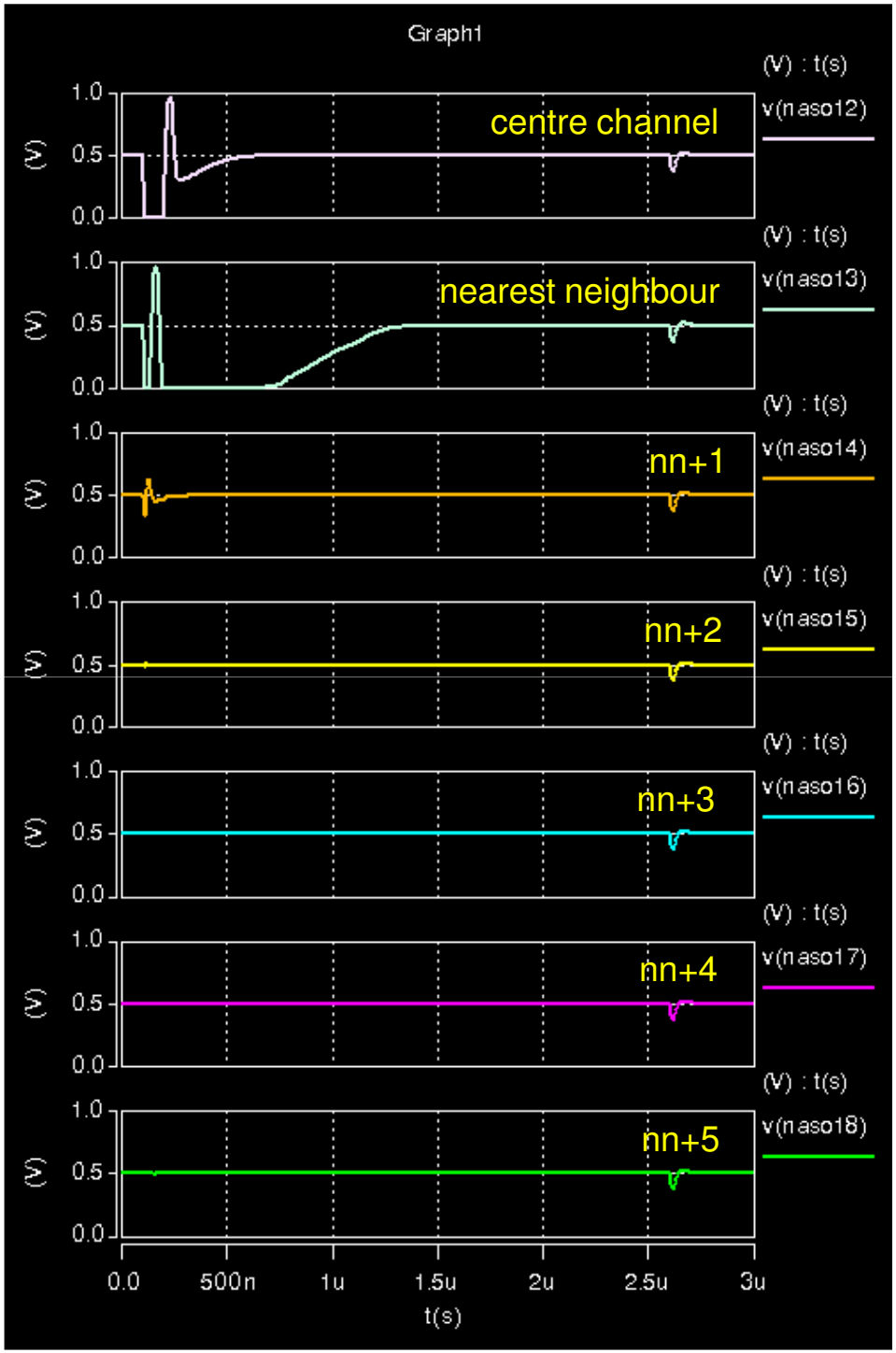
(5 mips = ~13 fC)



hips

100fC injected on centre channel at t = 100 nsec

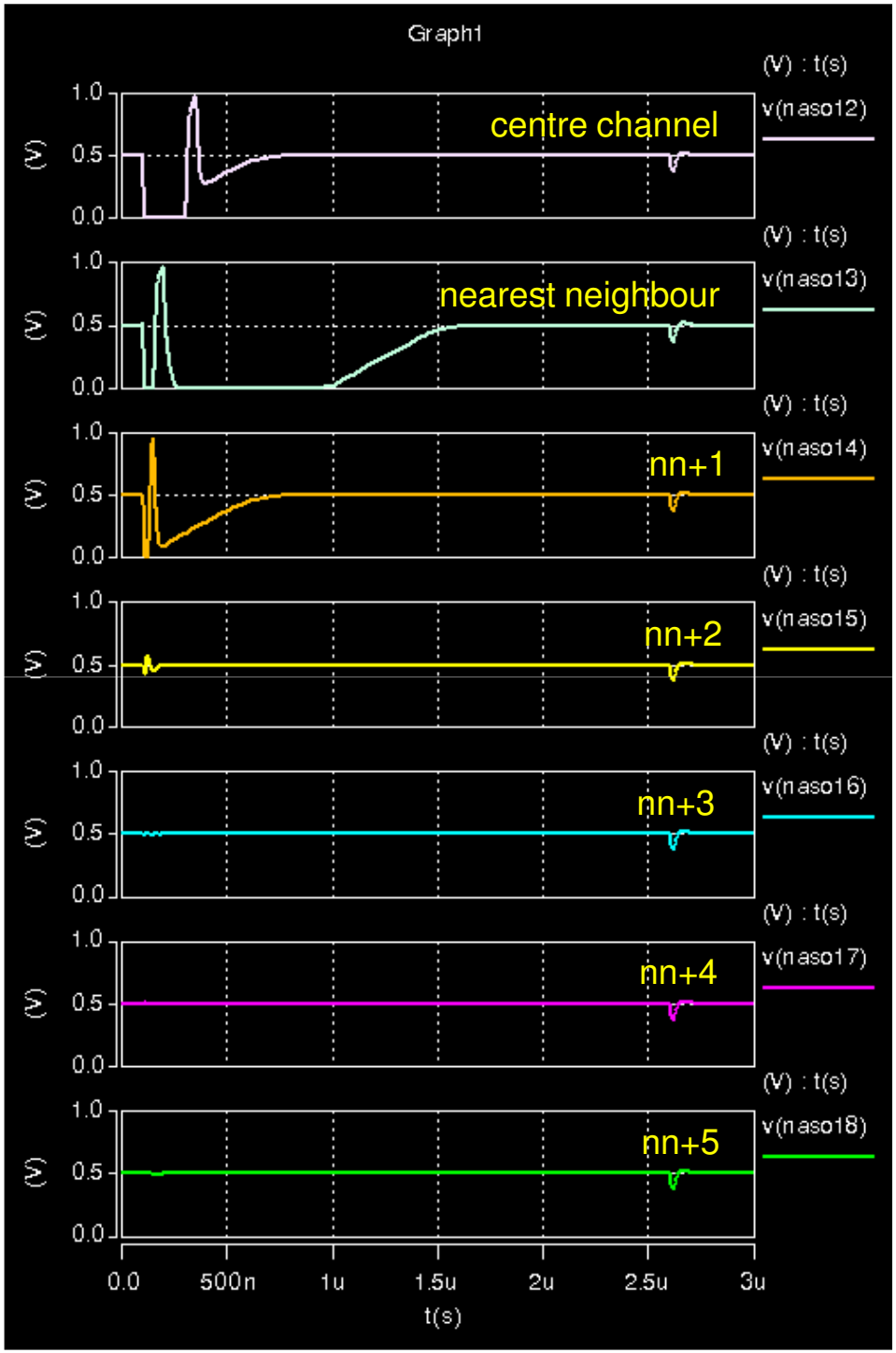
2.5 fC injected on all channels at t = 2.5 usec



hips

400fC injected on centre channel at t = 100 nsec

2.5 fC injected on all channels at t = 2.5 usec

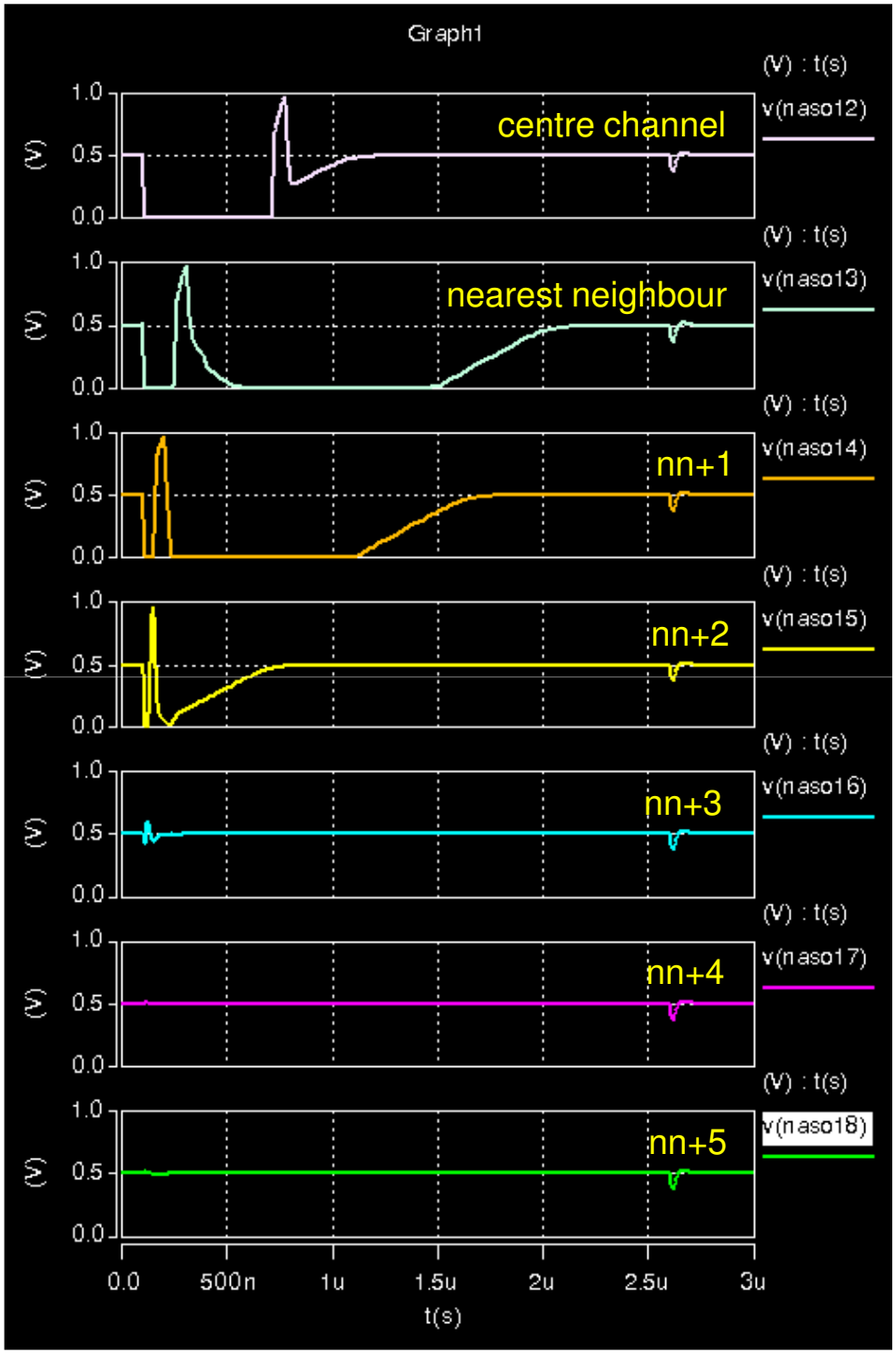


hips

1pC injected on centre channel at t = 100 nsec

2.5 fC injected on all channels at t =2.6 usec

all channels recovered by ~1.5 usec



hips

4pC injected on centre channel at t = 100 nsec

2.5 fC injected on all channels at t = 2.6 usec

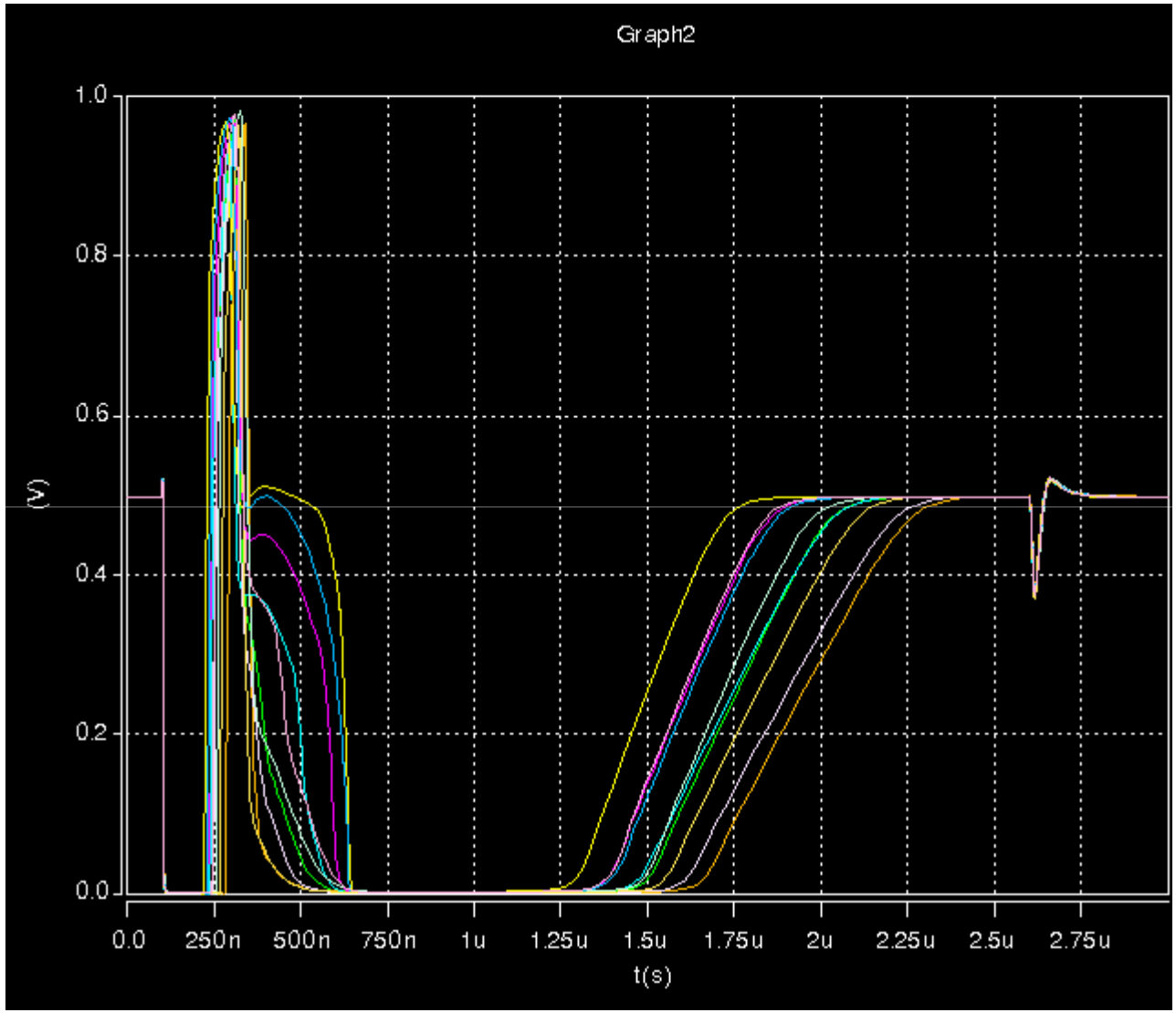
all channels recovered within ~2 usec

centre channel recovers before
nn, nn+1, ~nn+2

significant deadtime for centre chan.,
nn, nn+1, nn+2

nn+3 etc. ~ok

hips worst case



4pC injected on centre channel
at t = 100 nsec

2.5 fC injected on all channels
at t = 2.5 usec

look at worst channel nn+1

T=-20, +30, all corners

all channels recovered by
2.5 usec irrespective of
sim. conditions

hips and multi-channel simulations summary

interchannel crosstalk at ~5% level for normal signals

hips effects confined to central hit strip and some neighbours

number of neighbours depends on signal size

worst case 7 channels for 4 pC

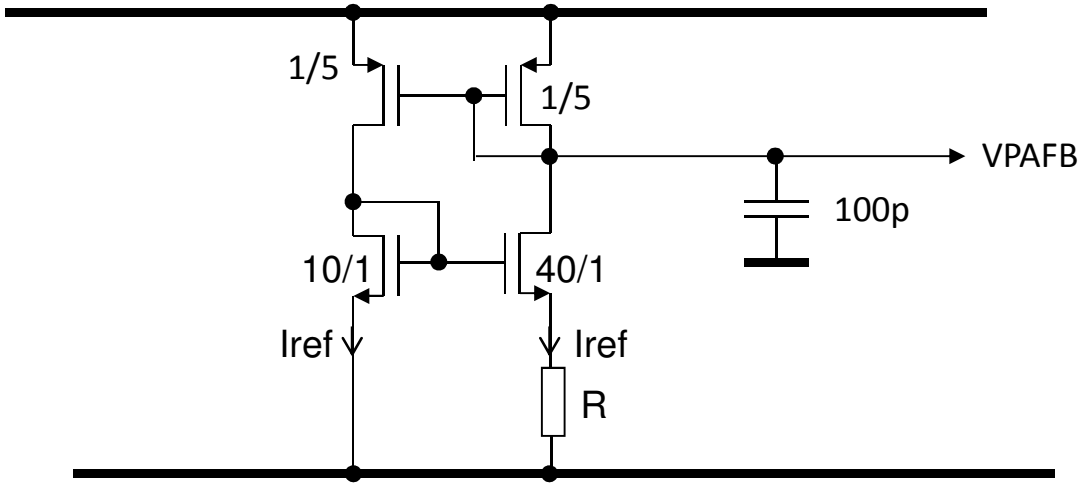
~ 3-4 channels for 400 fC

~ negligible effect up to ~40 fC

BACKUP

beta multiplier "explained"

$\beta = \mu C_{OX}(W/L)$ [proportional to W]



upper mirror forces same current (Iref) to flow in both lower transistors

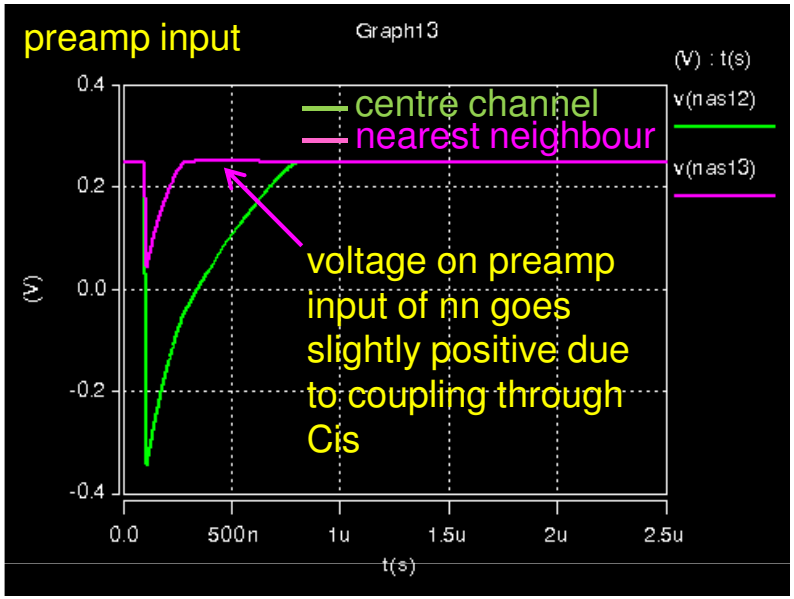
ok if V_{GS}(left) > V_{GS}(right), which can be achieved by making right NMOS wider than left by multiplier factor K (40/10)

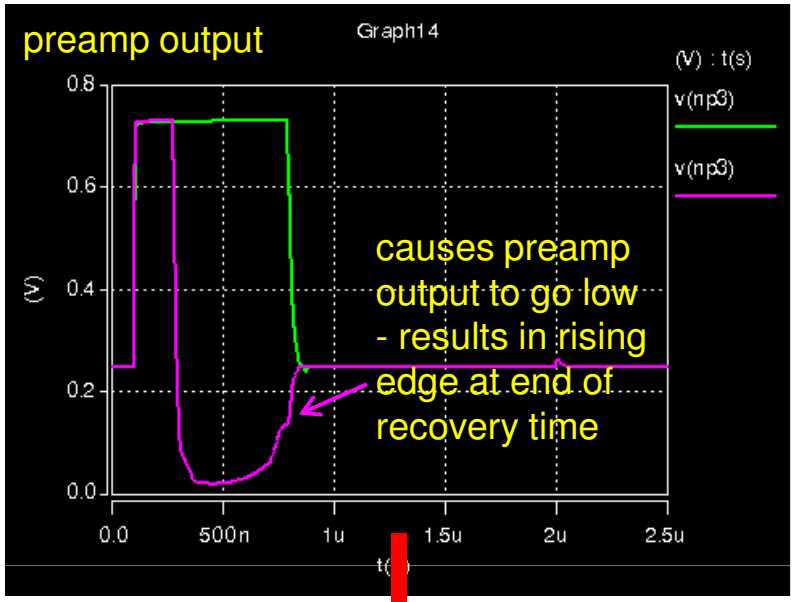
in weak inversion $I_{ref} = \frac{nU_T \ln K}{R}$ ($U_T = kT/q$)

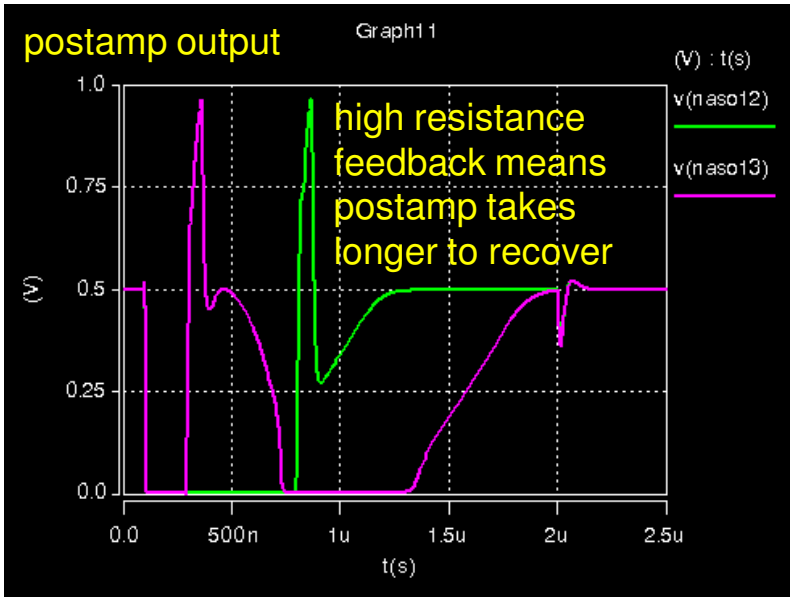
=> R ~ 5M for Iref = 10nA (n ~ 1.4, K=4, U_T ~ 25 mV)

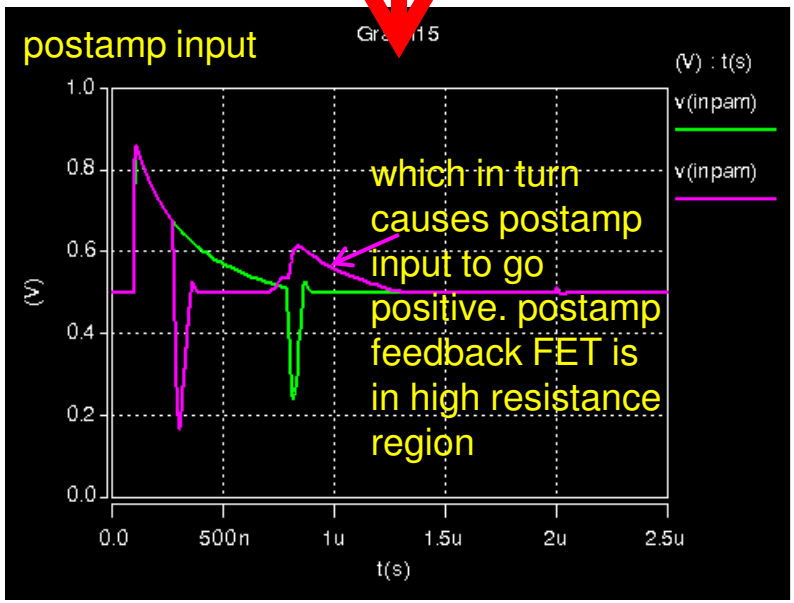
see *CMOS Circuit Design, Layout and Simulation (3rd ed.) R. Jacob Baker*, chapter 20 (particularly page 635 for weak inversion design)

why is nearest neighbour deadtime worse than centre channel?

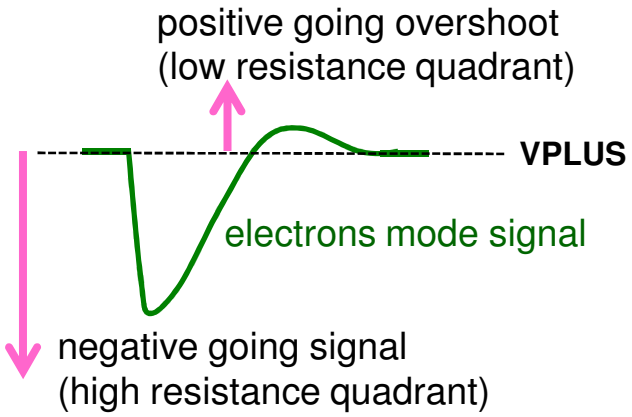


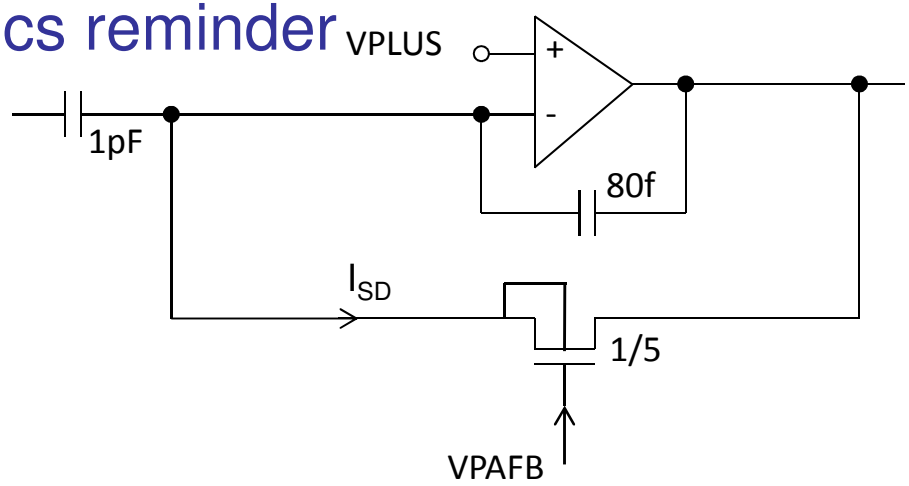


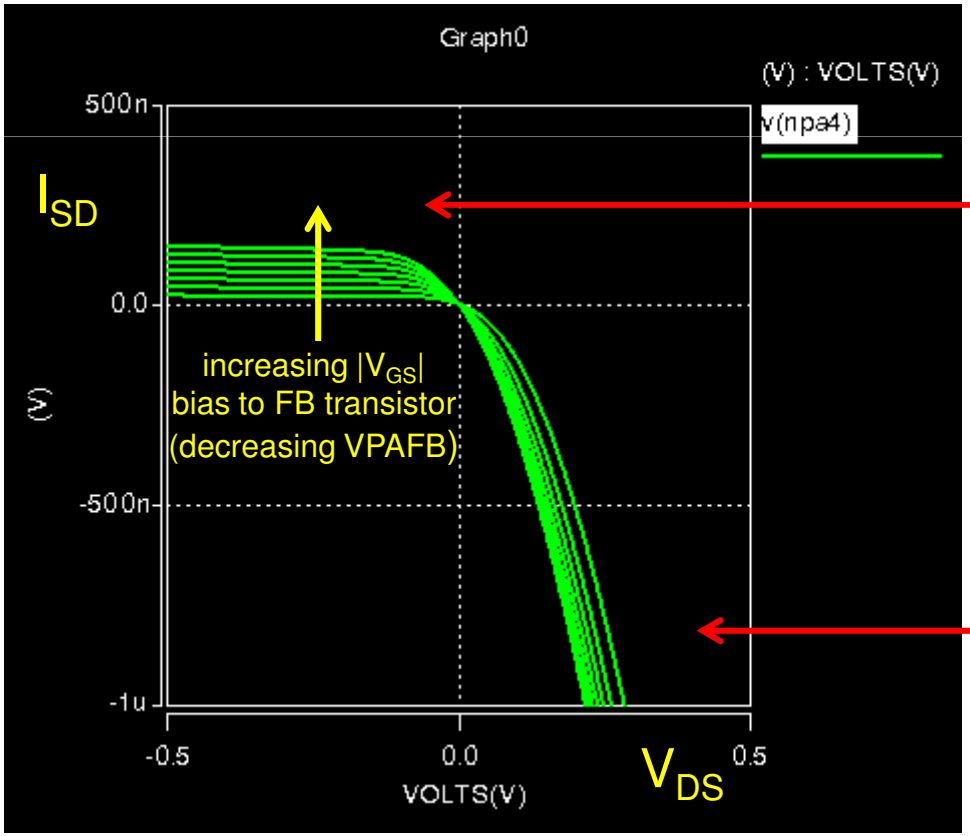


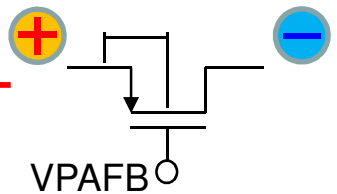


postamp feedback characteristics reminder

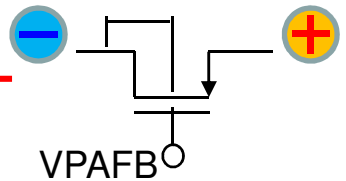






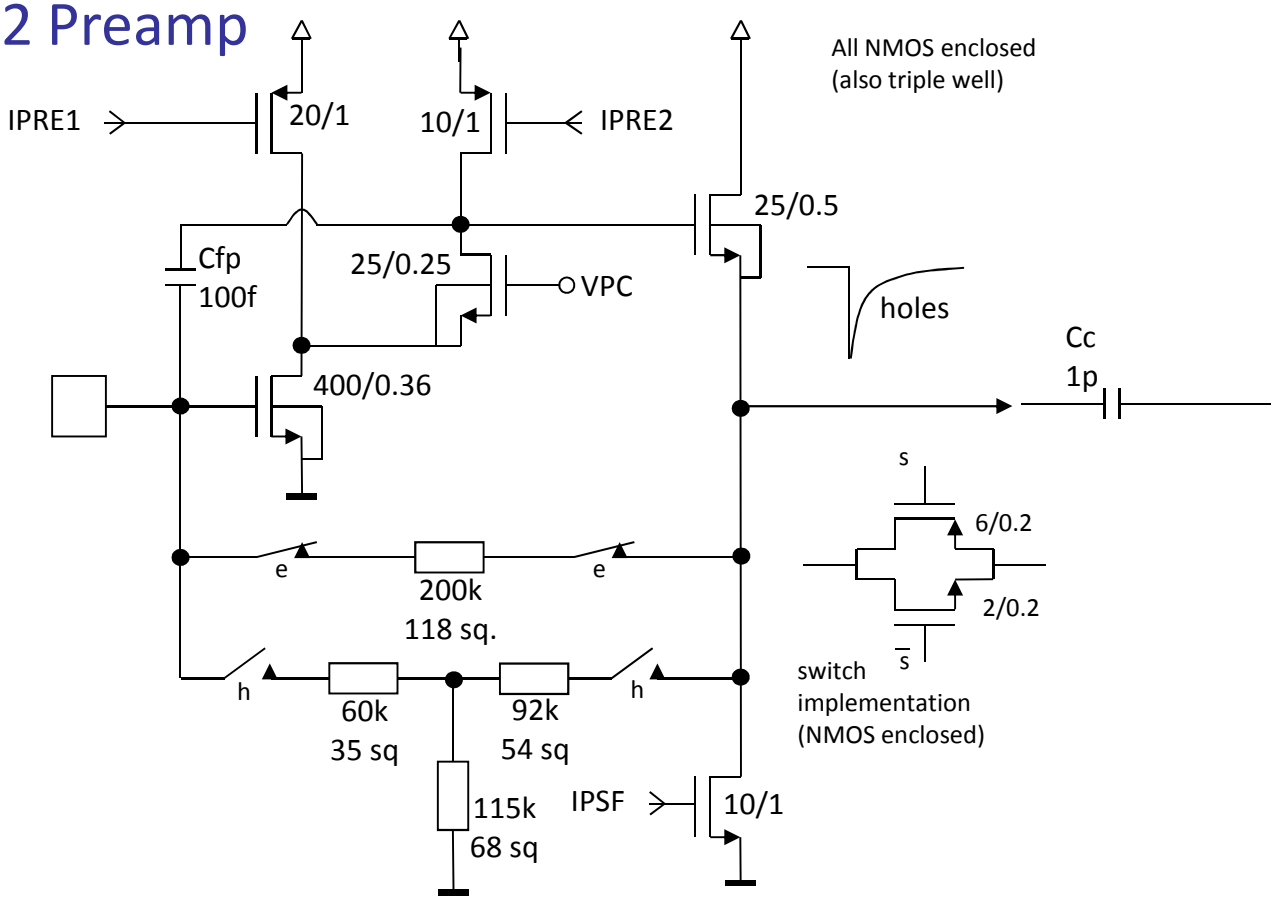


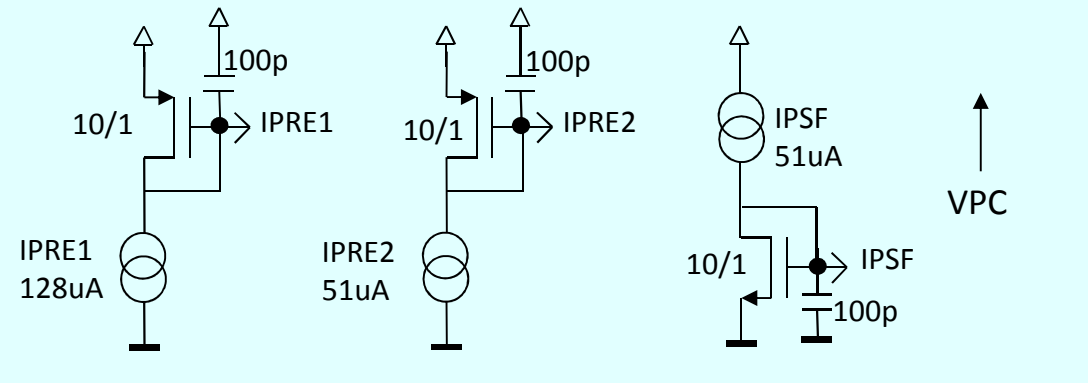
-ve going signal region
source at input side of postamp
V_{GS} ~ constant
only V_{DS} varies



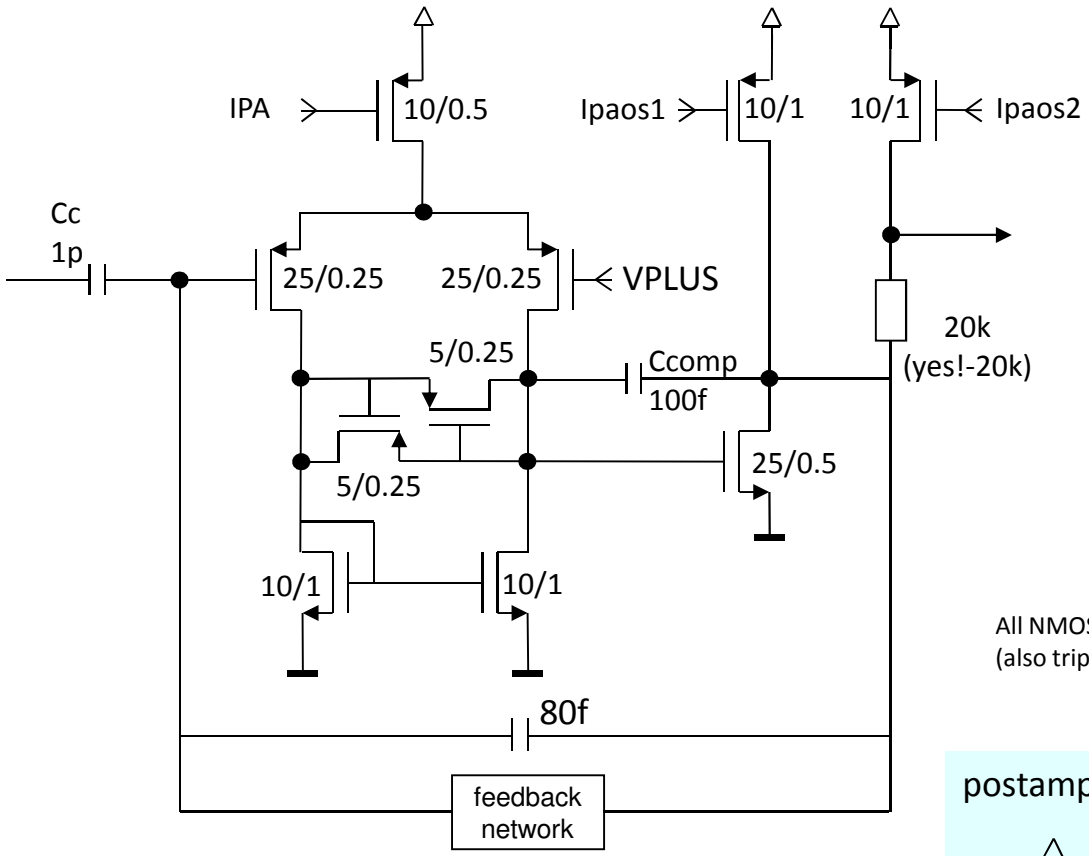
+ve going overshoot region
source swaps to output side
V_{GS} increases as postamp output overshoot increases

CBC2 Preamp


All NMOS enclosed
(also triple well)
IPRE1
20/1
10/1
IPRE2
25/0.5
Cfp
100f
25/0.25
VPC
holes
Cc
1p
400/0.36
s
6/0.2
2/0.2
s
e
e
200k
118 sq.
switch
implementation
(NMOS enclosed)
h
h
60k
35 sq
92k
54 sq
115k
68 sq
IPSF
10/1

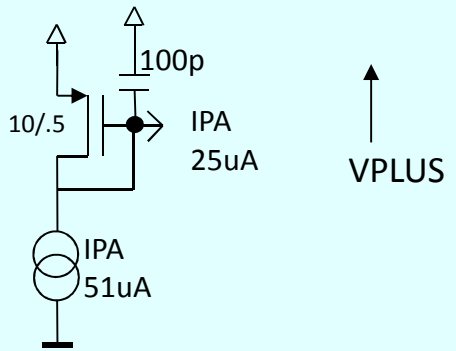

100p
10/1
IPRE1
IPRE1
128uA
100p
10/1
IPRE2
IPRE2
51uA
IPSF
51uA
VPC
10/1
IPSF
100p

CBC2 Postamp

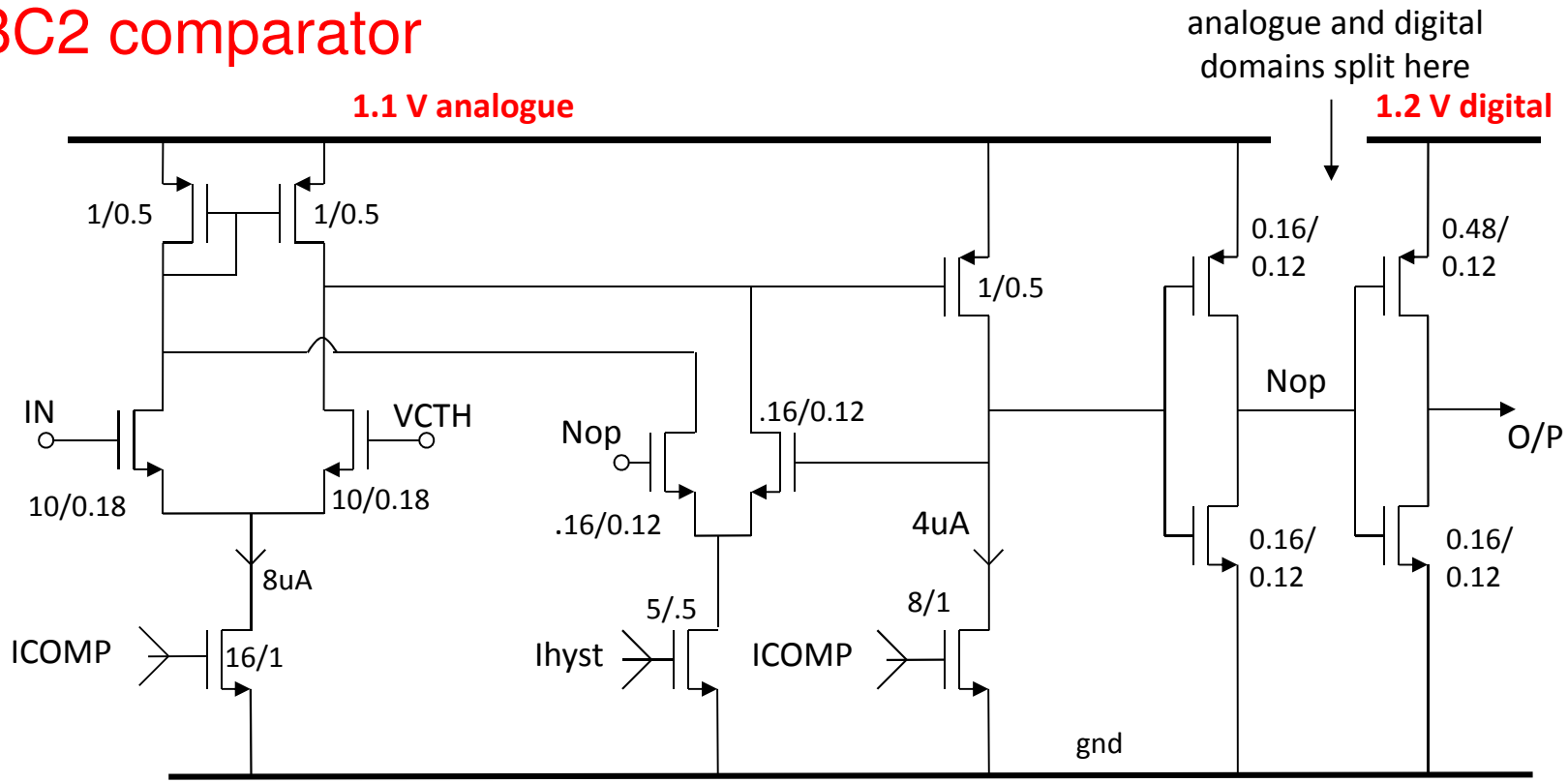


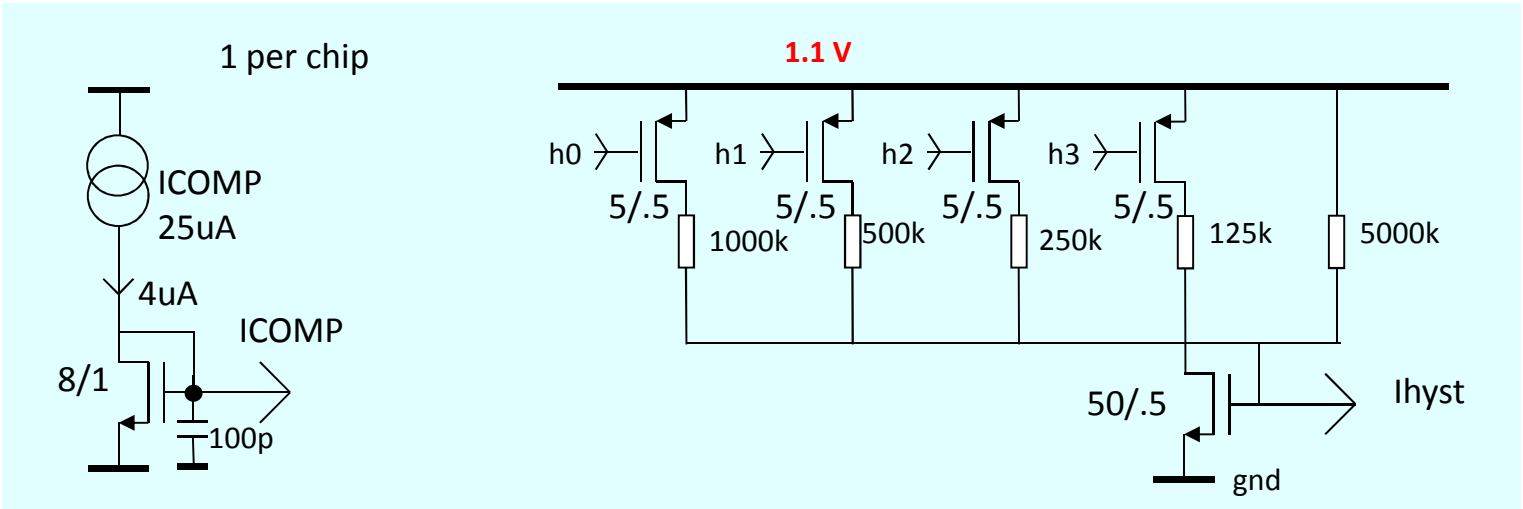
All NMOS enclosed
(also triple well)

postamp bias (1 per chip)



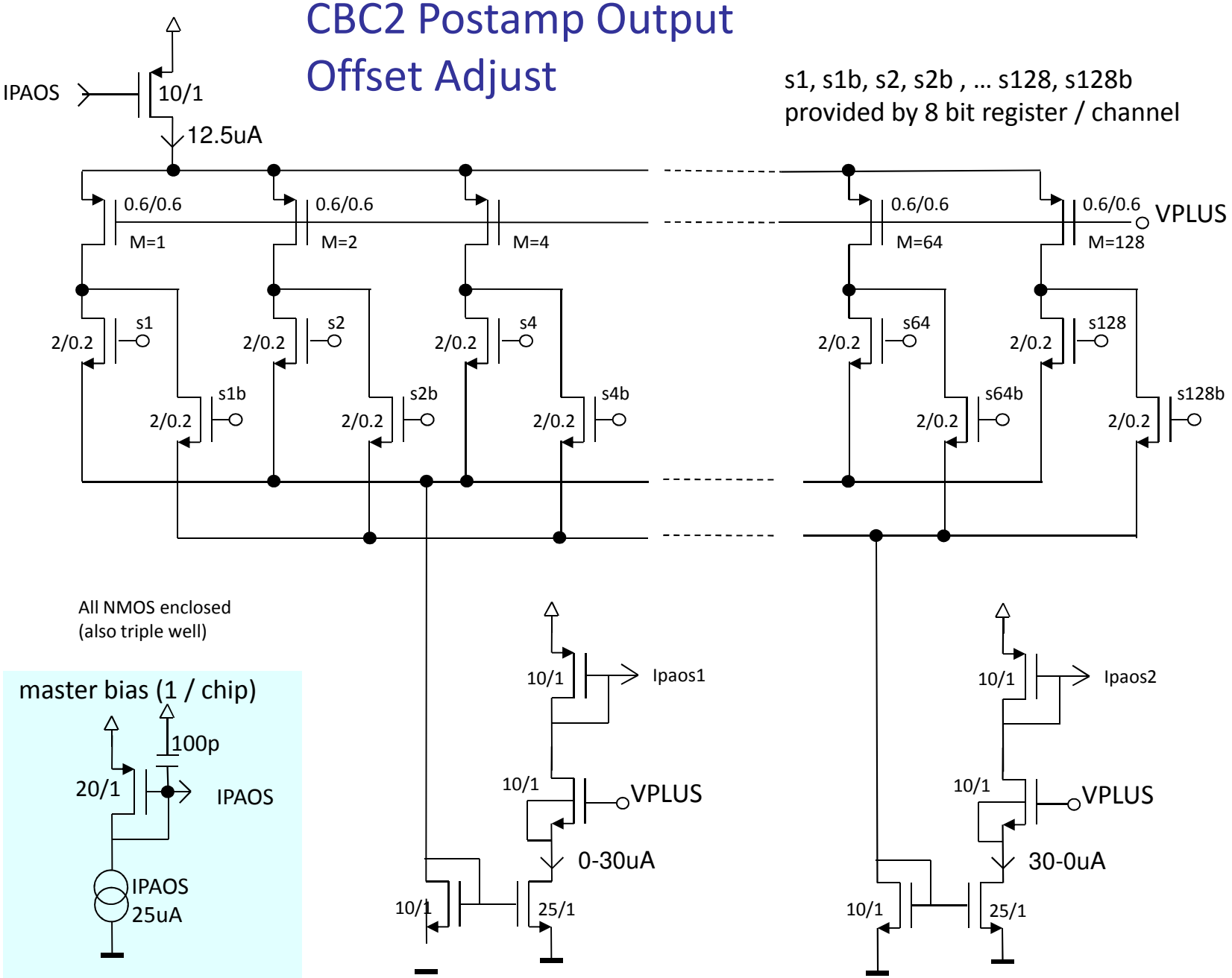
CBC2 comparator





CBC2 Postamp Output Offset Adjust

s1, s1b, s2, s2b , … s128, s128b
provided by 8 bit register / channel



CBC2 postamp feedback