CBC3 powering issues

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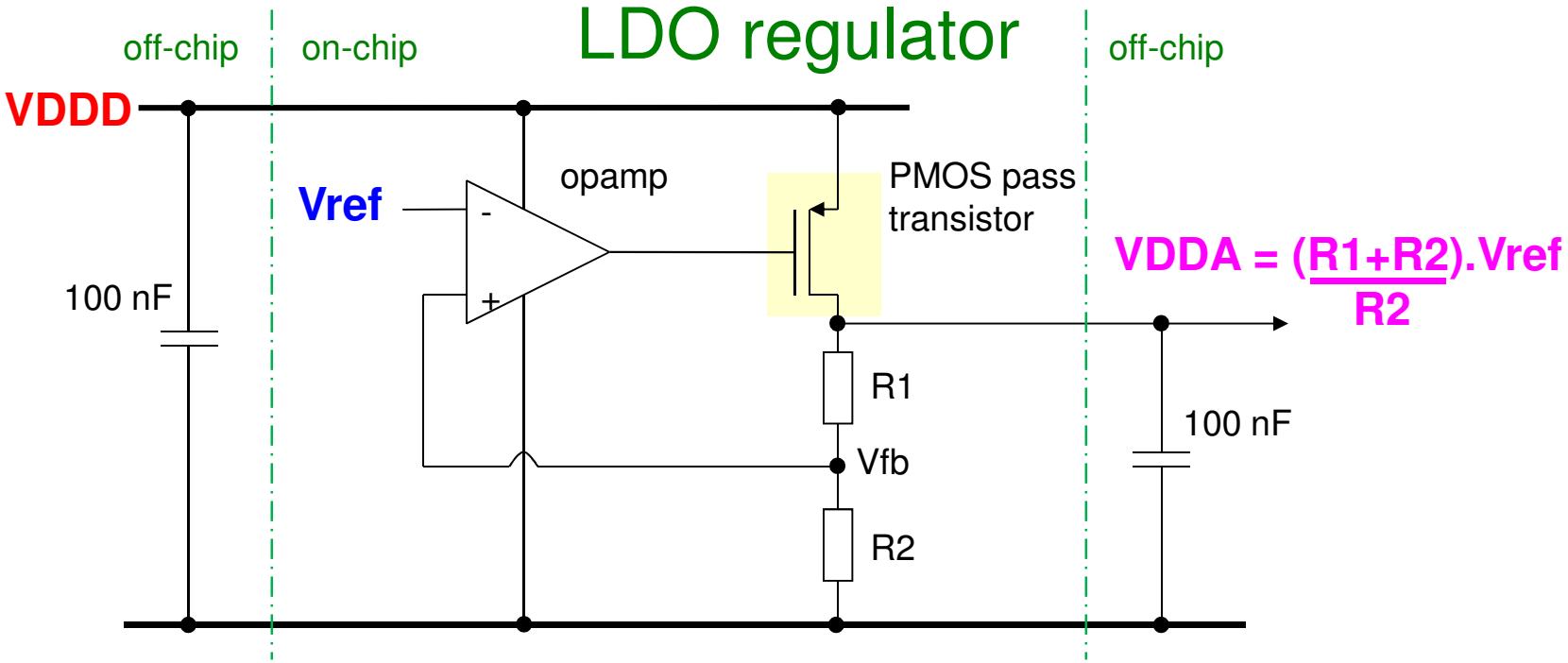
systems meeting, 4th June, 2015.

CBC2 powering scheme



CBC2 issues

Vref comes from bandgap (~0.6V)

analogue stages designed for VDDA > 1.1 V

needed to deal with both polarity input signals + tolerate DC coupling

=> VDDD needs to be > 1.2 to ensure headroom for LDO dropout voltage

and to tolerate expected bandgap voltage variations

moving to CBC3

sensor polarity chosen and AC coupled

analogue stages now adjusted to cope with 1V minimum for VDDA

some numbers

module power supply tolerances

more pessimistic: VDDD ± 10%: 1.08 - 1.2 - 1.32
less pessimistic: VDDD ± 5% 1.14 - 1.2 - 1.26

bandgap tolerance

quoted bandgap variations 619 mV ± 22 mV
and we have measured +25 mV drift after ionizing irradiation

=> 597 mV - 666 mV worst case bandgap range (632 ± ~5%)

have to design LDO to give VDDA = 1.0 V for minimum Vref (bandgap) of 597 mV

=> LDO "gain" = 1/.597 = 1.68

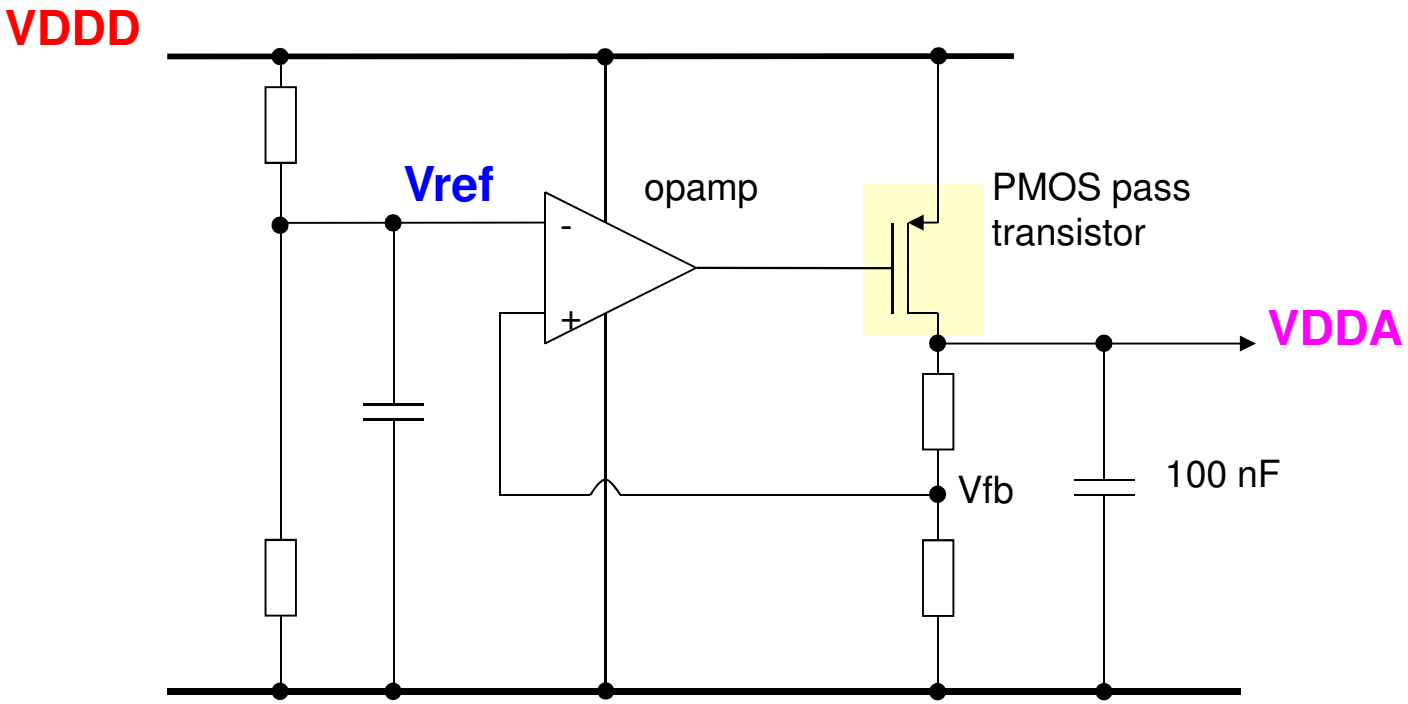
but if bandgap were to be maximum 666 mV then VDDA = 1.68 x 0.666 = 1.11 V

worst case scenarios

bandgap is at maximum , so VDDA = 1.11V
VDDD is at -10% minimum 1.08V <- **clearly doesn't work (Vout > Vin!)**
VDDD is at -5% minimum 1.14V <- **30 mV dropout not enough for LDO**

problem arises because bandgap and VDDD variations will not be correlated

possible CBC3 approach



possible solution - don't use bandgap for LDO reference

instead use divided down (and filtered) version of VDDD
1 Megohm & 100pF components easily achievable (even bigger time constants if necessary)

adjust LDO resistors for 1.1 VDDA output at nominal 1.2 VDDD

possible CBC3 approach - effect of VDDD variation

VDDD ±10%

	min	nom	max
VDDD [V]	1.08	1.2	1.32
Vref [V]	0.54	0.6	0.66
VDDA [V]	0.99	1.1	1.21
dropout [mV]	90	100	110

VDDD ±5%

	min	nom	max
VDDD [V]	1.14	1.2	1.26
Vref [V]	0.57	0.6	0.63
VDDA [V]	1.05	1.1	1.16
dropout [mV]	95	100	105

comments

all voltages correlated: VDDD, Vref (=VDDD/2), VDDA (=Vref x LDO gain)

dropout situation should be ok at > 90 mV

max - min VDDA range
0.99 - 1.21 for VDDD ± 10% scenario
1.05 - 1.16 for VDDD ± 5%

(minimum is the more important parameter here)

comments

using divided down voltage from VDDD for Vref to LDO may be best way to go

- VDDA of > ~1.0 V is maintained
- can still benefit from supply filtering effect of LDO
- Vref and VDDA correlated with VDDD so dropout maintained
- VDDD ± 10% can be tolerated

is bandgap still useful?

- not so clear if VDDD **can** be provided with ± 5% tolerance
  - 130nm CBC bandgap range (599 - 666 mV including radiation effects)
    ~ equivalent to ~ ± 5% tolerance

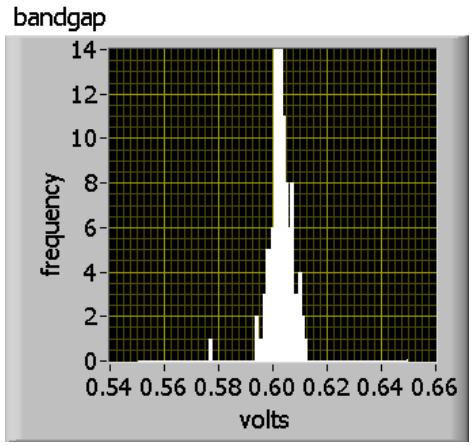
note: we will be relying on accurate rad-hard bandgap in DC-DC chip
(but we probably have to anyway)

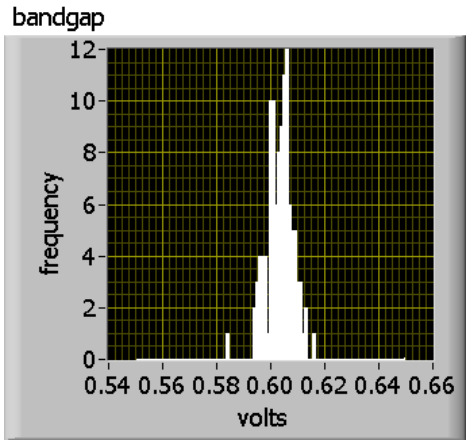
wafer test results

A7PNF7H

AVPNC3H

bandgap voltage

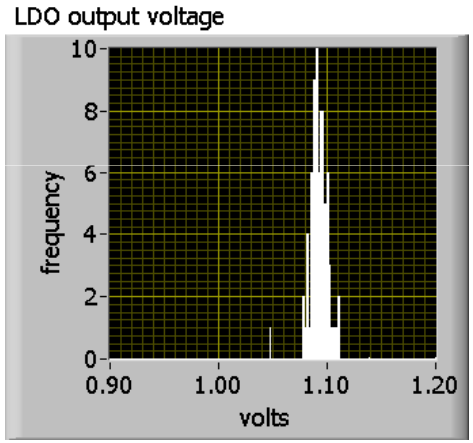


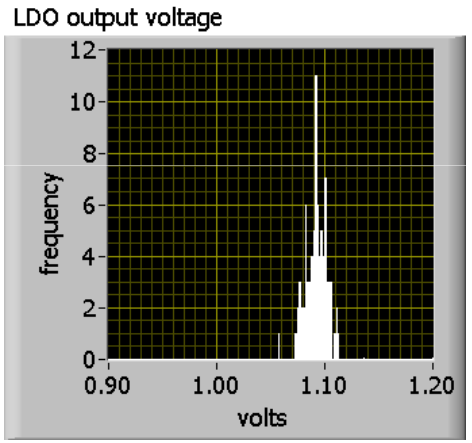


data from all chips from 2 wafers

including rejects

LDO output





bandgap measurements on the low side of the 619 ± 22 expected

but could be a systematic error