CBC3 status

Mark Raymond

recent update from Mark Prydderch in Tracker week (29/1/15)

can’t add much today, but

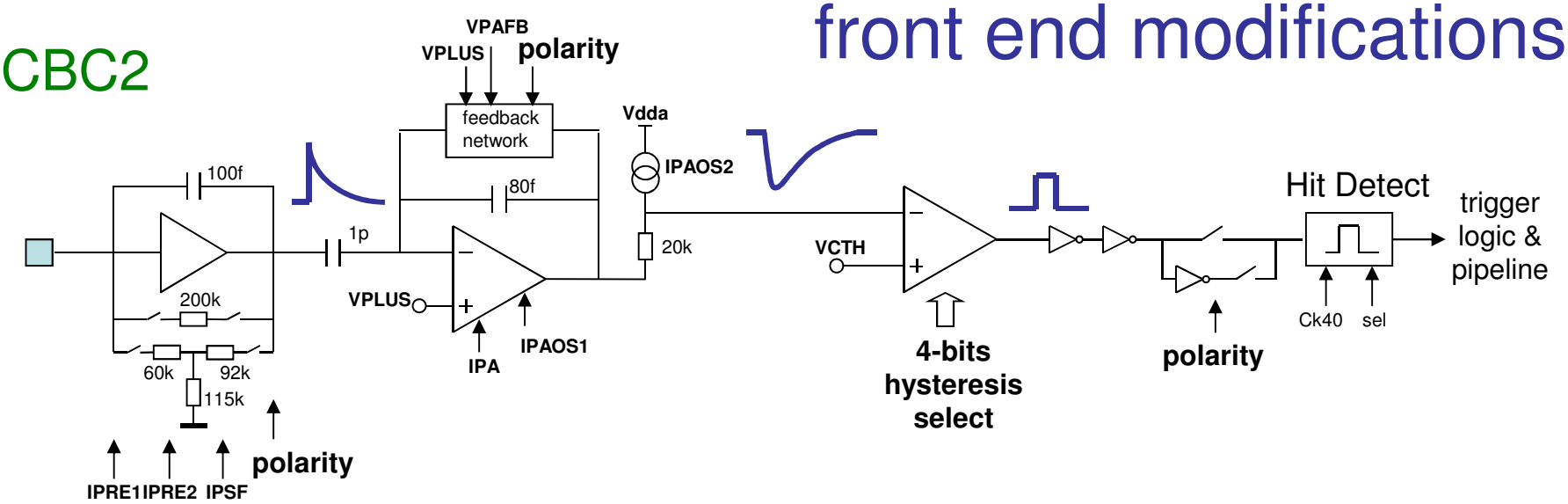
some progress on front end amplifier

CBC3 hit detect functionality

systems meeting, 24th February, 2015.

front end modifications

CBC2



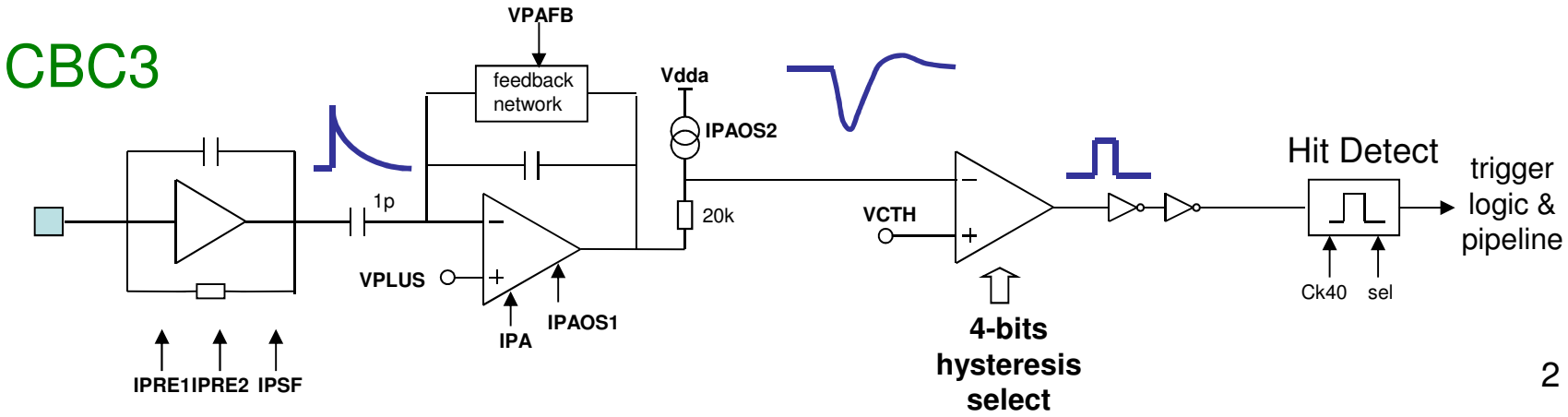
preamp/postamp

- remove polarity option
- faster pulse shape (return to baseline within 50 nsec)
- increase input device current programmable range
  (capability to cope with larger input capacitance)
- 1V VDDA operation

postamp/comparator

- fix CM stability issue
  balance comparator current
  re-visit postamp feedback biasing

CBC3



front end amplifier

have made adjustments for:

- VDDA = 1V from LDO
- capability to run with higher current
  in input transistor
- shorter overall pulse shape

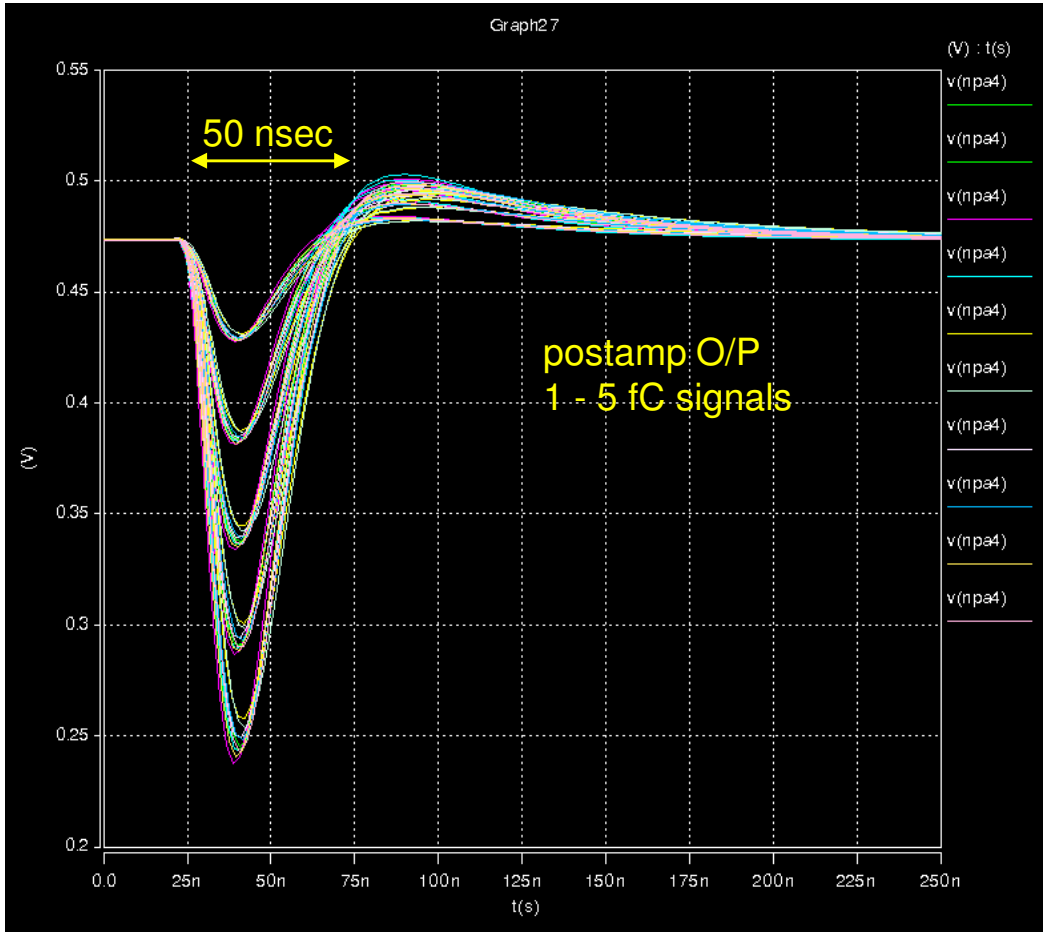
consequences are:

- optimal performance for electrons mode only
- AC coupling to sensors (can still sink ~500nA)

status

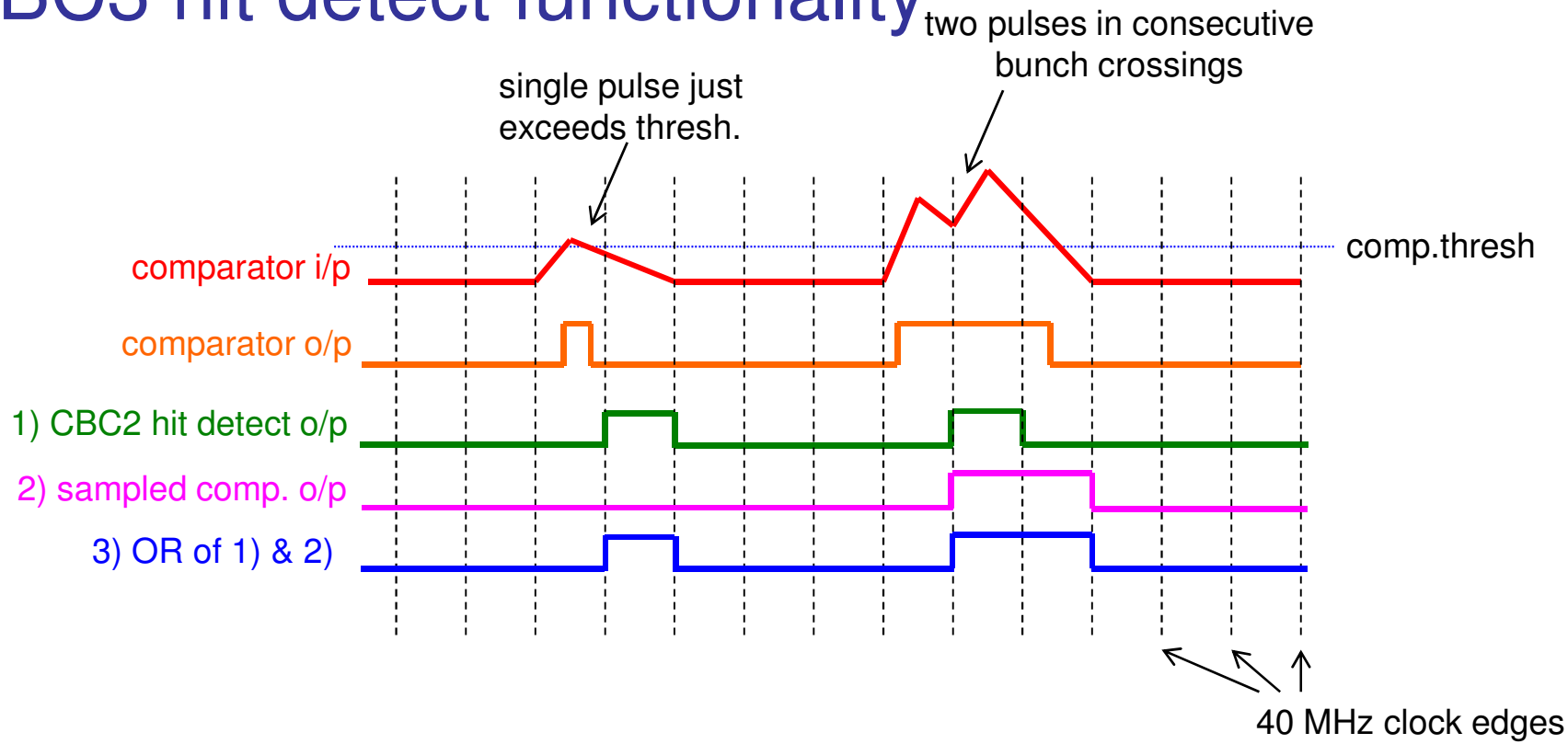
work in progress, but
all specifications seem achievable
~50uW power increase to keep noise within spec.
300uW for CBC2 -> 350uW for CBC3

will report in more detail when design finished



postamp output pulse shape
all process corners, T = +30 and -10
Cin = 8pF
noise ~ 1000e
power ~350uW (preamp + postamp)

CBC3 hit detect functionality



have spent some time understanding required functionality of hit detect circuit for CBC3

(the circuit that captures the comparator output and feeds both correlation logic and pipeline)

CBC3 pulse shape peaks at ~15-20 nsec and falls back to baseline by ~50 nsec

need full efficiency for single pulse that only just exceeds threshold, as well as piled up pulses

=> need OR of CBC2 hit detect and sampled comparator output

other circuitry progress

further layout work to match stub gathering logic to correlation logic now ~complete

stubs overflow flag (>3 stubs) added (will appear in output data)

existing I2C logic: double checking for SEU conditions (issue raised last time)

some bias generator work

S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B2	**SoF**	**R**
S1	S2	S3	B2	?	**R**
S1	S2	S3	B2	?	**R**
S1	S2	S3	B2	**Sync**	**R**

submission

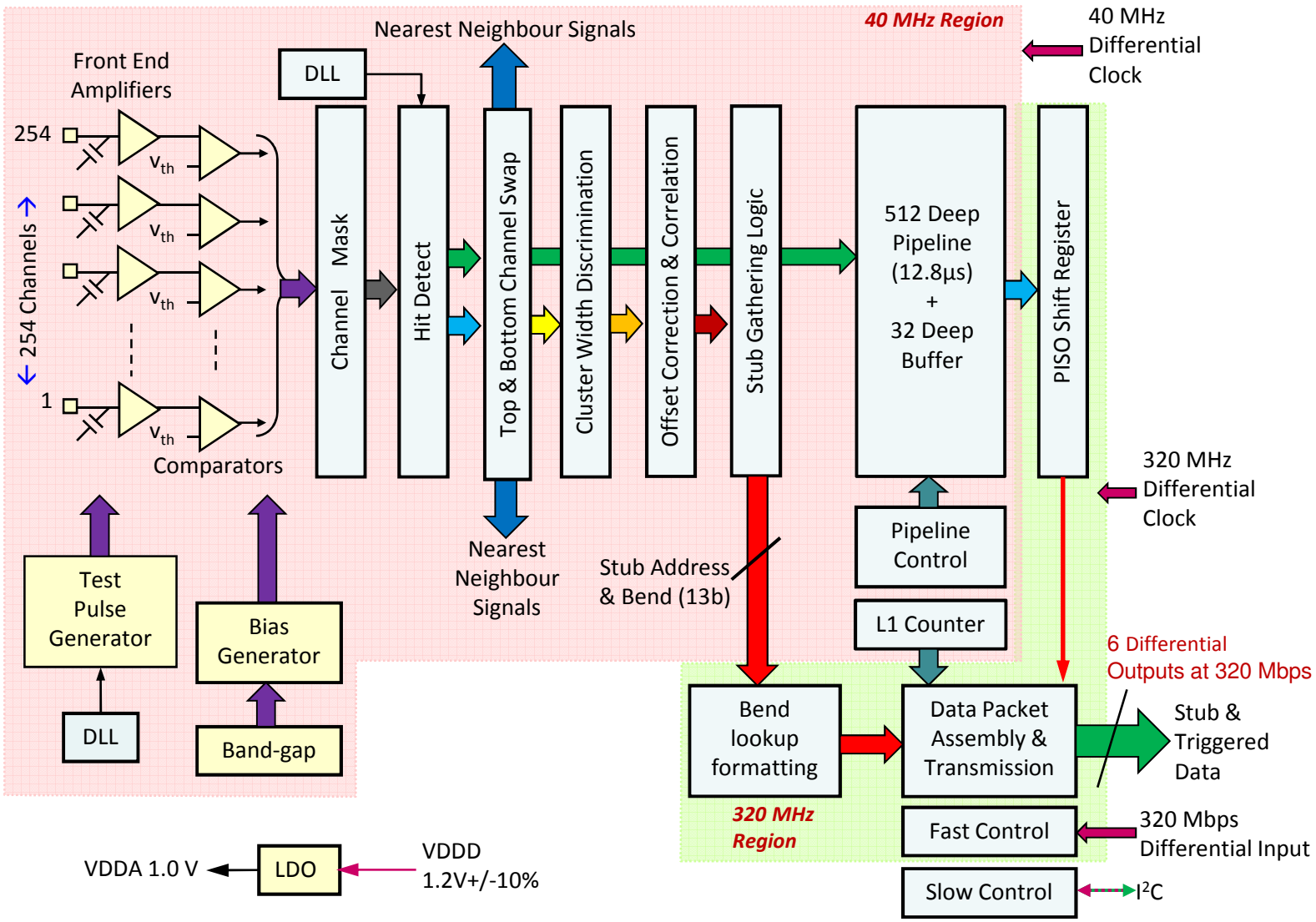
MOSIS MPW schedule has submssion dates November 16th 2015, February 16th 2016

November date looks tight, February now probably more likely

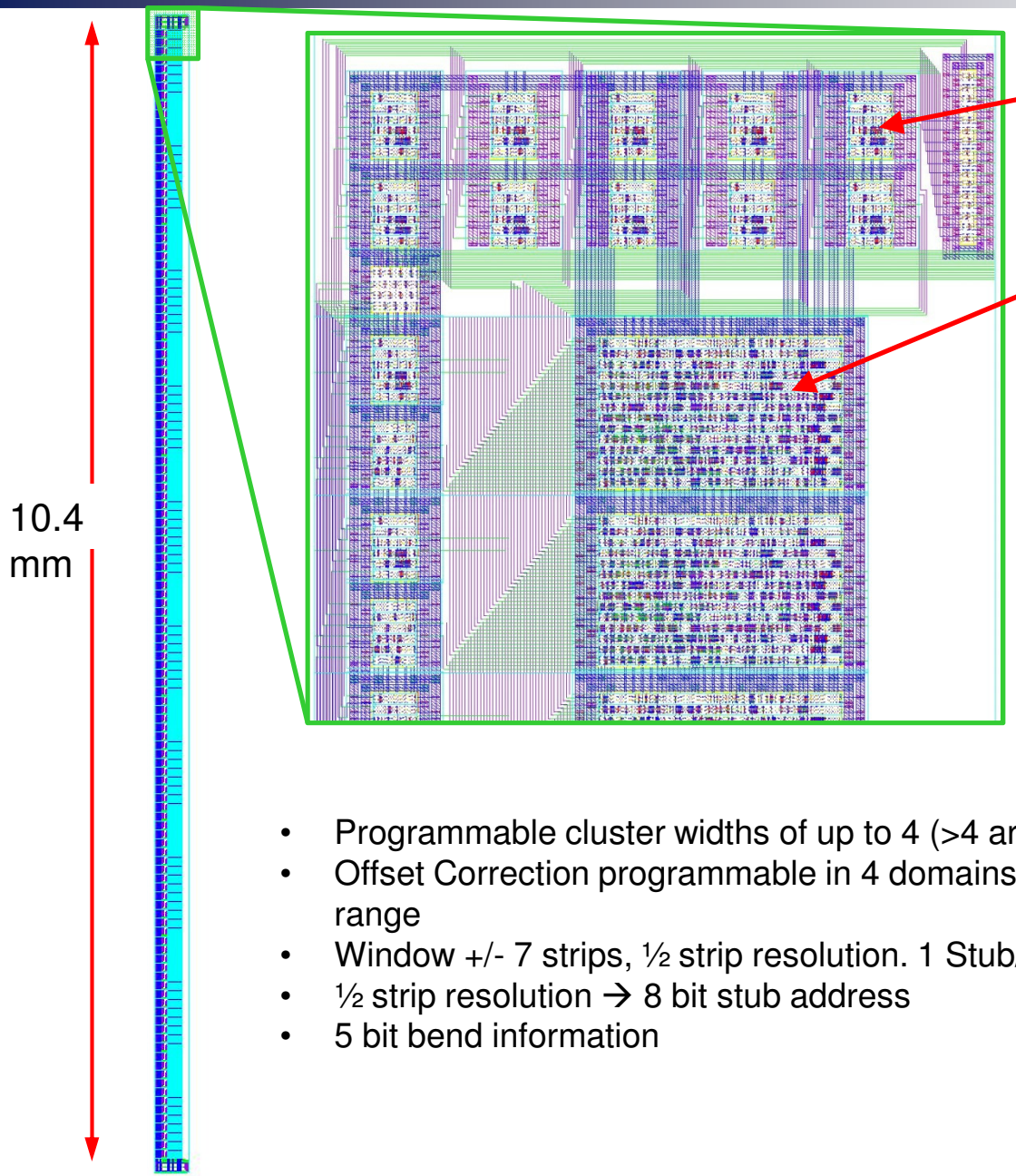
extra

(Mark Prydderch's slides from Tracker week talk)

CBC3 Architecture

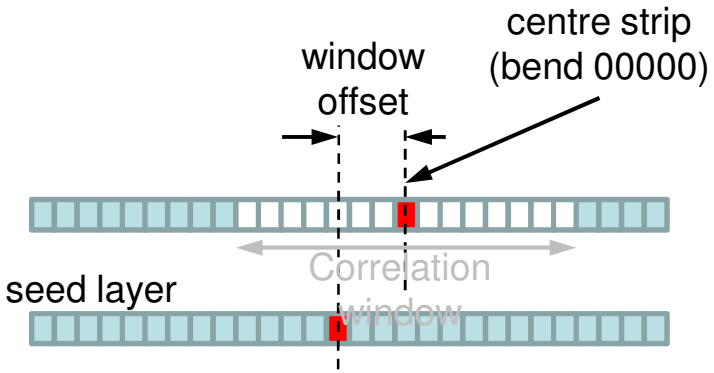


Stub Logic



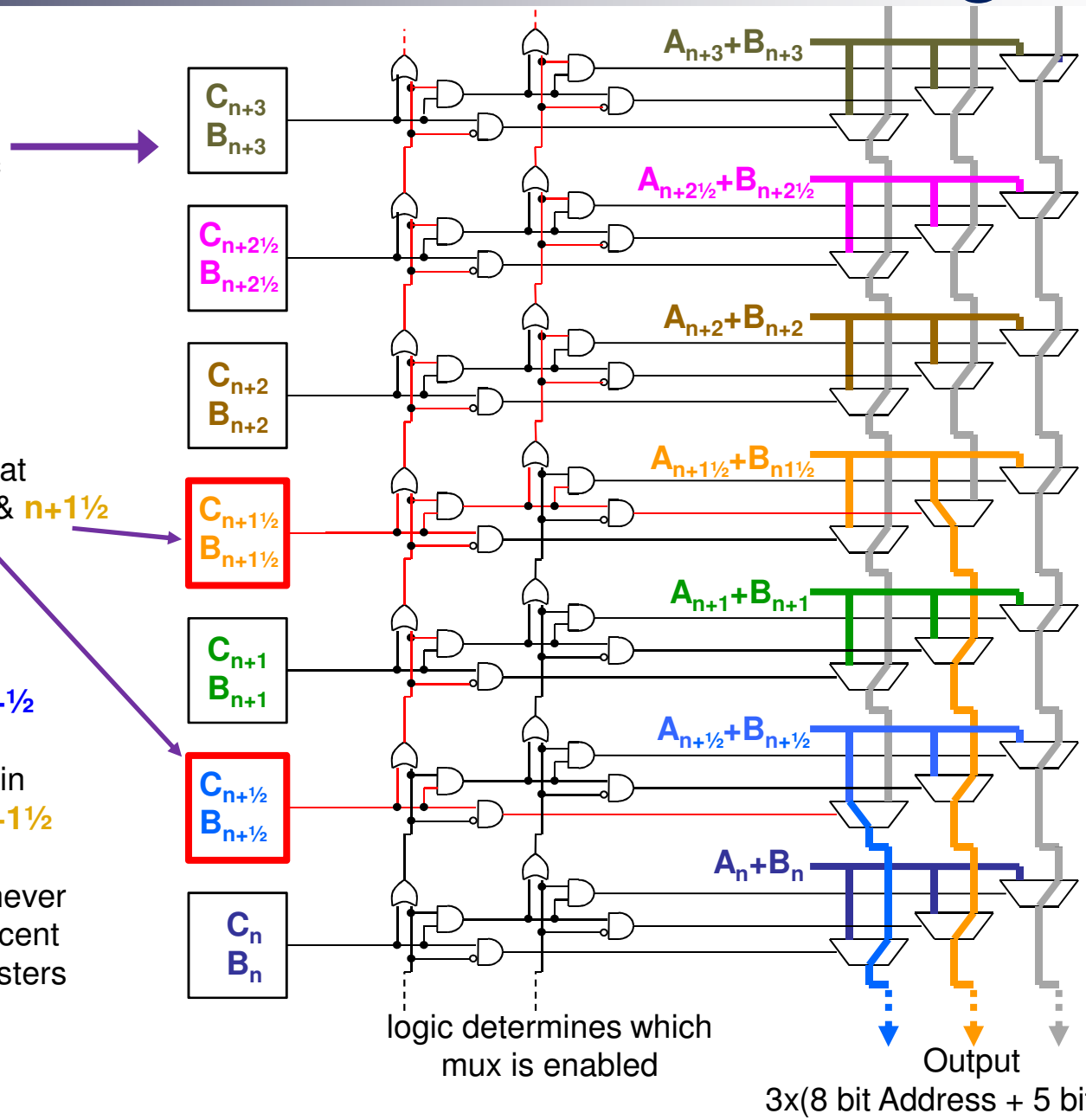
CWD Logic for off chip Neighbours

Offset Correction, Correlation and Bend Logic



- Programmable cluster widths of up to 4 (>4 are rejected)
- Offset Correction programmable in 4 domains across chip with +/- 3 strips adjustment range
- Window +/- 7 strips, ½ strip resolution. 1 Stub/window (highest Pt)
- ½ strip resolution → 8 bit stub address
- 5 bit bend information

CBC3 Stub Gathering Logic



Example:

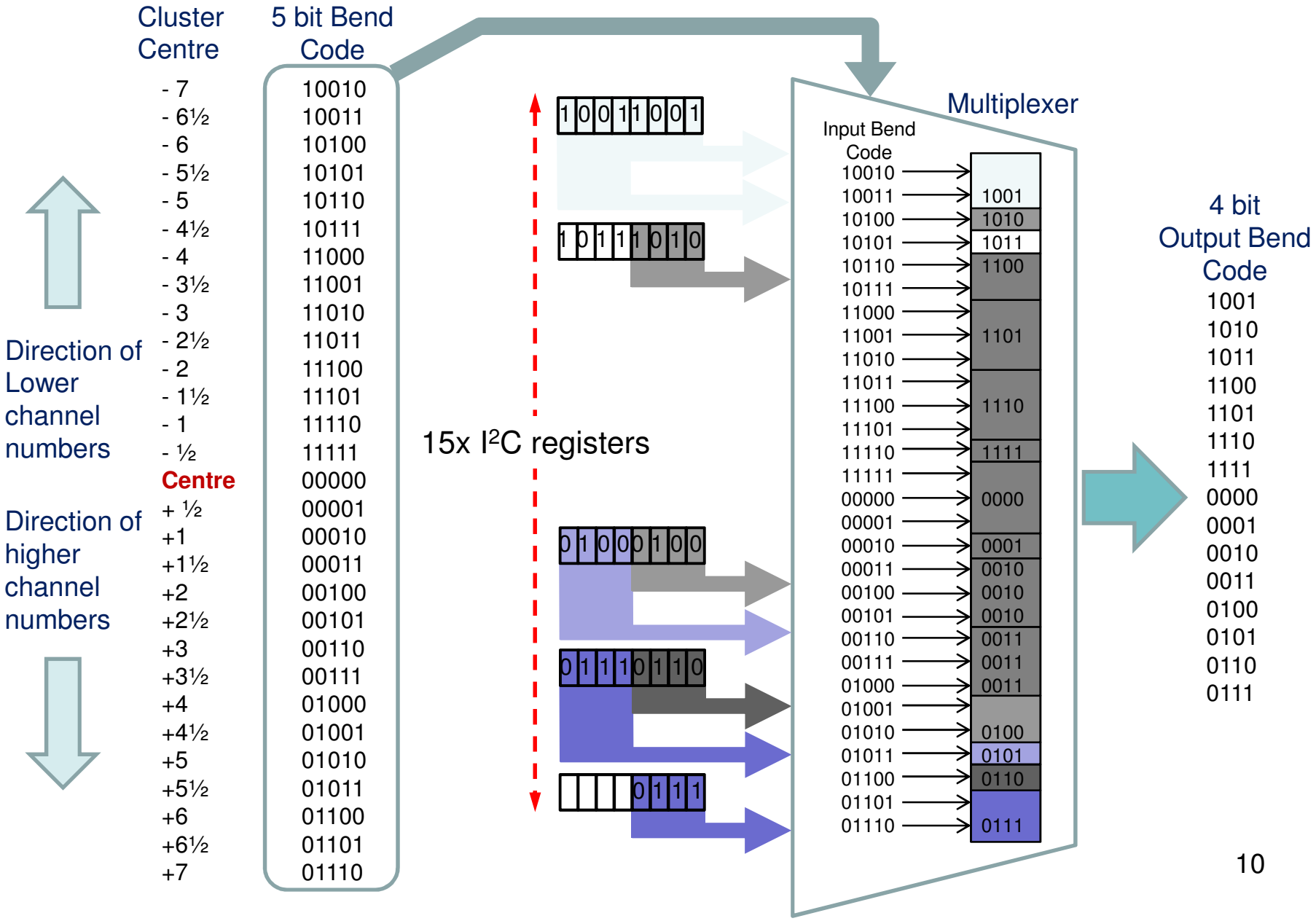
2 positive correlations at cluster locations **n+½** & **n+1½**

Left multiplexer chain activated for cluster **n+½**

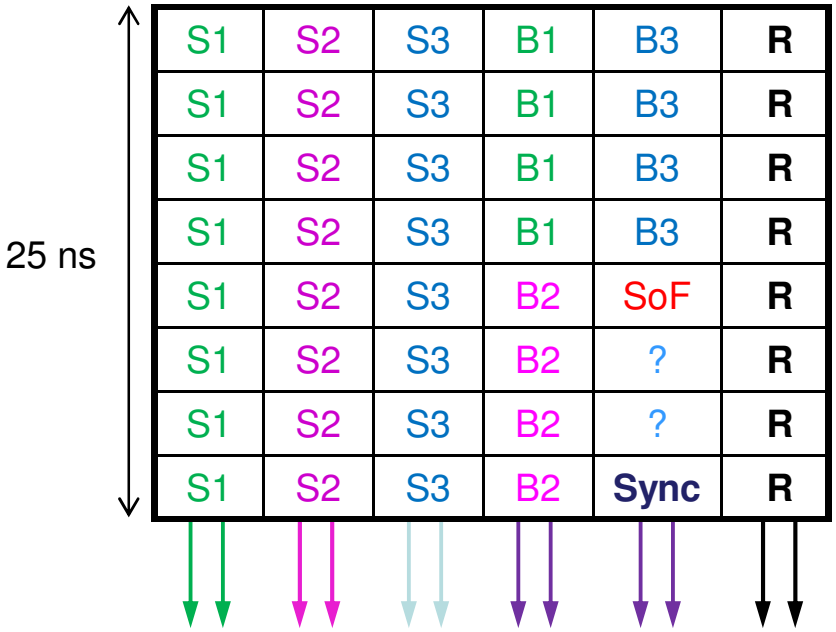
Middle multiplexer chain activated for cluster **n+1½**

Note: CWD logic will never pass immediately adjacent clusters (i.e. active clusters on n and n+½ are not possible)

CBC3 Bend Look-Up Table



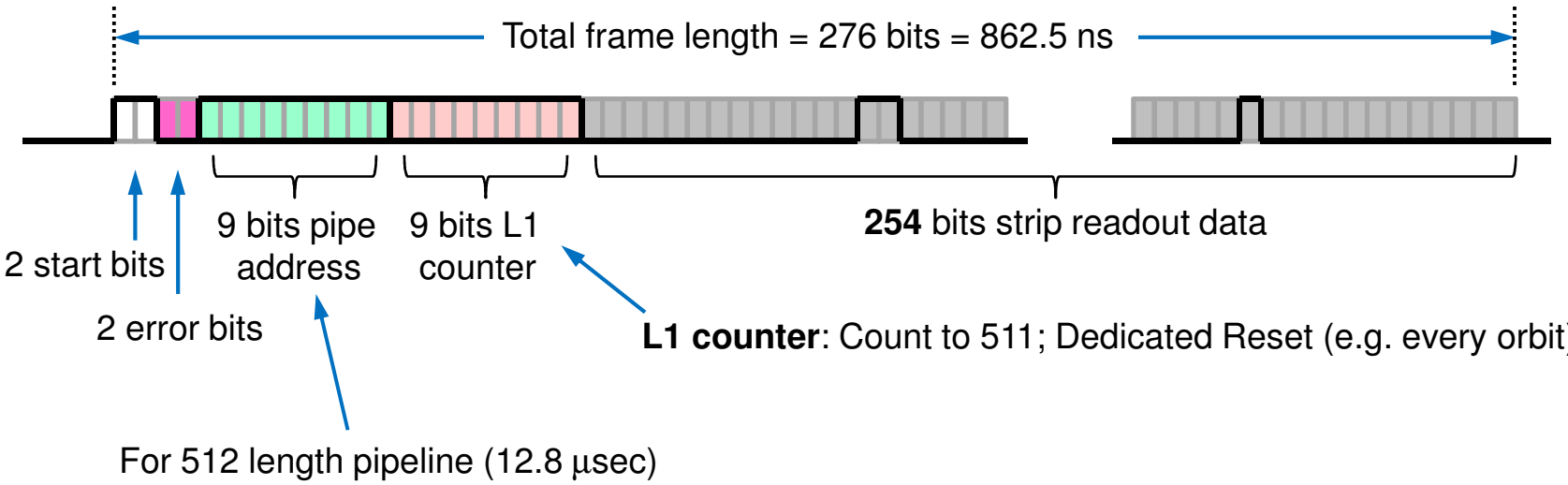
CBC3 Data Readout



S = Cluster address (½ strip resolution)
B = Bend data
SoF = Stub Overflow (>3 Stubs)
? = Spare/To be defined
Sync = For synchronisation with CC
R = Triggered readout data
(remains unsparsified)

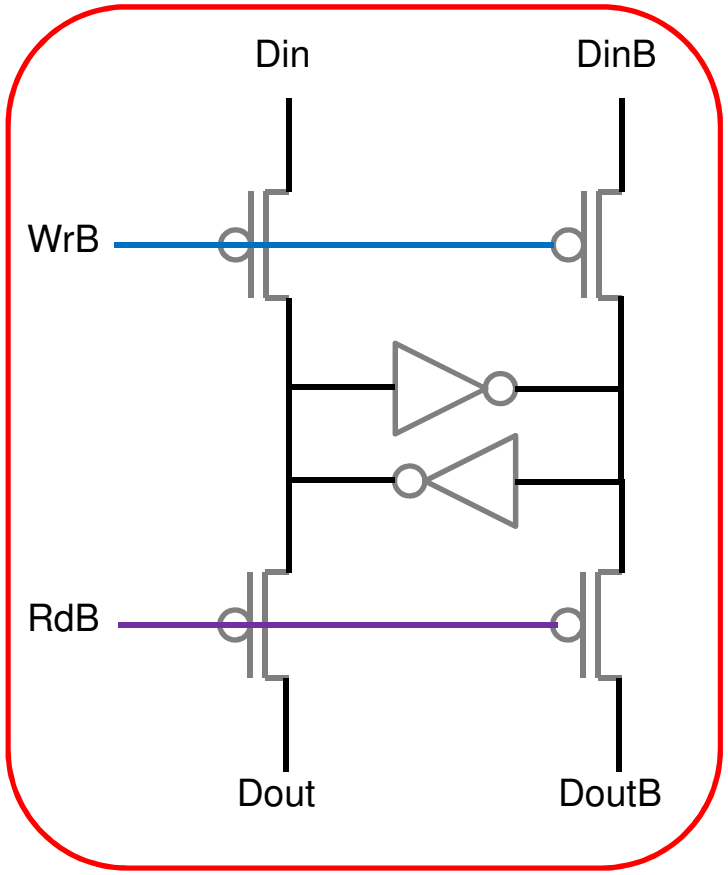
Six differential (SLVS) outputs running at 320 Mbps

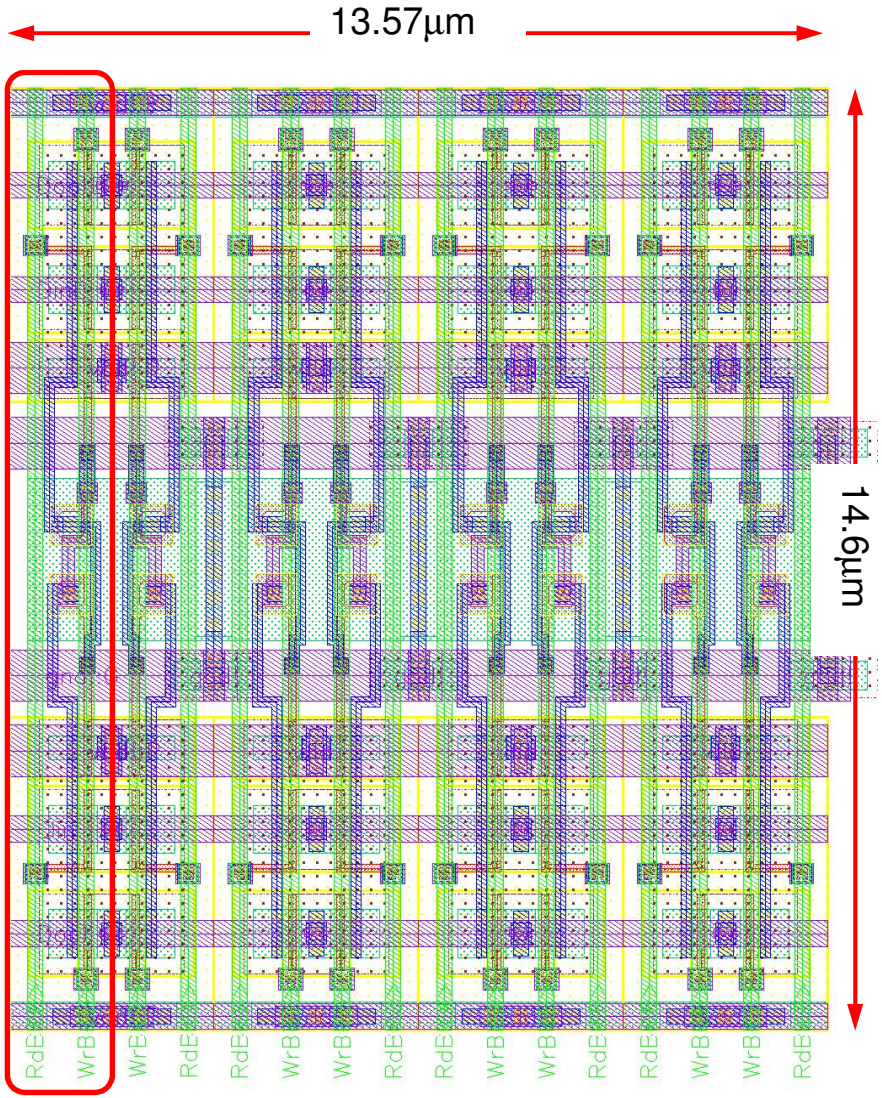
CBC3 Triggered Data Format



NOTE: Existing buffer length of 32 is sufficient for very low inefficiency at 1 MHz rate

CBC3 SRAM





Layout of 8 SRAM cells

Miscellaneous

Fast Command Interface: Fast Reset, Trigger, Test Pulse Trigger, L1 Counter Reset

Biases: VCTH to be monotonic & 1 mV resolution (10 bit); Modify IREF so that Ibias is related to GND rather than VDDA.

I2C register SEU immunity: Modify registers to improve immunity

Clock domains: DLL with programmable tap off for all of 40 MHz domain

Powering: 1.2V VDDD +/- 10%; no switched cap DC-DC; LDO modified to cope with minimum VDD

40MHz Test Mode: To allow testing at 40MHz on Wafer Prober

Pad Pitch: As for CBC2