CBC3 design progress

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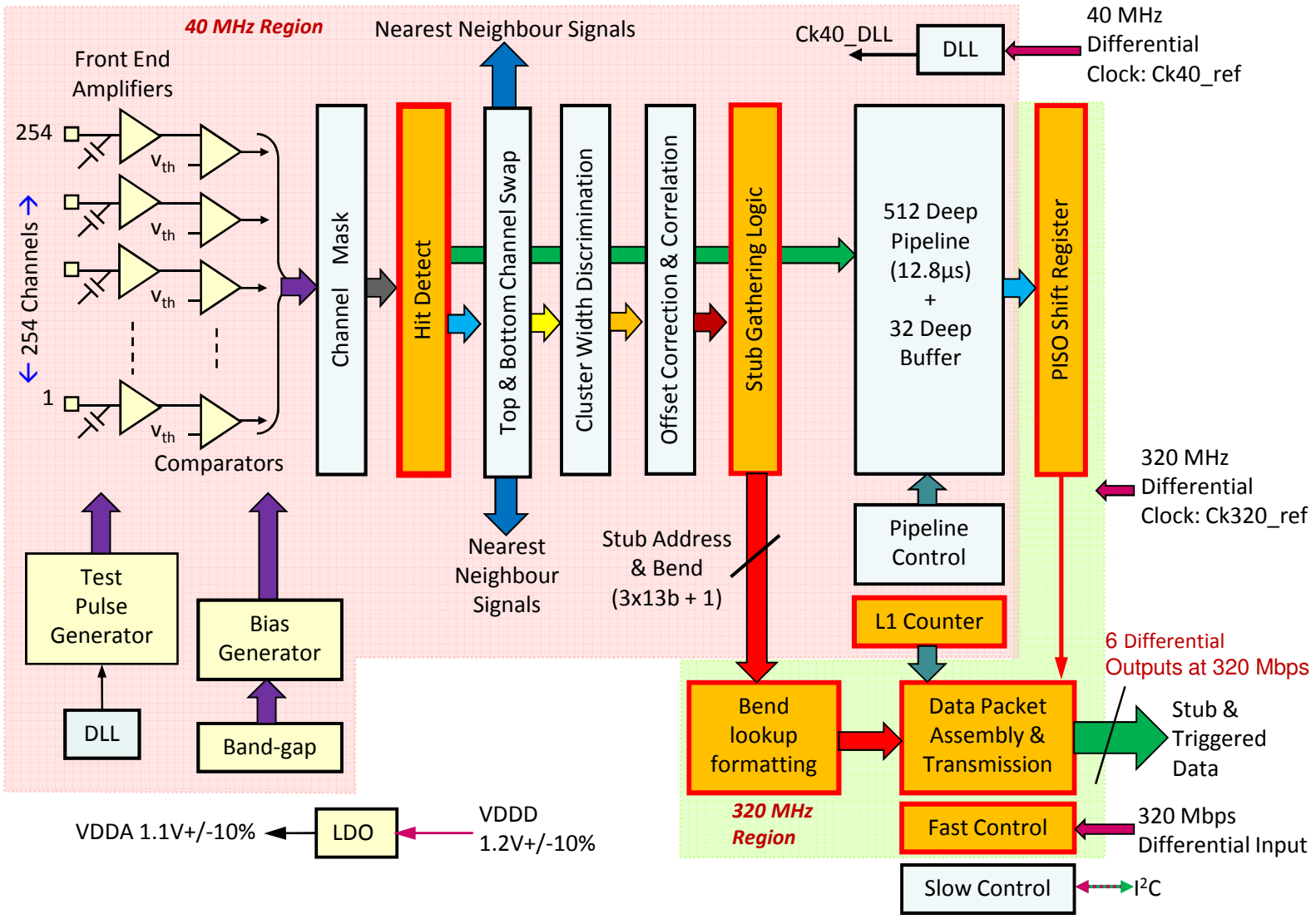
CBC3 progress review at RAL last week
- progress with digital circuits
- progress with front end

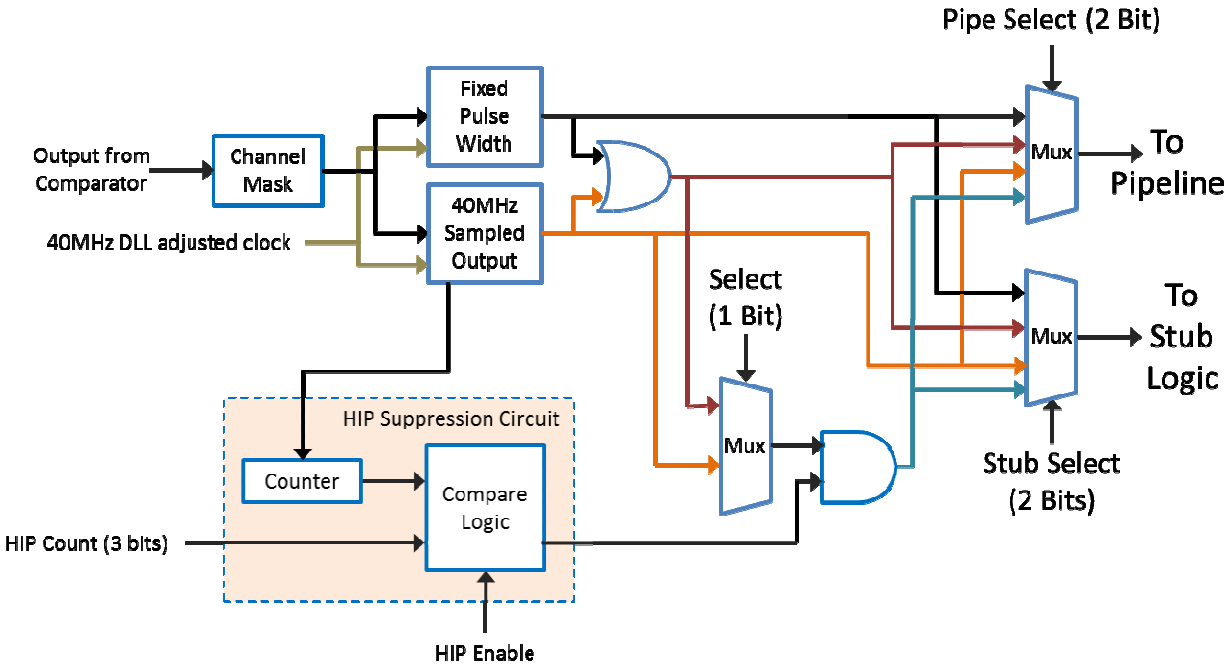
some open questions for discussion

systems meeting, 22nd July, 2015.

CBC3 digital design progress

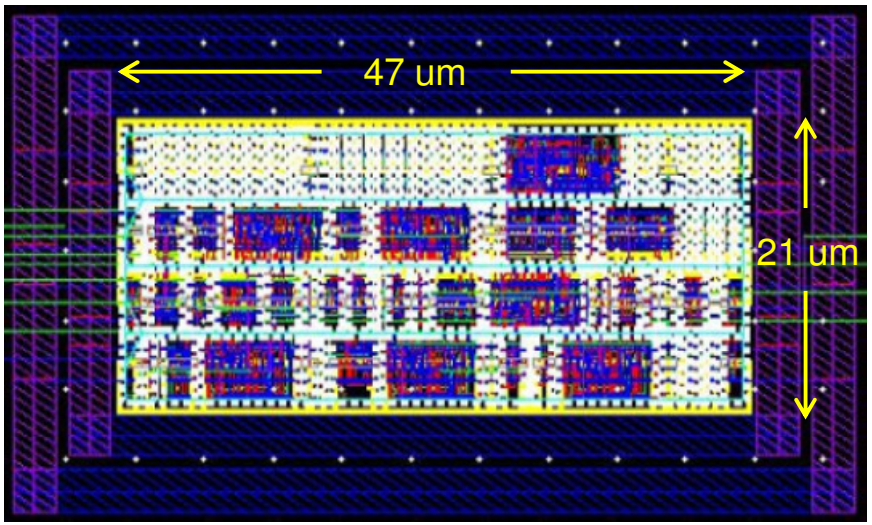


Hit Detect

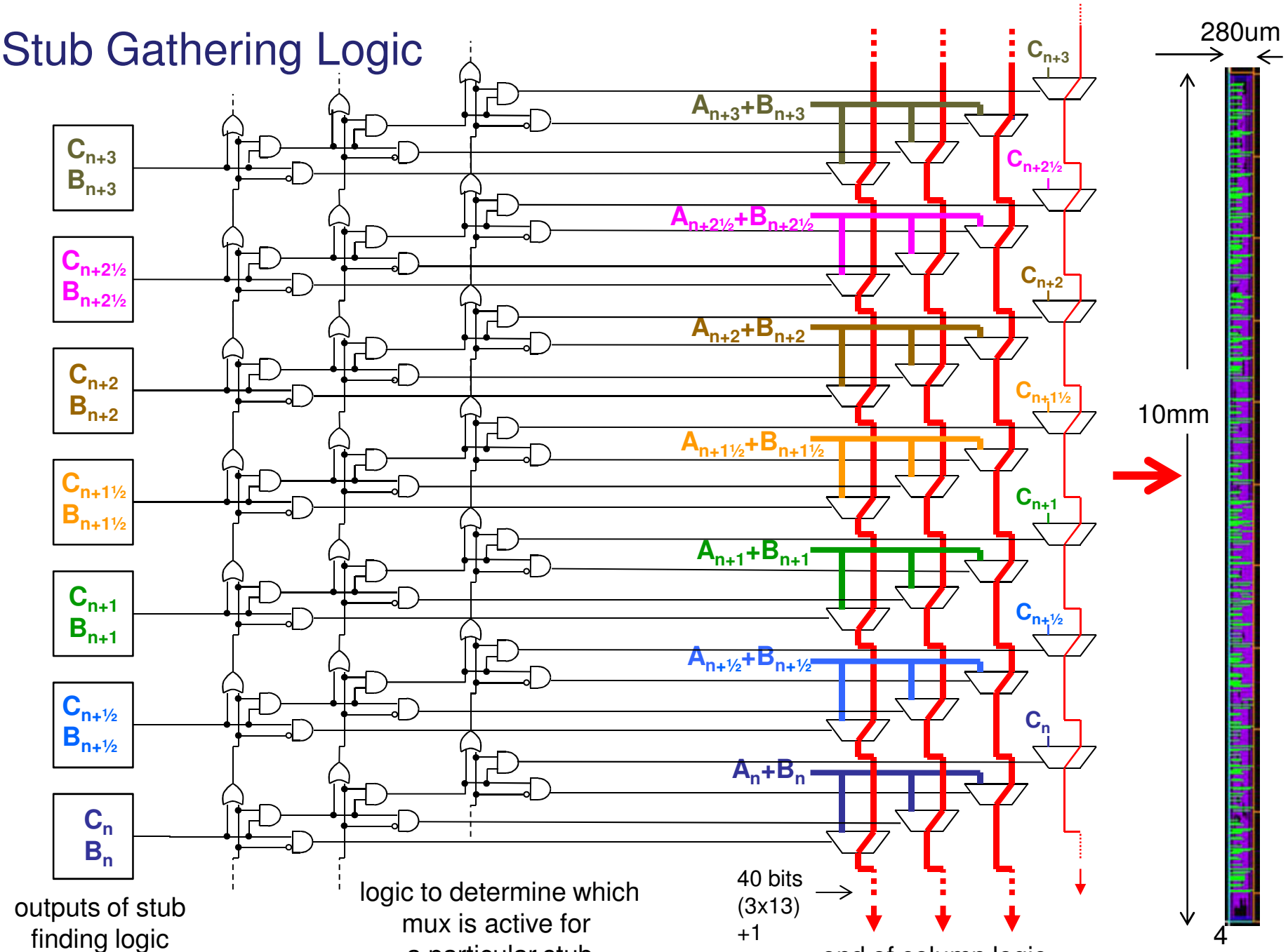


functionality previously discussed:
http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3 Progress_Apr_15 .pdf

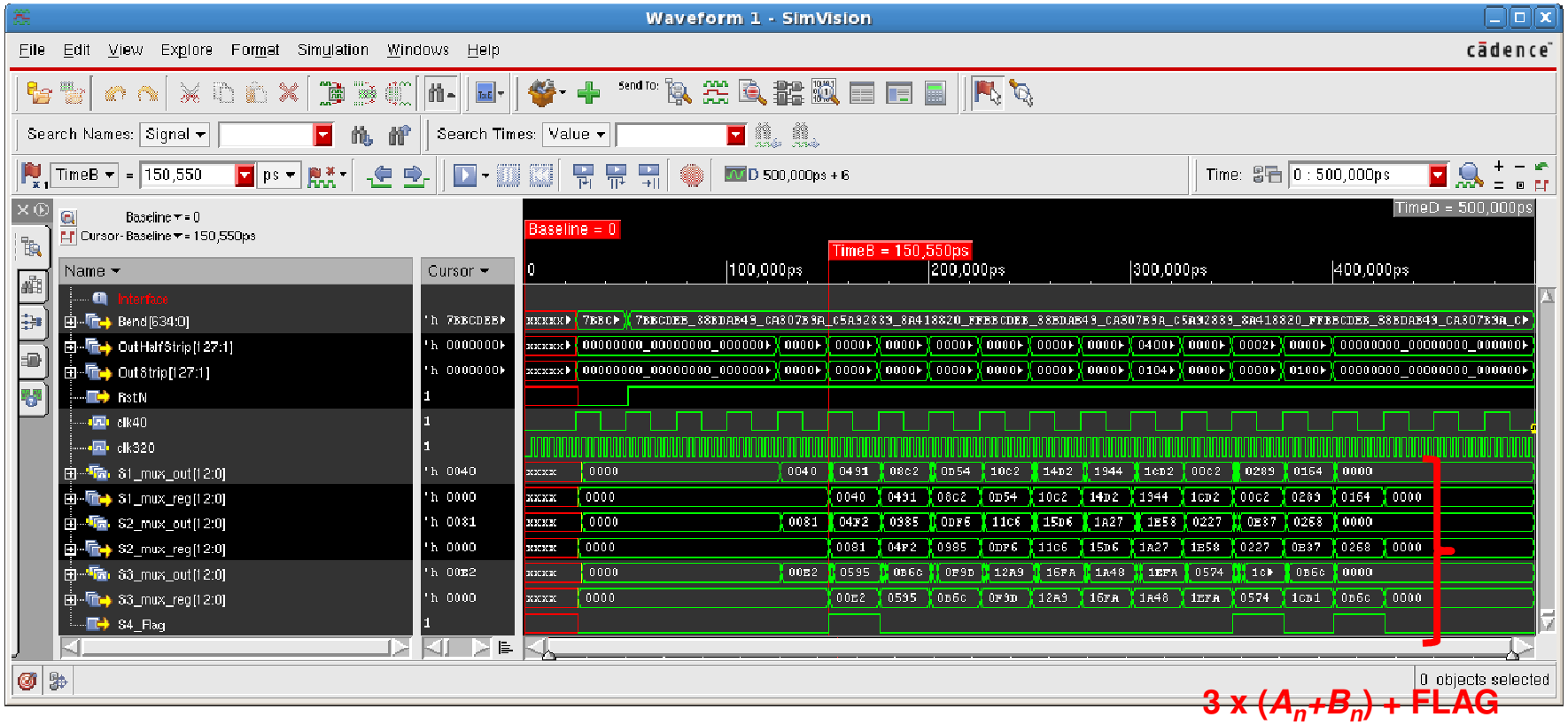
simulations and layout now complete



Stub Gathering Logic



Stub Gathering Logic

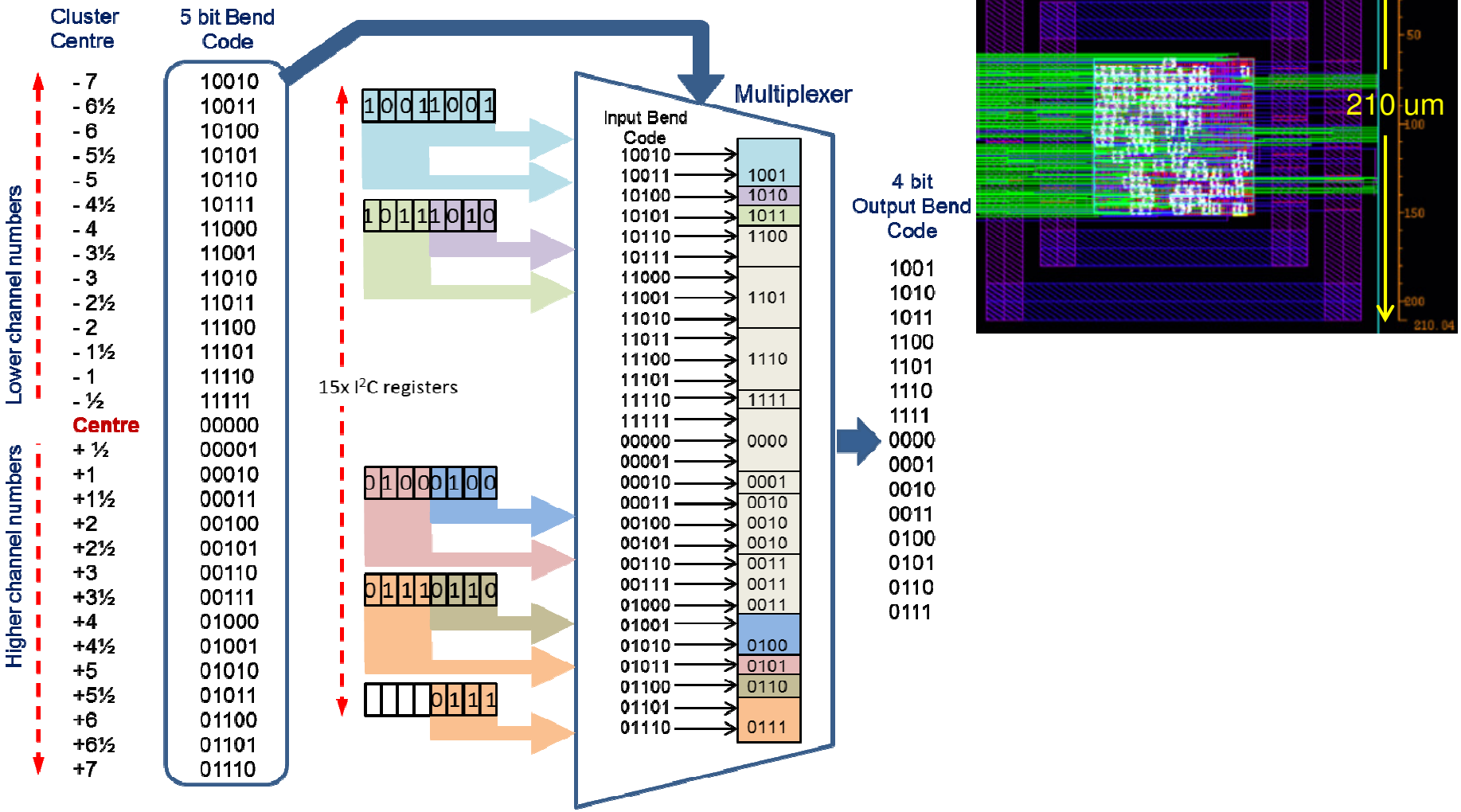


post layout simulation passed well within max propagation allowed delay of 10.5 nsec

fast/typical/slow corners, 1.2+/-0.1V, -55/25/+125 deg.C ← simulation conditions used throughout

some further simulations of situations likely to produce worst case propagation delays planned

Bend Lookup Table

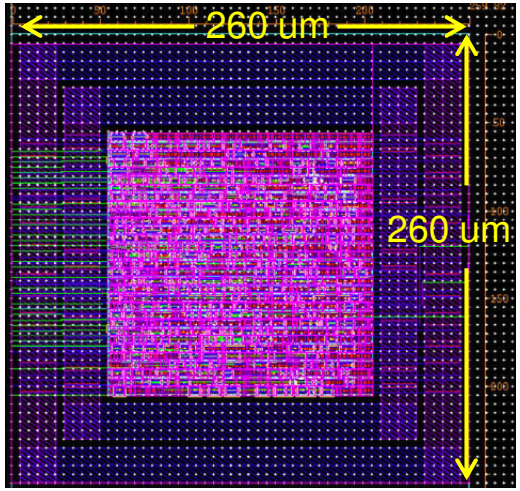


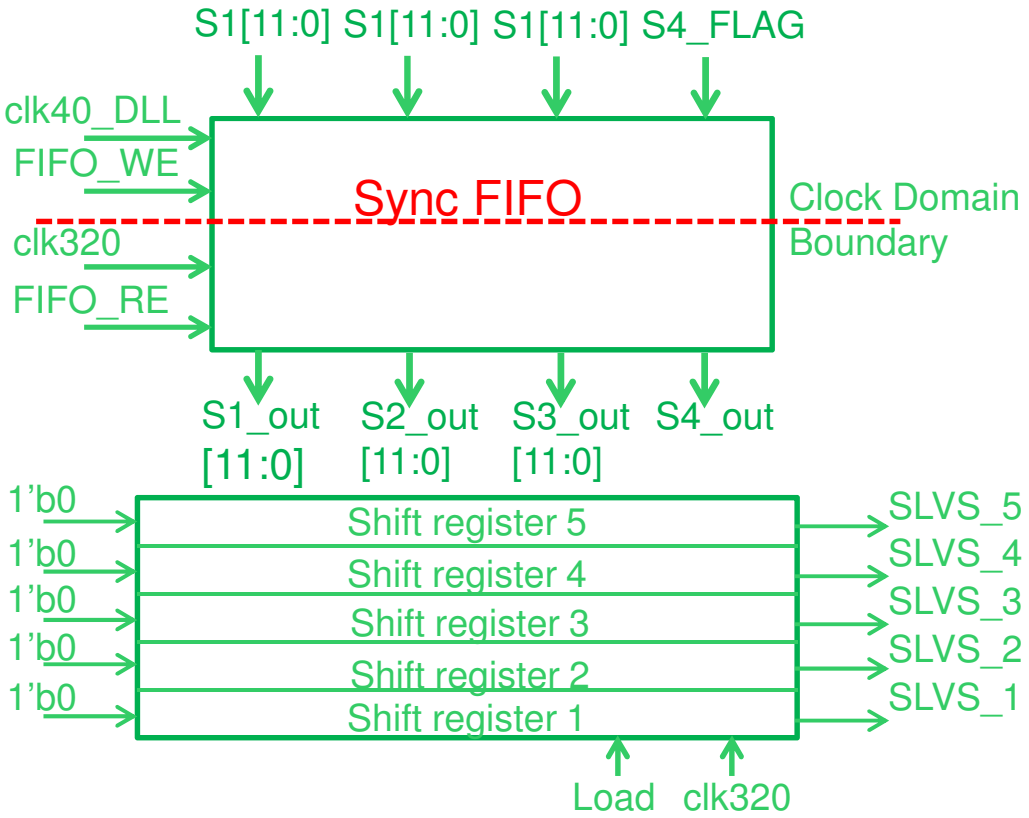
15 I2C registers needed to contain mapping (each reg. contains two 4-bit bend codes)
post layout simulation passed

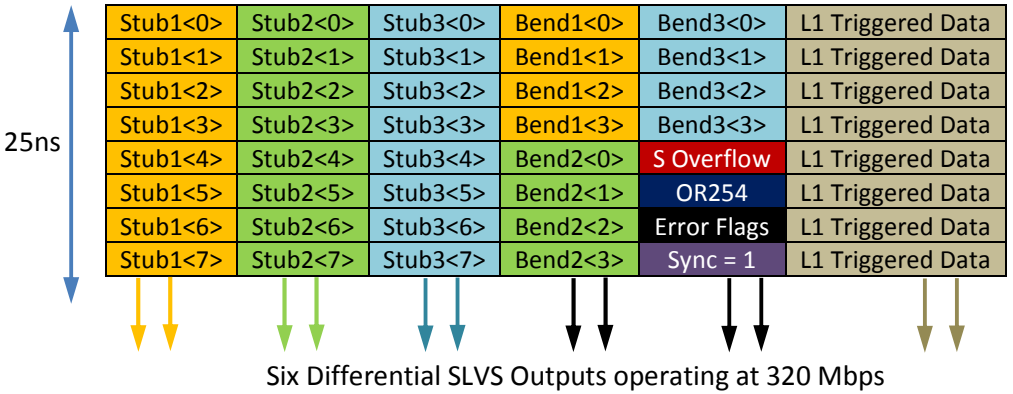
Data Packet Assembly & Transmission

FIFO implements clock domain crossing

control logic triplicated







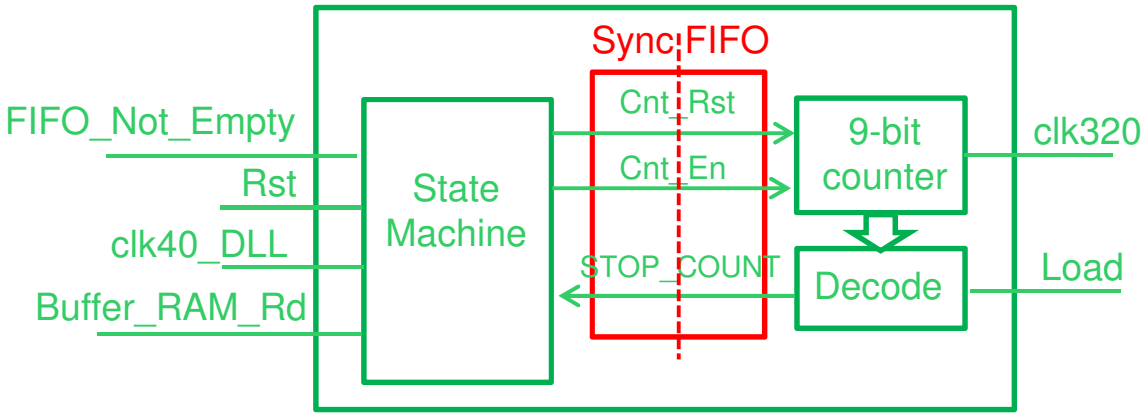
post layout simulation passed

6ps rms jitter on 320 and 40 MHz reference clocks - elink spec.

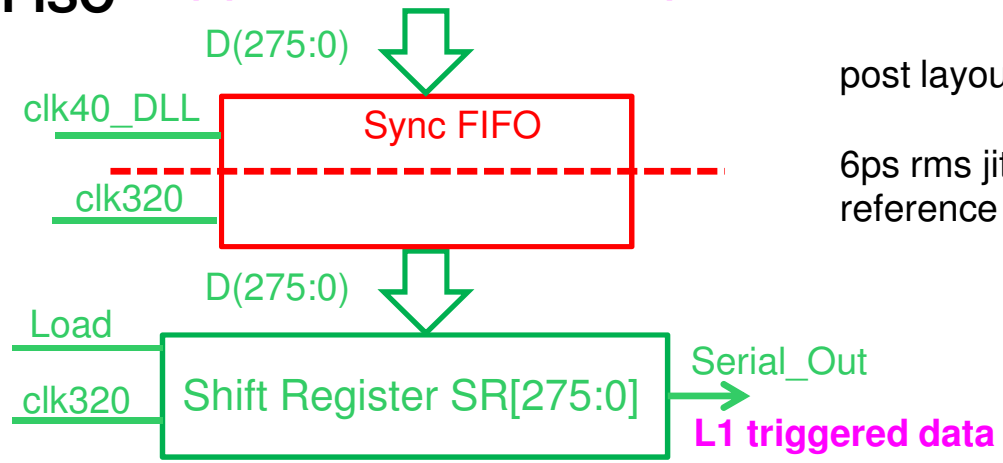
PISO shift register

more clock domain crossings required for triggered readout data from buffer ram locations

control logic (triplicated)

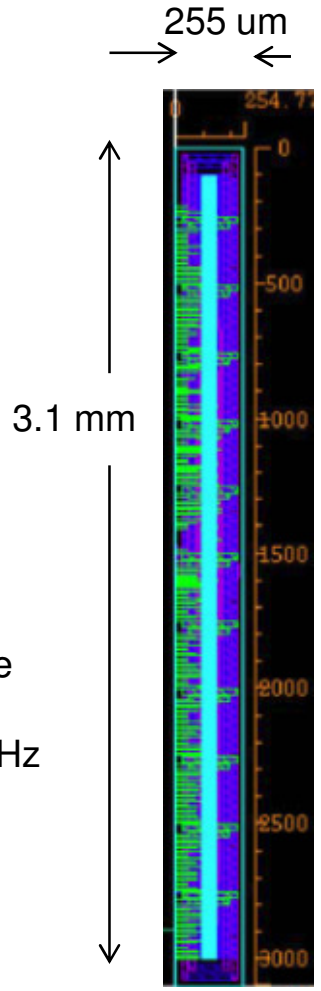


PISO **pipeline buffer ram (32 deep)**



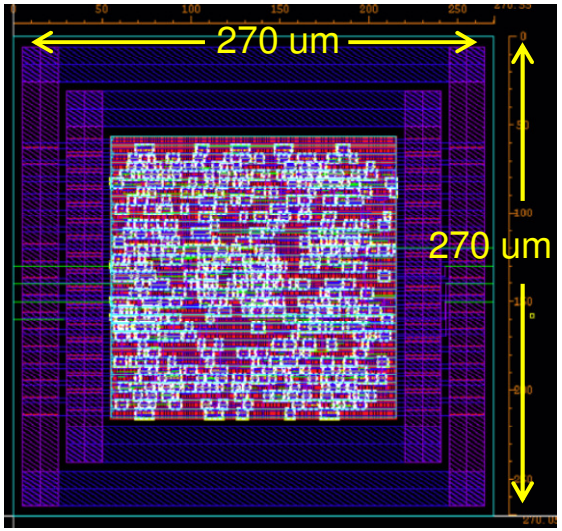
post layout simulation complete

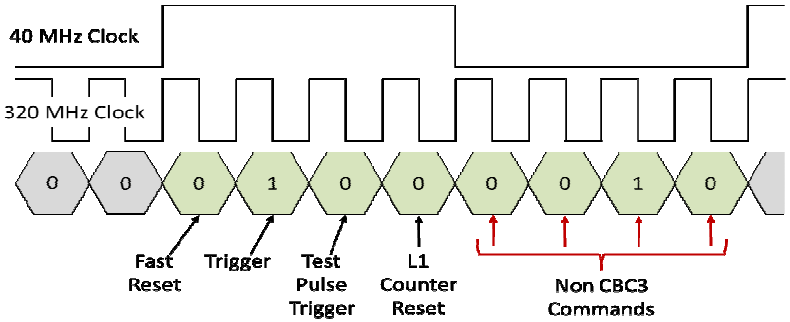
6ps rms jitter on 320 and 40 MHz reference clocks

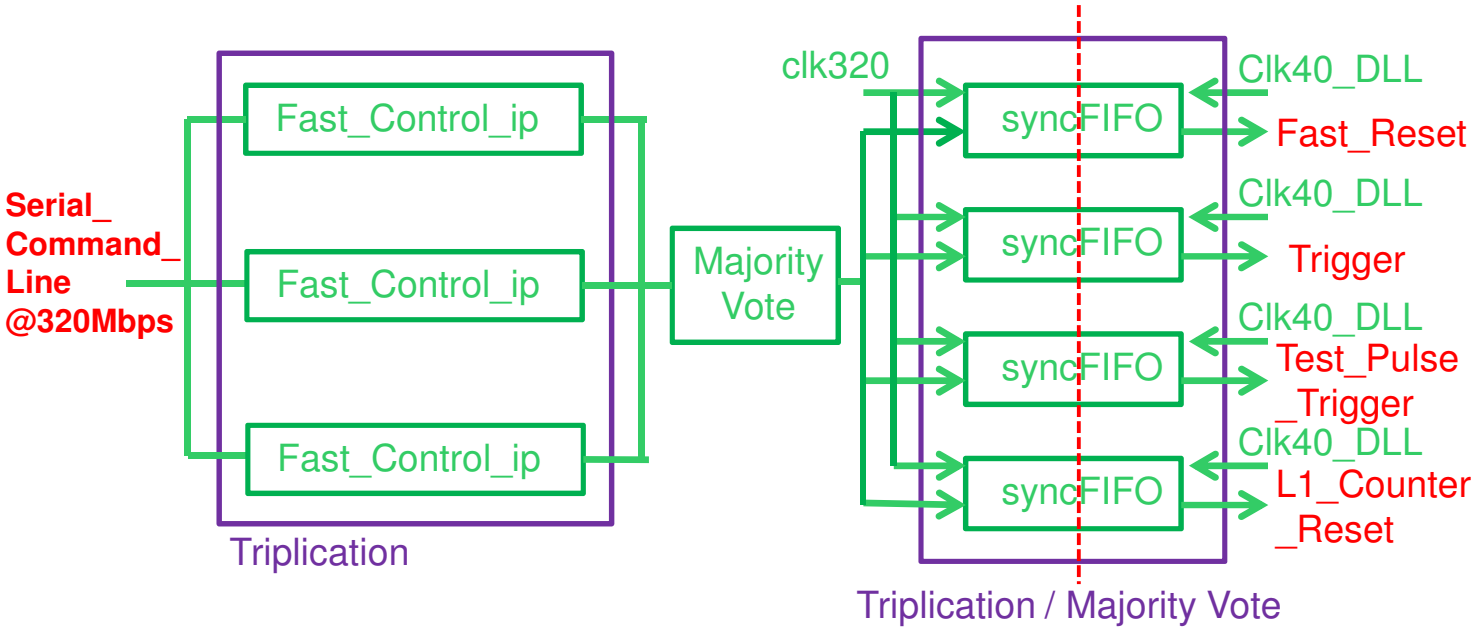


Fast Control Interface

fast control signals must be decoded and also cross clock domains
triplication for SEU
post layout simulation complete
Ck40_DLL delay varied over full range (0 -> 24 nsec)
6ps rms jitter on 320 and 40 MHz reference clocks

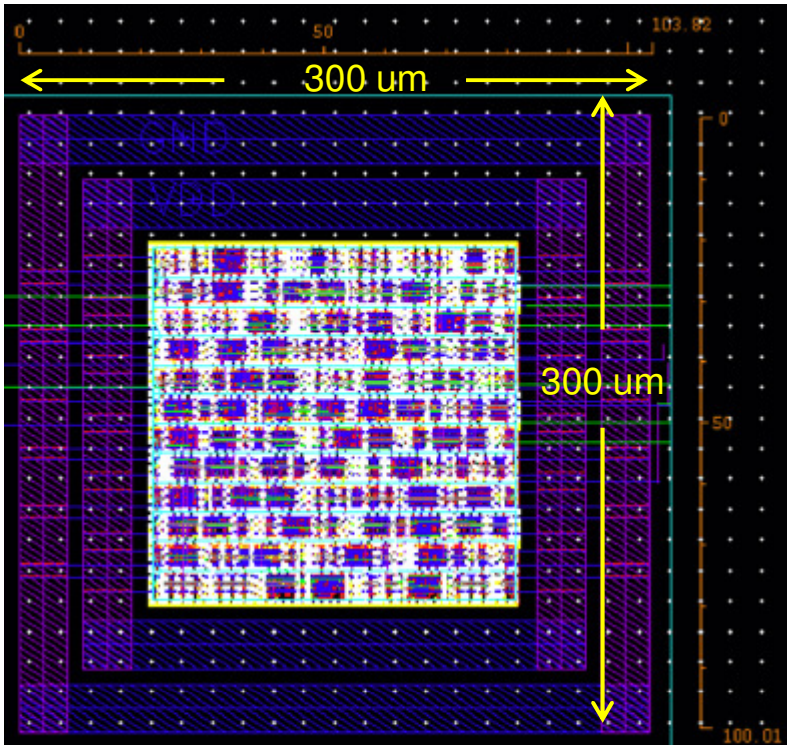


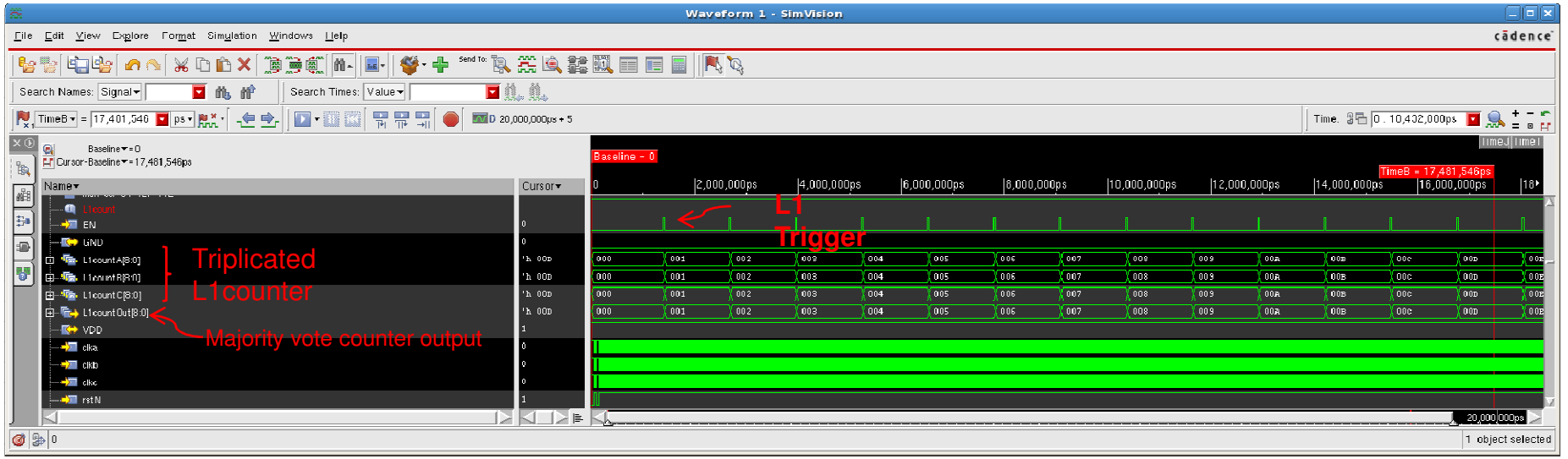




L1 counter

triplicated 9-bit counter running in Ck40_DLL domain
post-layout simulation passed





digital power

Block	Power Dissipation (mW)	Maximum Track Length* (um)	Track Width (um)	Maximum IR Drop (mV)
Stub Gathering Logic	4.25	10345	20	29.3
L1count	3.77x10-2	100	10	5.02x10-3
SAT_FIFO_SLVS_1_5	0.237	260	20	4.73x10-2
SAT_FIFO_SLVS_6	0.9405	3100	20	1.9
Fast Control	0.287	270	20	5.16x10-2
Hit Detect	6.86x10-2	63	3	1.91x10-2
Bend LUT	0.1874	210	20	1.12x10-2

no power concerns for any of digital blocks so far
more (worst case) power simulations planned

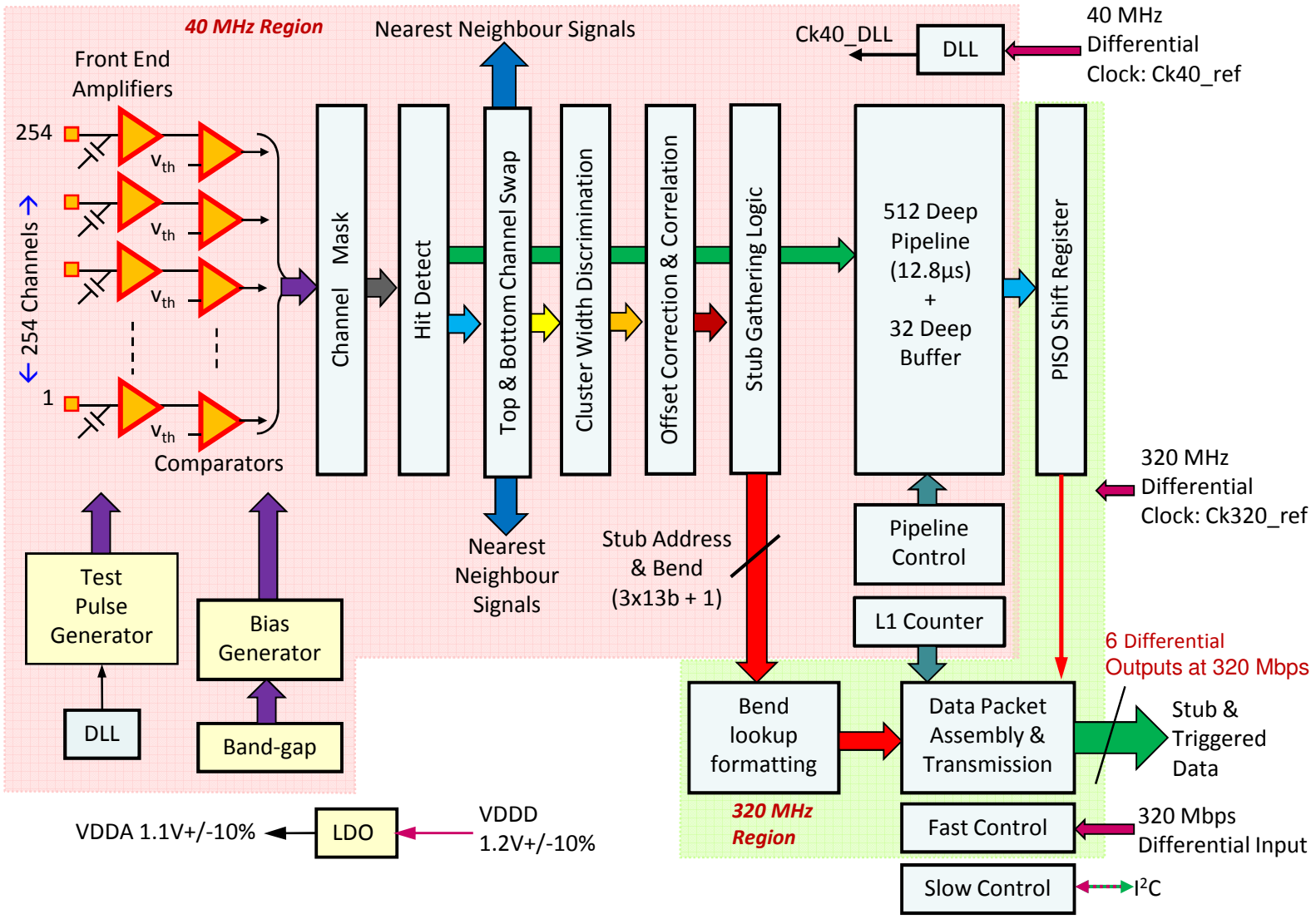
digital block progress summary

progress through to layout of all new (to CBC) blocks

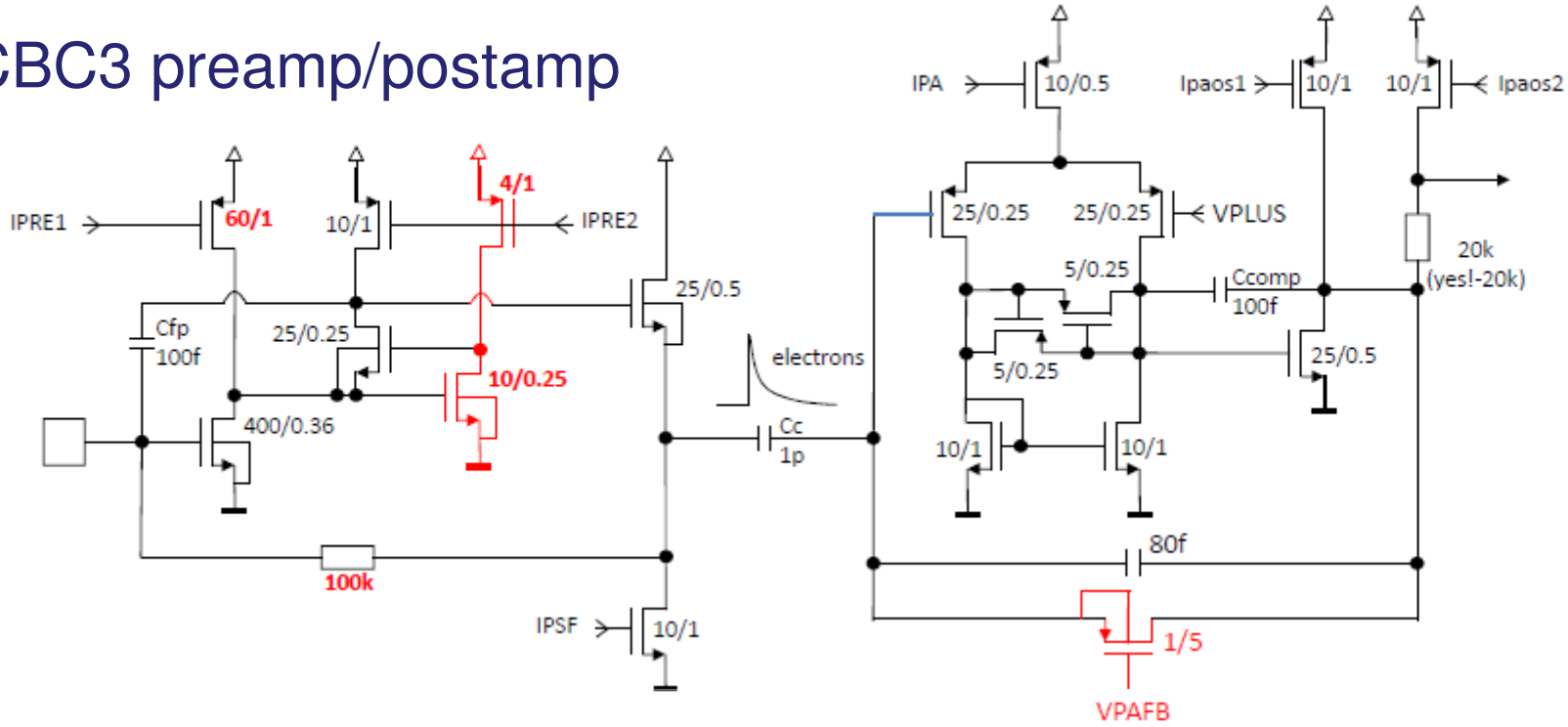
post layout simulations carried out

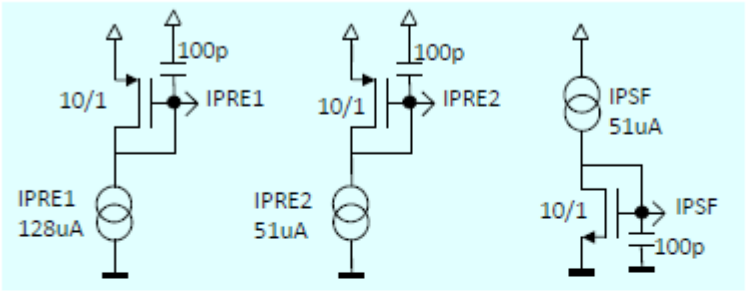
more simulation planned, anticipating worst case scenarios (rates and distributions of hits)

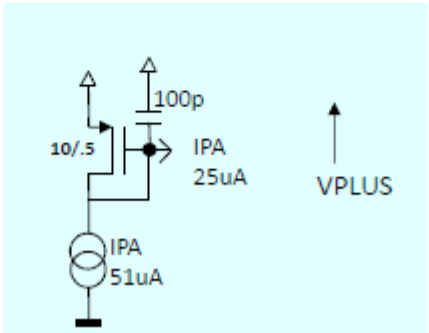
CBC3 front end progress

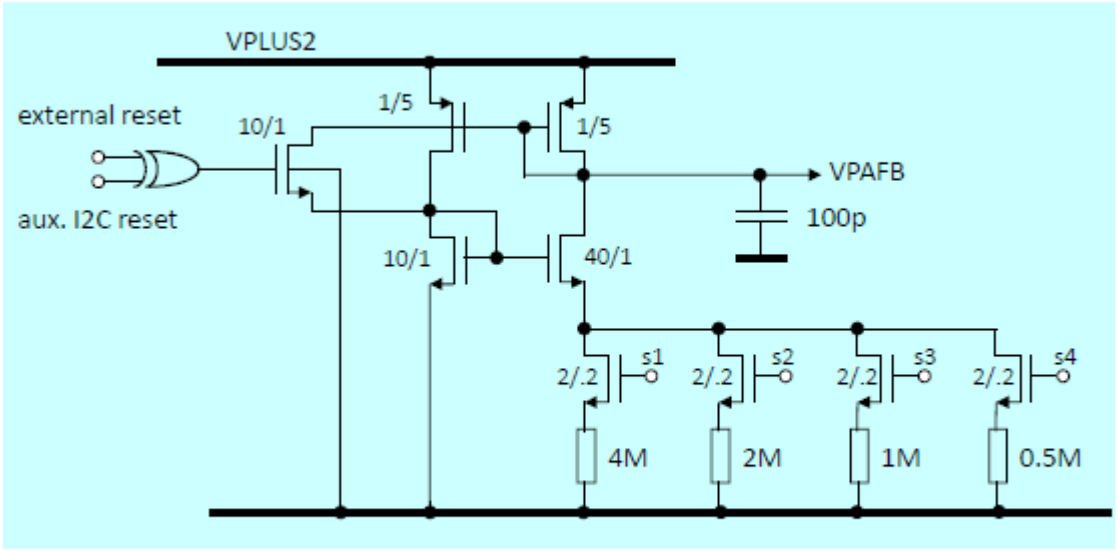


CBC3 preamp/postamp



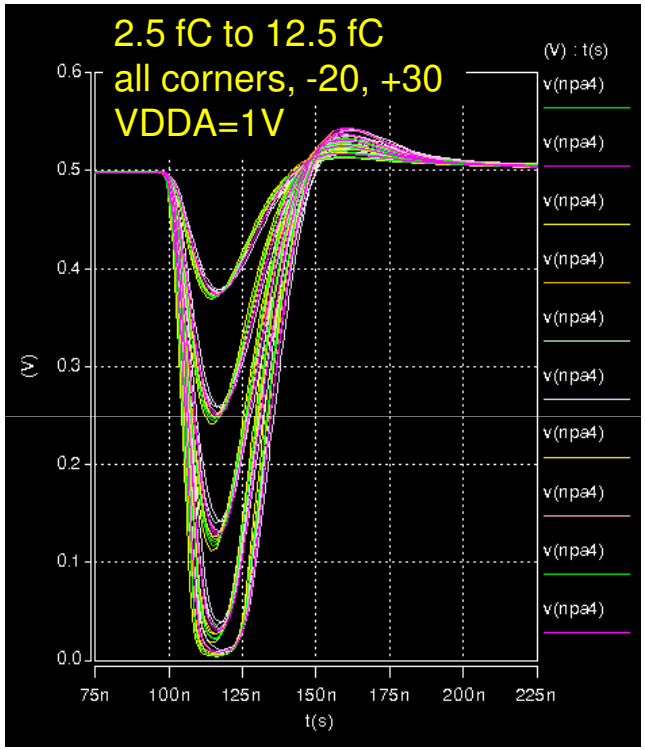


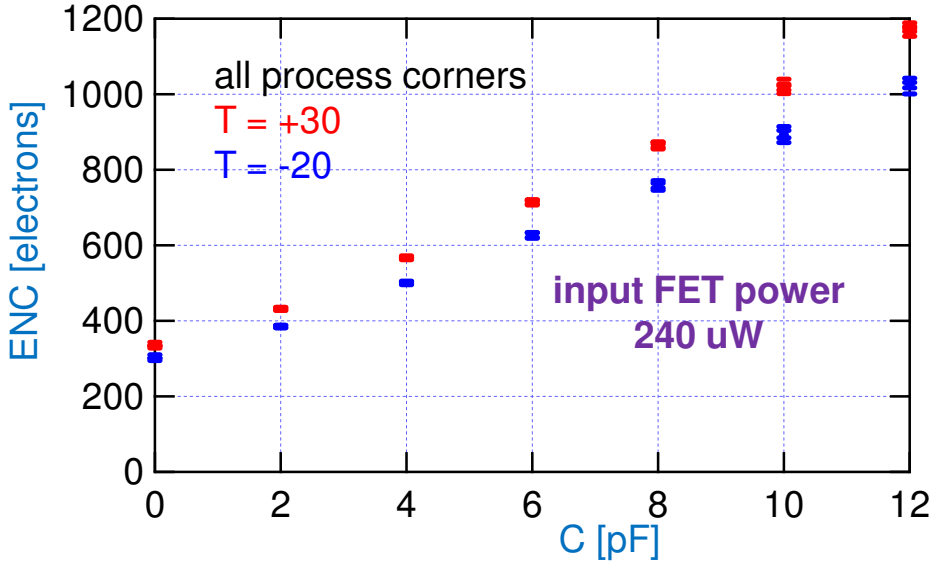


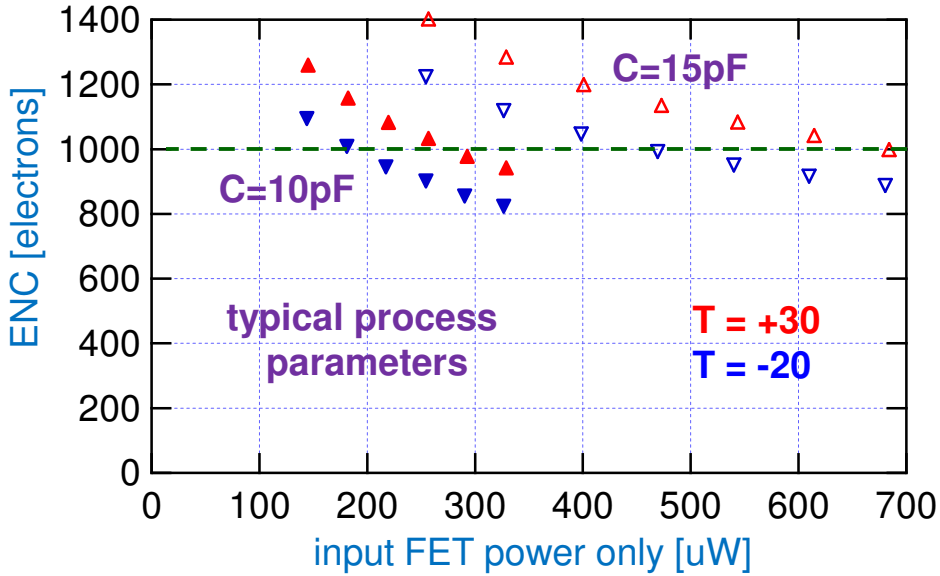


CBC3 front end progress

details of changes to preamp/postamp circuits and performance shown last time*



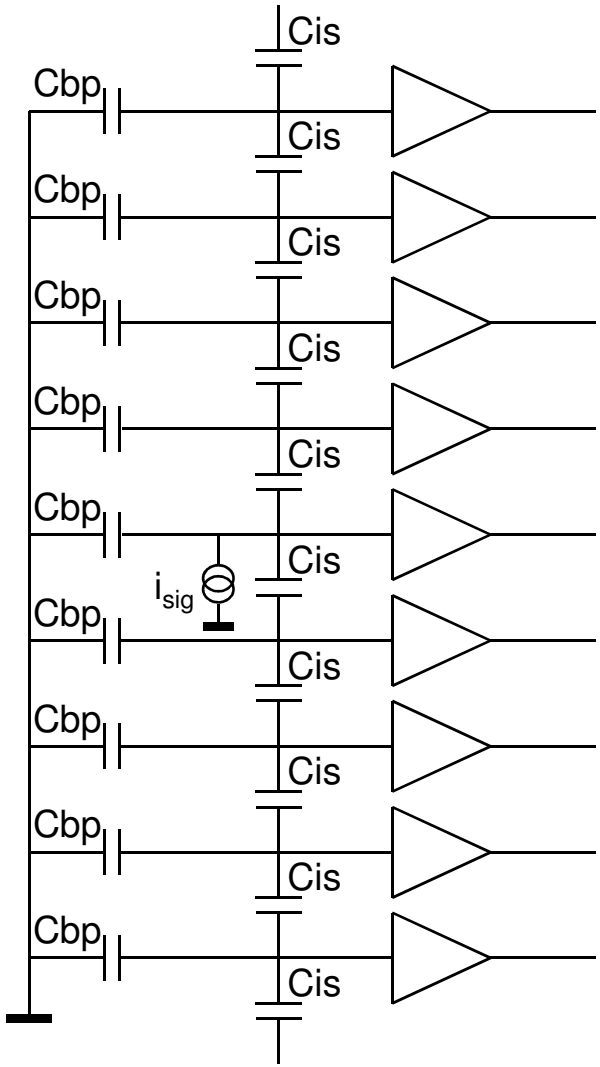




no time to present multi-channel and hips response simulations last time

* http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_FE_status_June2015.pdf

multi-channel behaviour

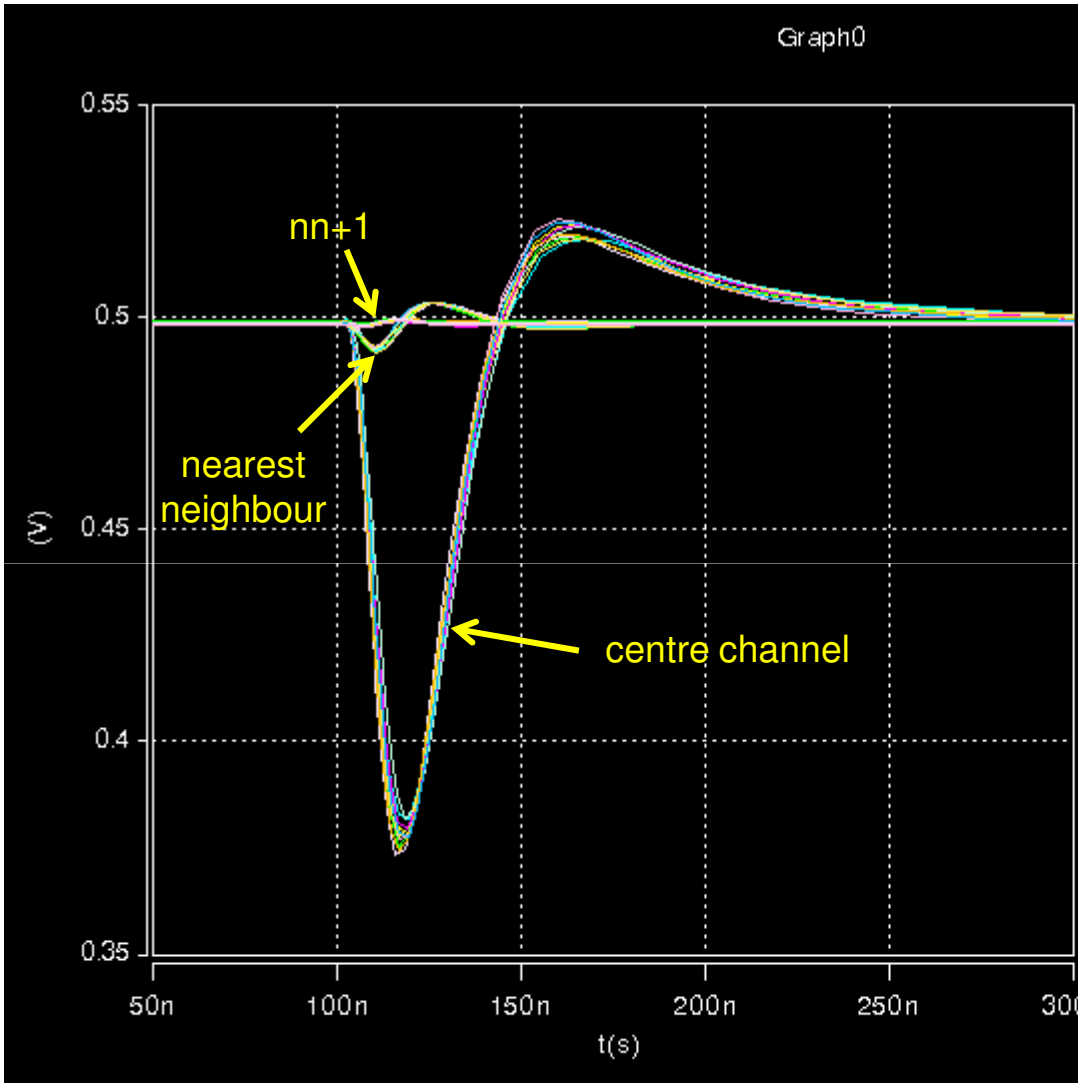


simulations here for Cis = 2.5pF, Cbp = 2pF, Cstray = 2pF
=> Ctot = 9 pF

inject charge into central channel

look at postamp output for
central channel
nearest neigbour,
nearest neighbour +1
….

interstrip crosstalk

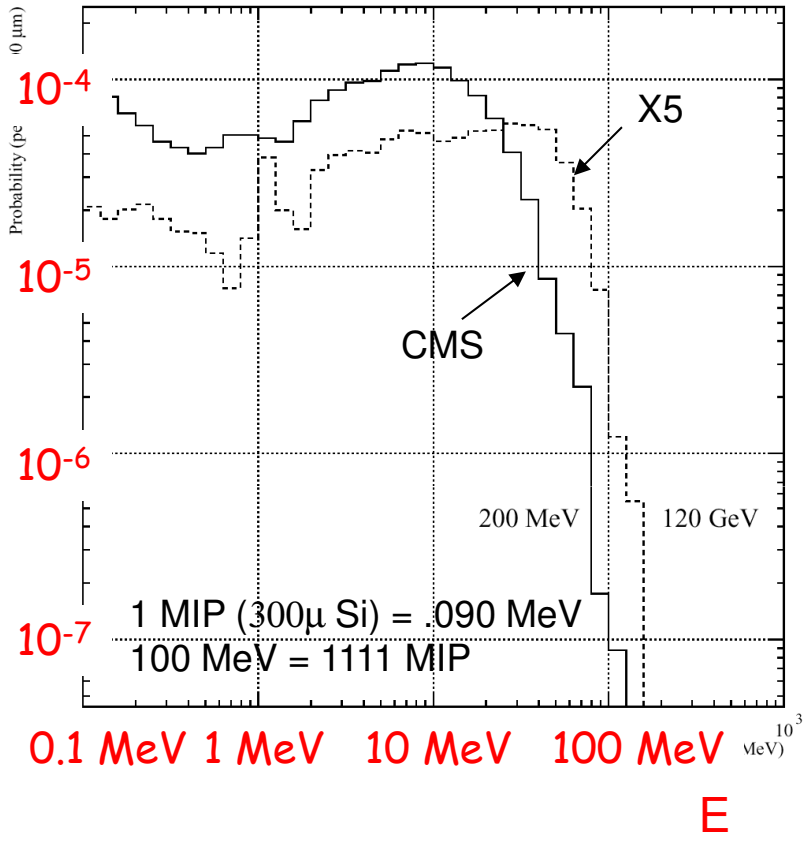


2.5 fC charge injected
T=-20/+30
all corners
nominal biases

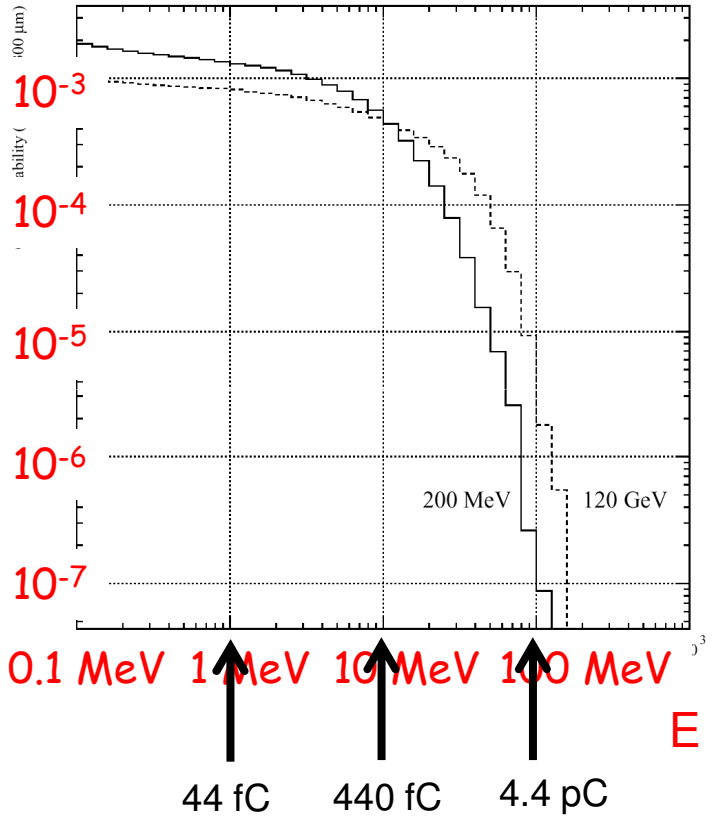
nearest neighbour peak
crosstalk ~ 5 %

now look at hips behaviour - M.Huhtinen simulations

Differential Energy spectrum: Probability/incident pion of depositing energy E in 300µm Si layer



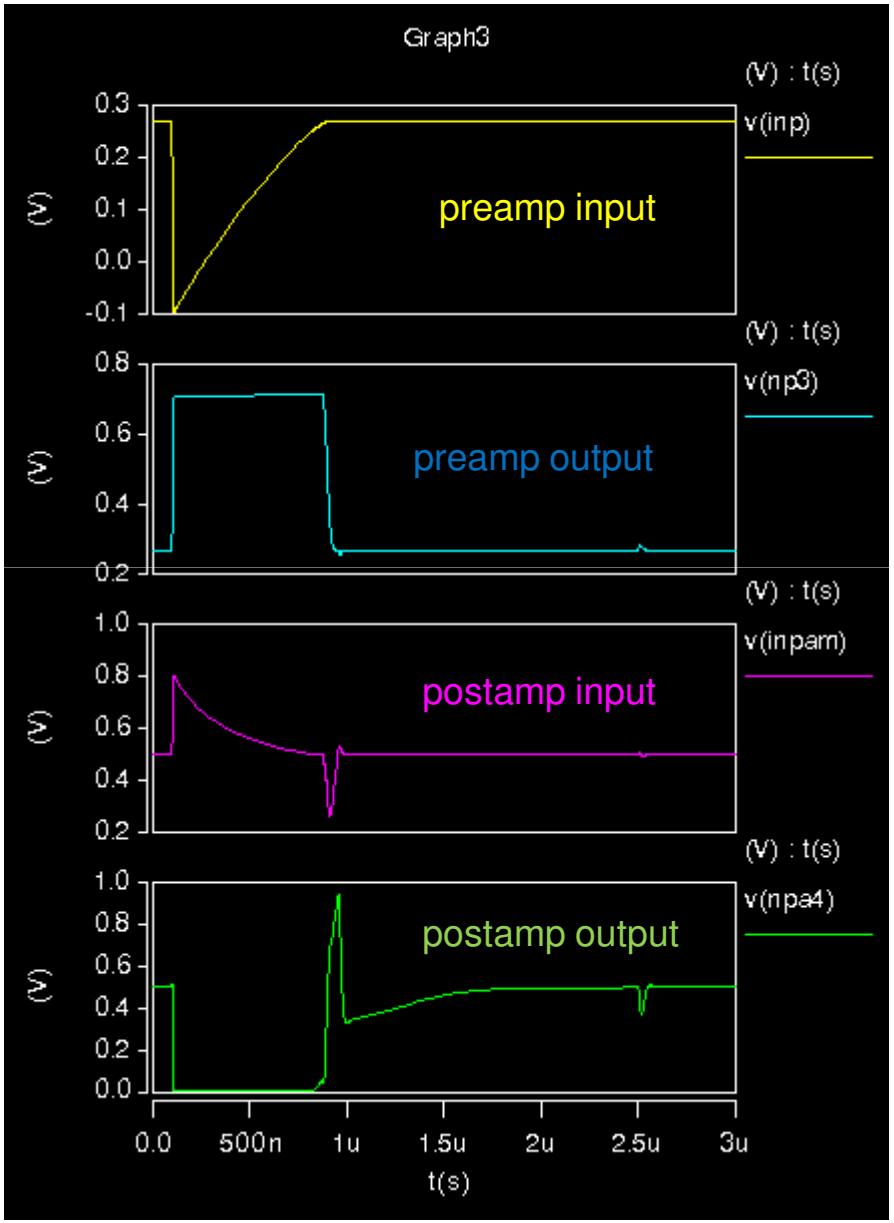
Integral spectrum: total prob. of pion depositing energy > E



spec. based on what is achievable

channel receiving 4 pC signal should be sensitive to normal signals after 2.5 usec

hips behaviour



single channel response

4 pC injected at t=100ns, 2.5 fC injected at t=2.5us

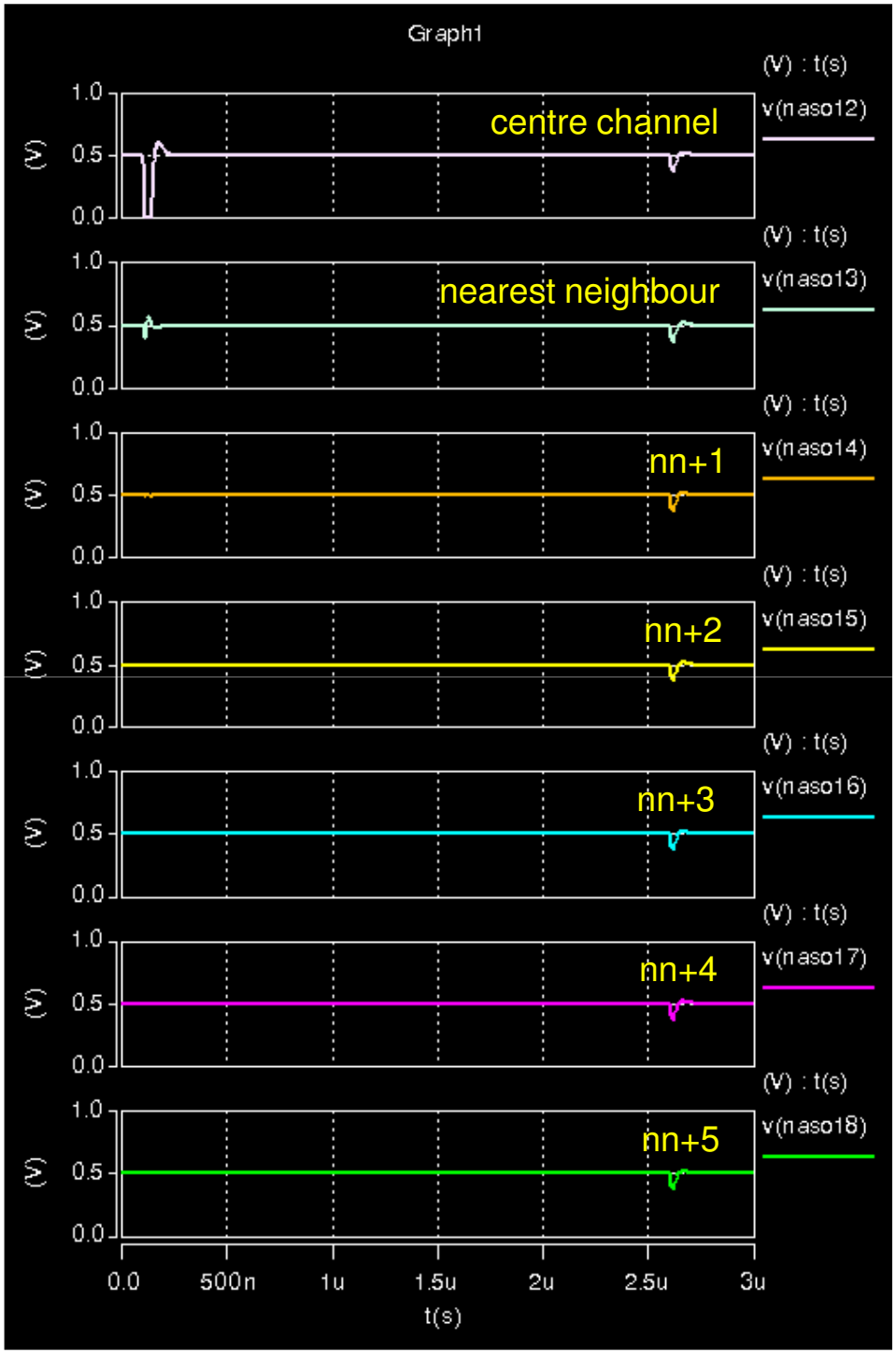
preamp can't "swallow" 4 pC
=> voltage builds up at input and discharges away through feedback resistance

preamp output saturates until charge has decayed away, then returns quickly to baseline

preamp output injects signal into postamp input via 1pF coupling capacitance. +ve signal discharges slowly (postamp feedback in high resistance region) -ve signal discharges quickly (postamp feedback in low resistance region)

postamp output initially saturates -ve
when preamp output recovers postamp output initially saturates +ve, recovers quickly but overshoots then recovers more slowly to baseline

back to normal sensitivity within 2.5 usec

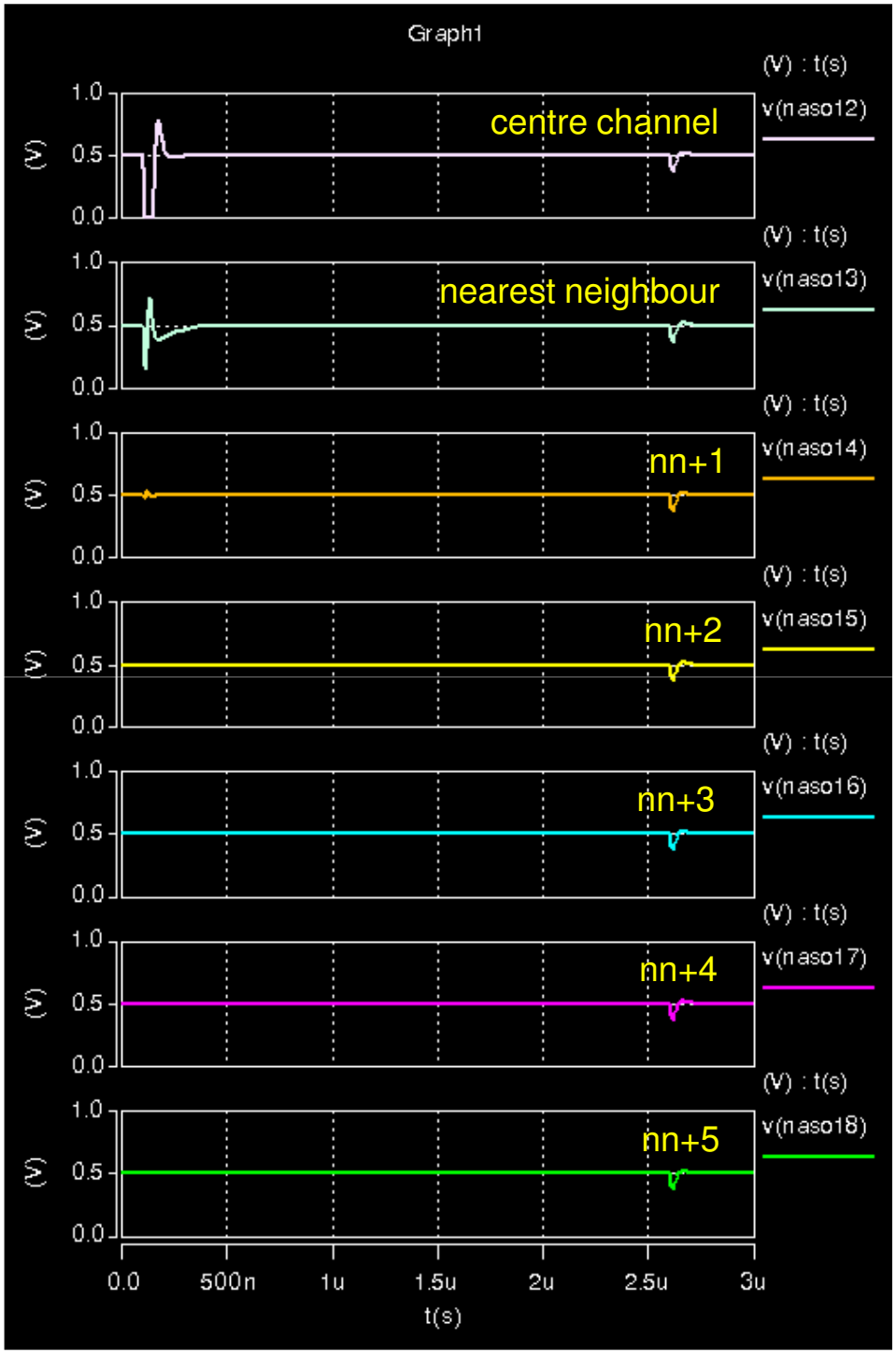


hips

40fC injected on centre channel at t = 100 nsec
(nominal bias conditions, typical process params)

2.5 fC injected on all channels at t = 2.5 usec

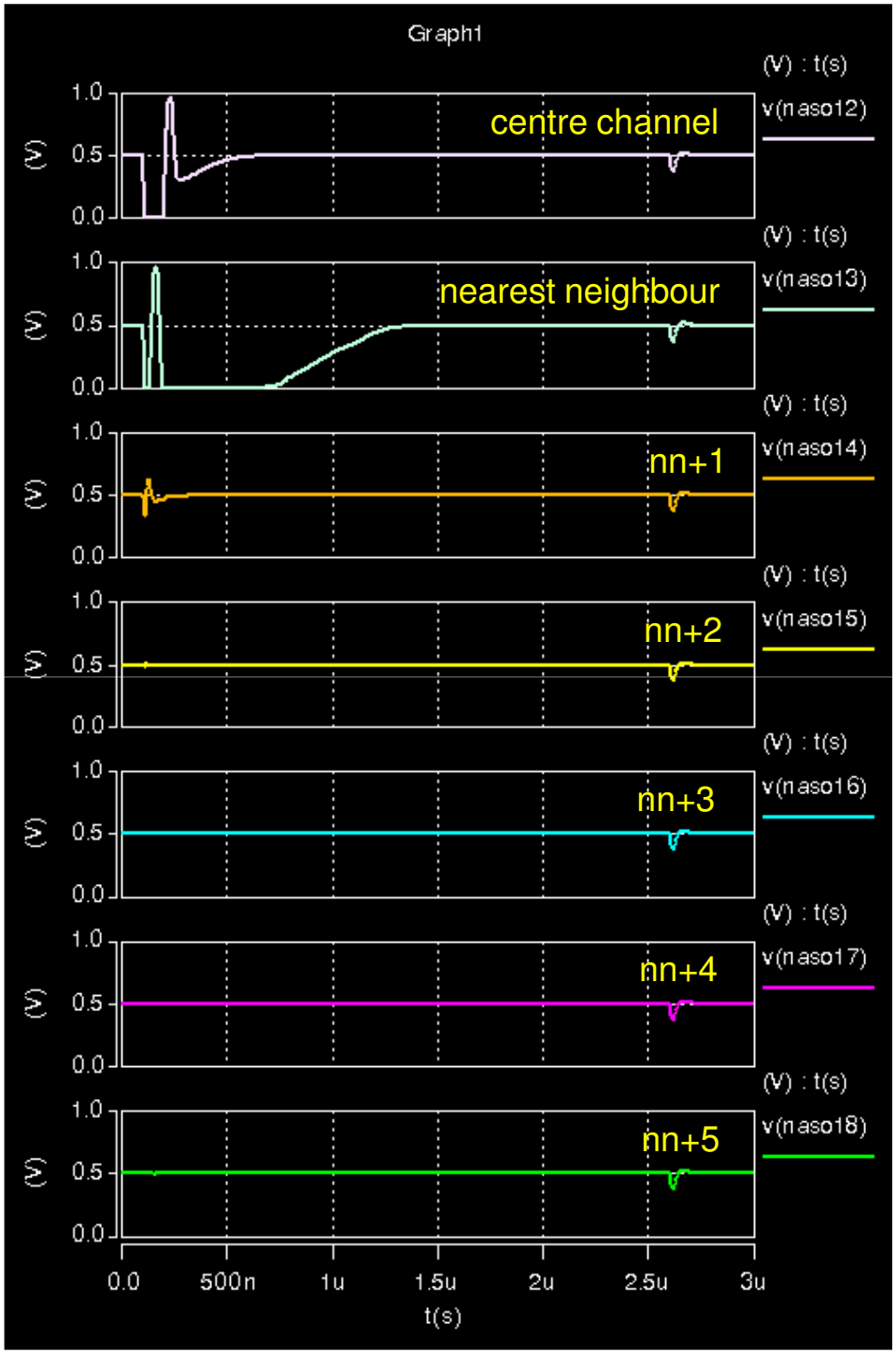
(5 mips = ~13 fC)



hips

100fC injected on centre channel at t = 100 nsec

2.5 fC injected on all channels at t = 2.5 usec



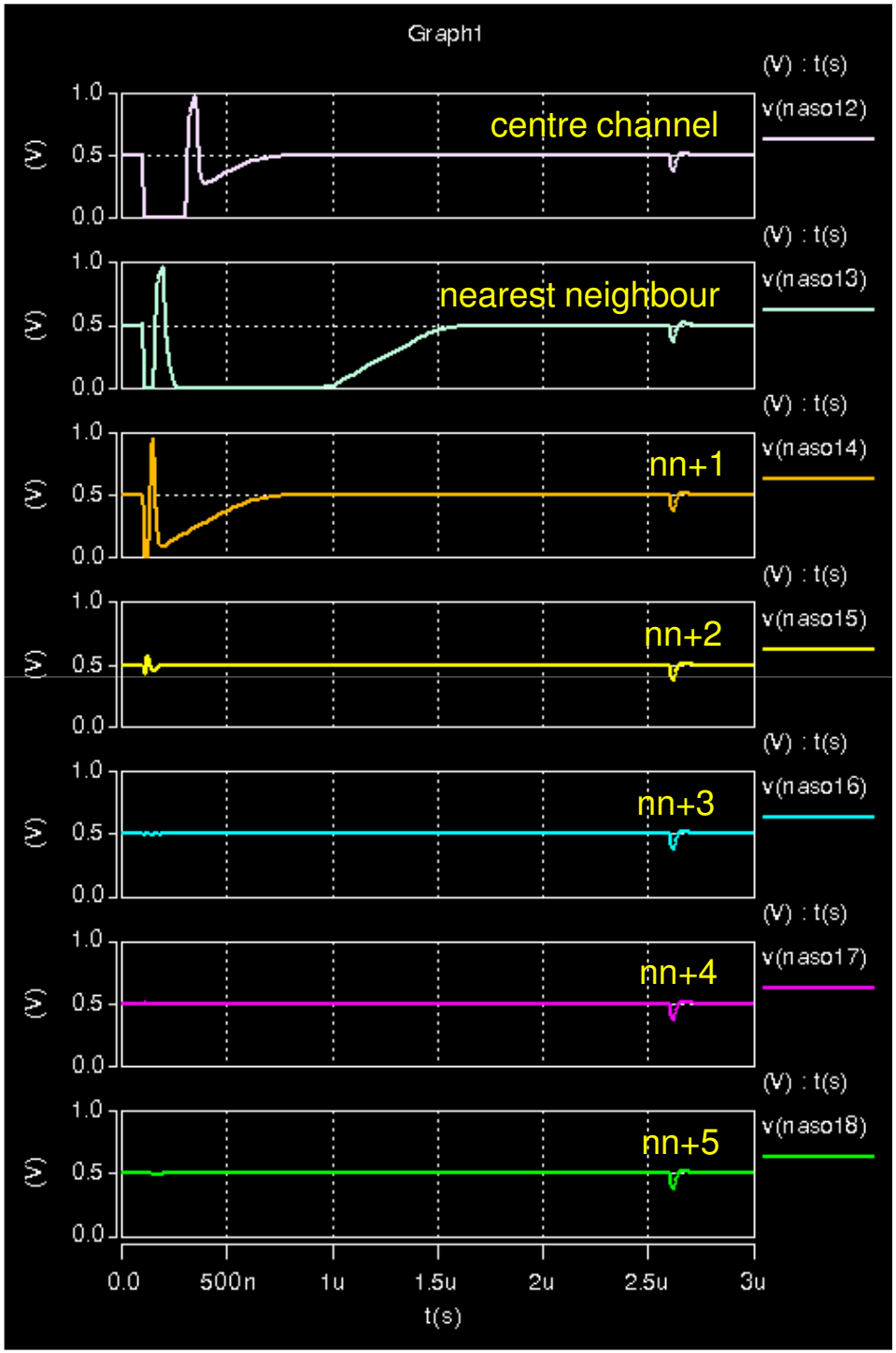
hips

400fC injected on centre channel at t = 100 nsec

2.5 fC injected on all channels at t = 2.5 usec

note: nearest neighbour takes longer to recover than centre channel

(why? - see backup)

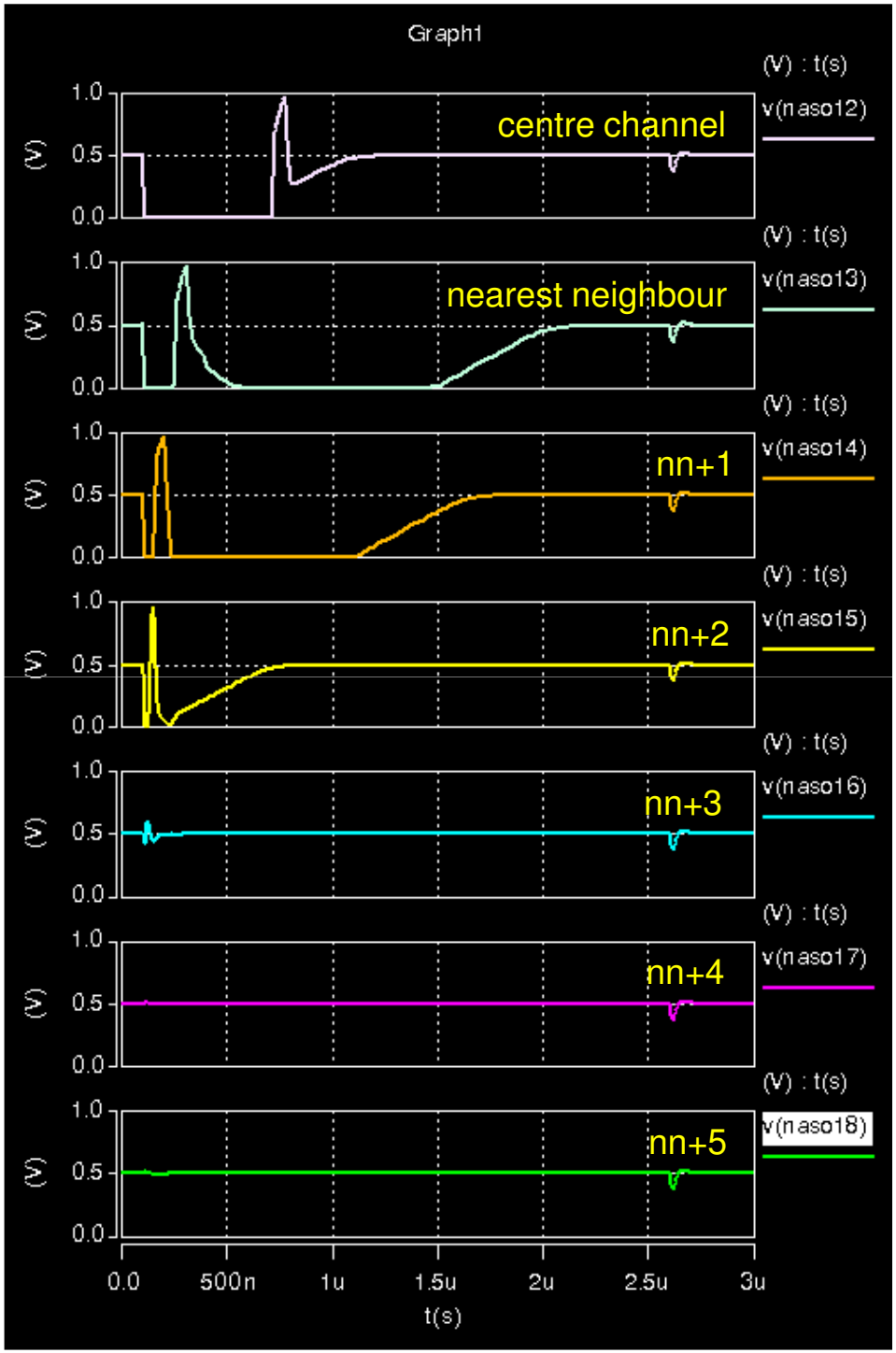


hips

1pC injected on centre channel at t = 100 nsec

2.5 fC injected on all channels at t =2.6 usec

all channels recovered by ~1.5 usec



hips

4pC injected on centre channel at t = 100 nsec

2.5 fC injected on all channels at t = 2.6 usec

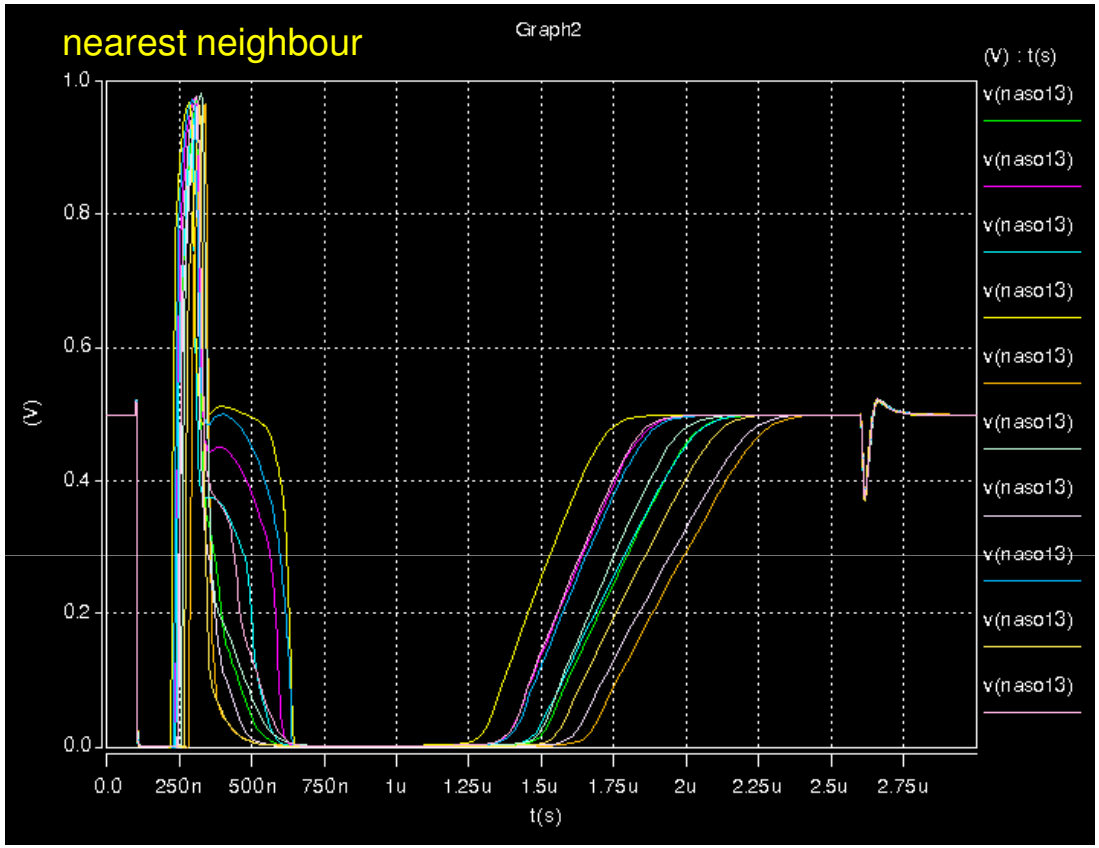
all channels recovered within ~2 usec

centre channel recovers before
nn, nn+1, ~nn+2

significant deadtime for centre chan.,
nn, nn+1, nn+2

nn+3 etc. ~ok

hips worst case



4pC injected on centre channel
at t = 100 nsec

2.5 fC injected on all channels
at t = 2.5 usec

look at worst channel
nearest neighbour

T=-20, +30, all corners

all channels recovered by
2.5 usec irrespective of
sim. conditions

hips and multi-channel simulations summary

interchannel crosstalk at ~5% level for normal signals

hips effects confined to central hit strip and some neighbours

number of neighbours depends on signal size

worst case 7 channels for 4 pC

~ 3-4 channels for 400 fC

~ negligible effect up to ~40 fC

all channels recovered within 2.5 usec

further work and issues: comparator

modification to balance current consumption when triggered/not triggered

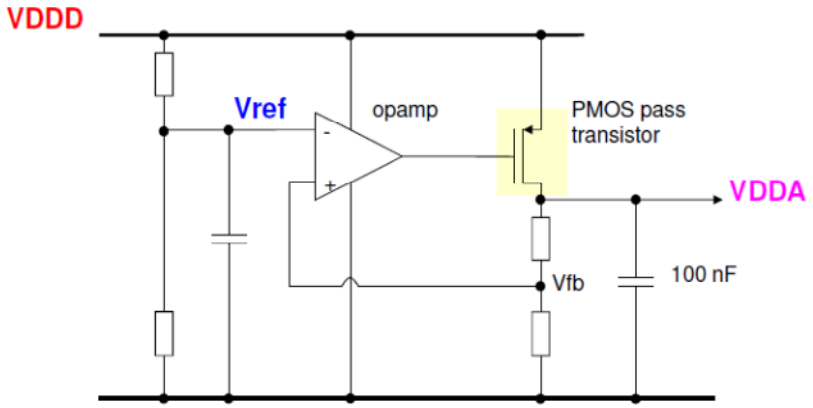
design exists - further simulation required - will report in future

further work and issues: powering

see last time for LDO reference proposals

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_powering_June2015.pdf

more work required



130nm bandgap

can still be used as reference for bias generator

but radiation issues limit accuracy

possibility to use PMOS based bandgap (Jan Kaplon)

more stable to radiation (ionizing and displacement)

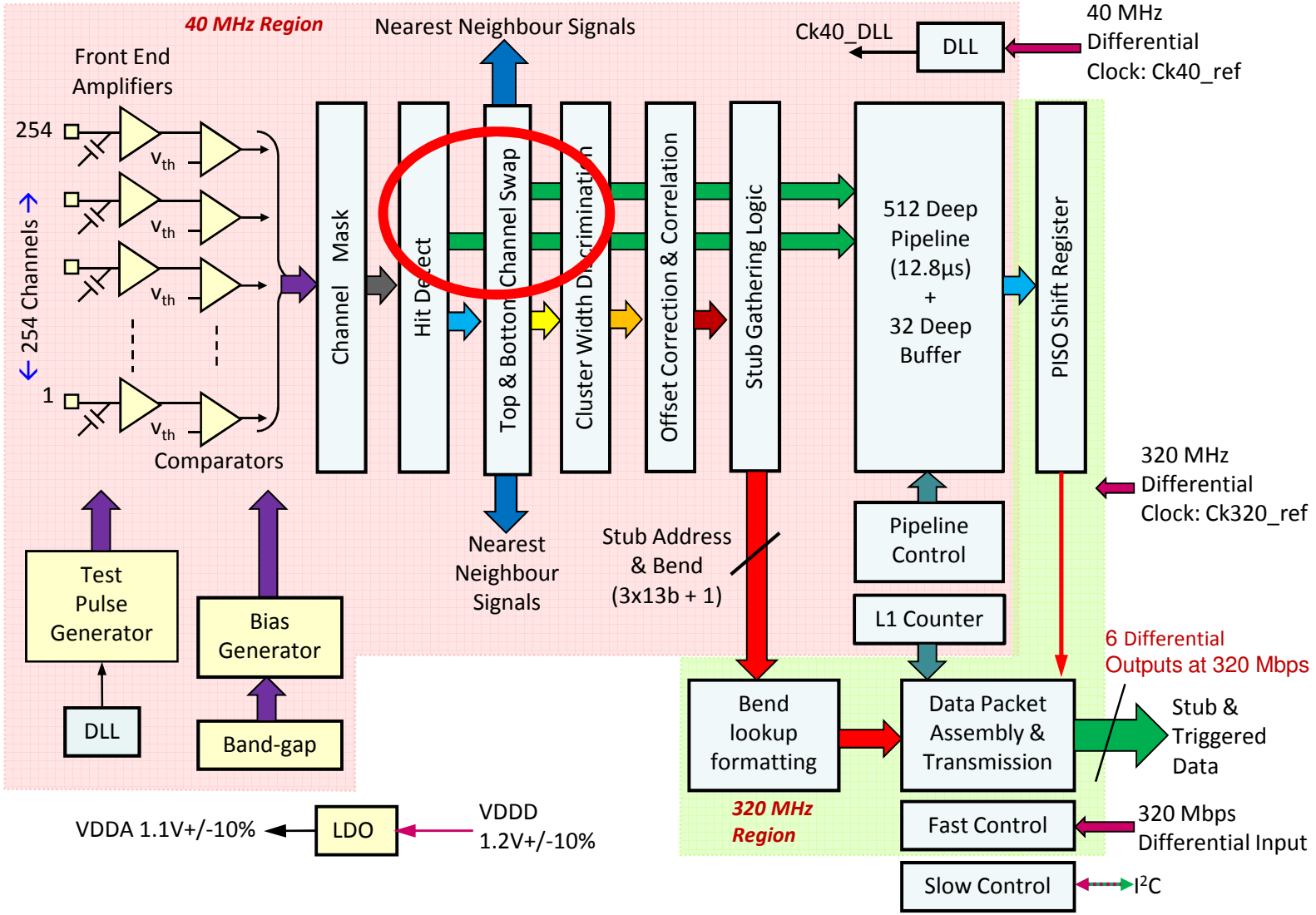
but stronger process dependence

possible approach could be to measure during wafer test and -

either reject chips with voltage outside acceptable range

or sort chips into close matched batches

signals to pipeline: layer swapped or not?



CWD block fed by layer swapped signals (1<->2, 3<->4, 5<->6,….) so seed layer is always nearest IP
should pipeline be fed by layer swapped signals or not?
(current thinking is “not”)

conclusions

CBC3 design progresses

design solutions exist for all new digital blocks

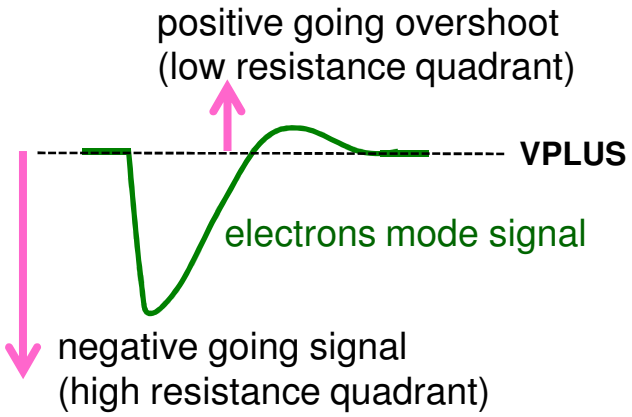
- no obvious implementation problems so far

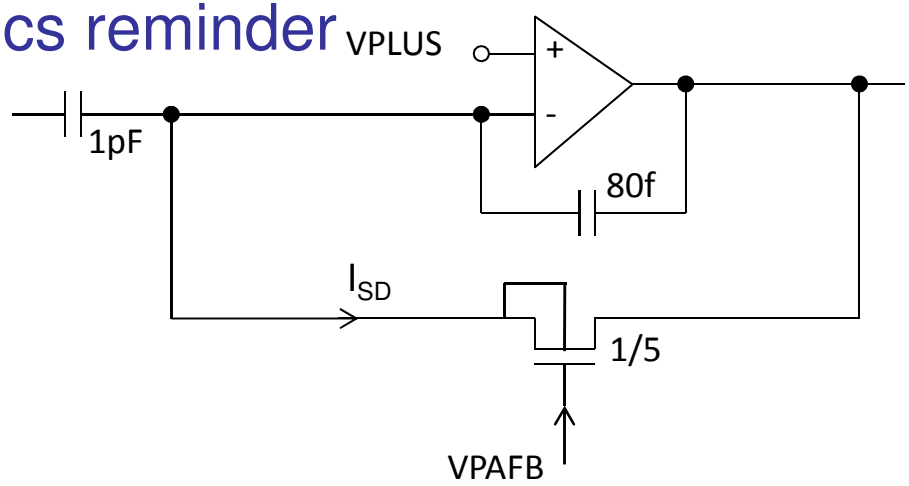
a few issues still to address

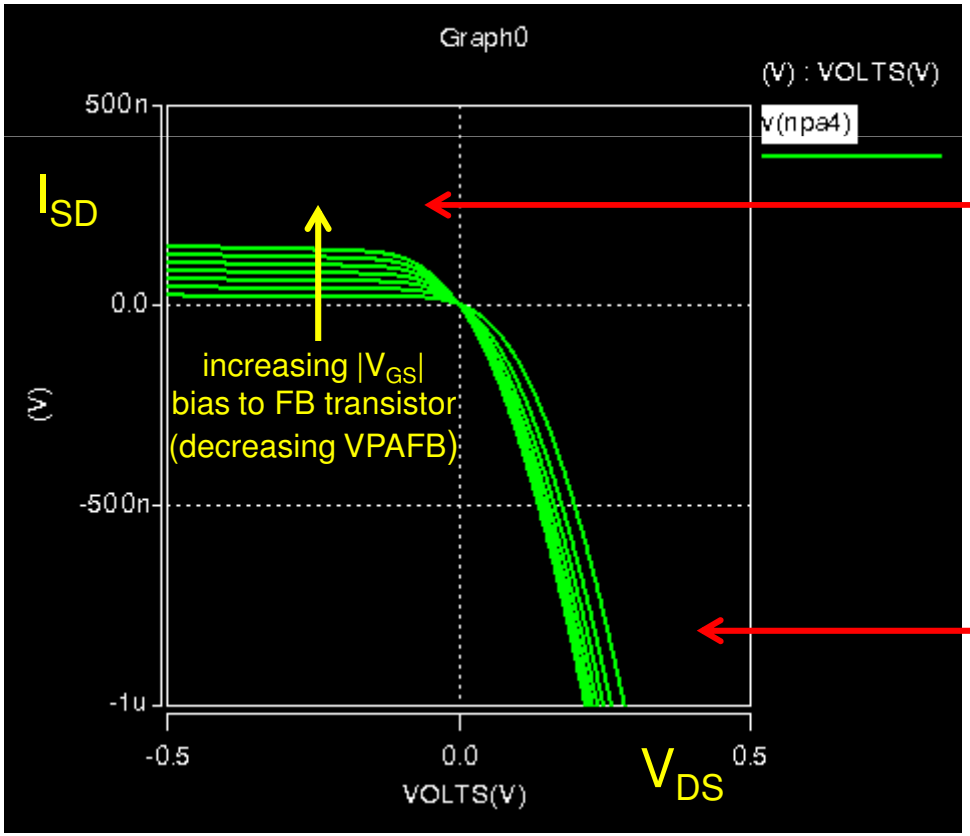
still on course for February submission

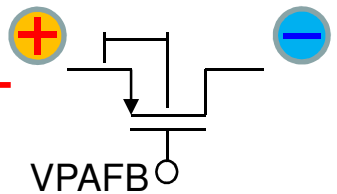
BACKUP

postamp feedback characteristics reminder

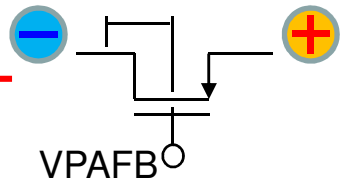






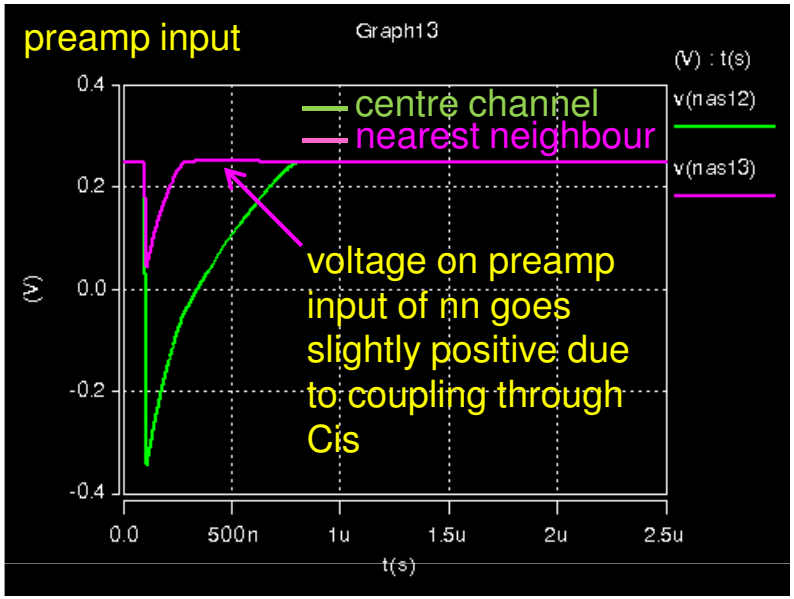


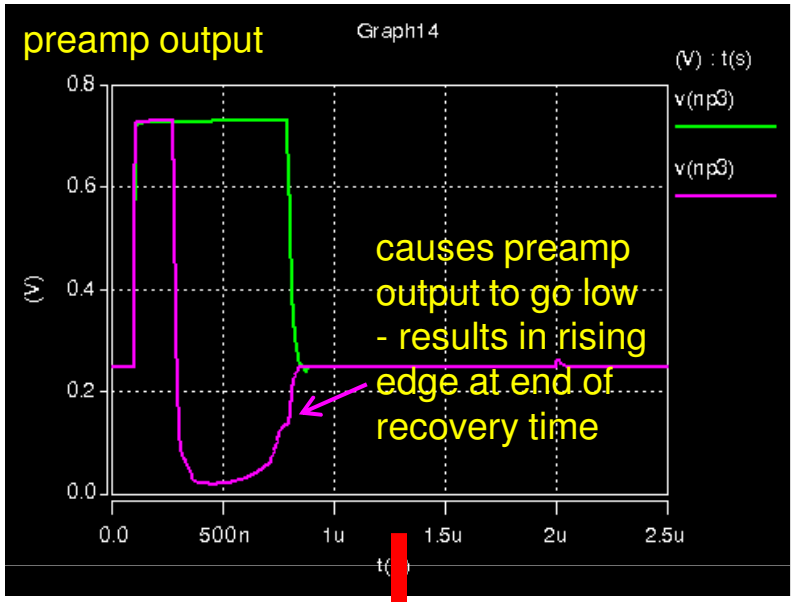
-ve going signal region
source at input side of postamp
V_{GS} ~ constant
only V_{DS} varies

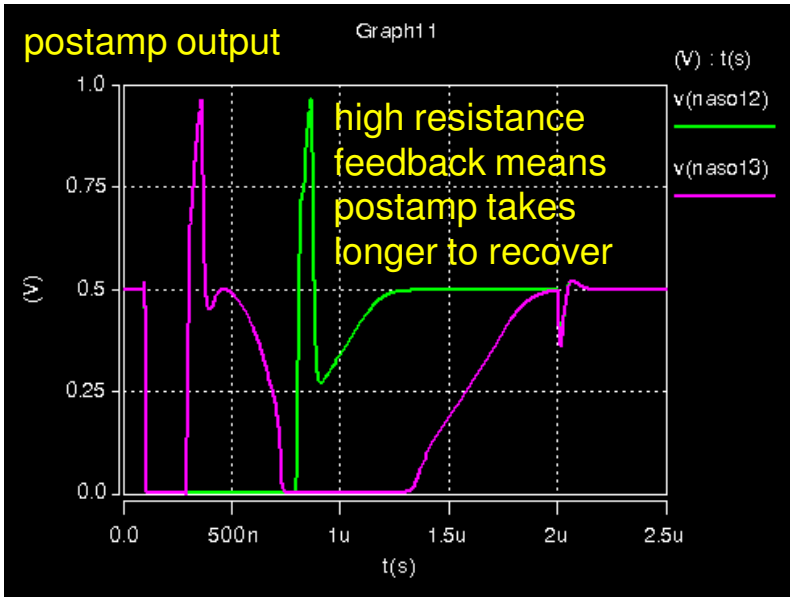


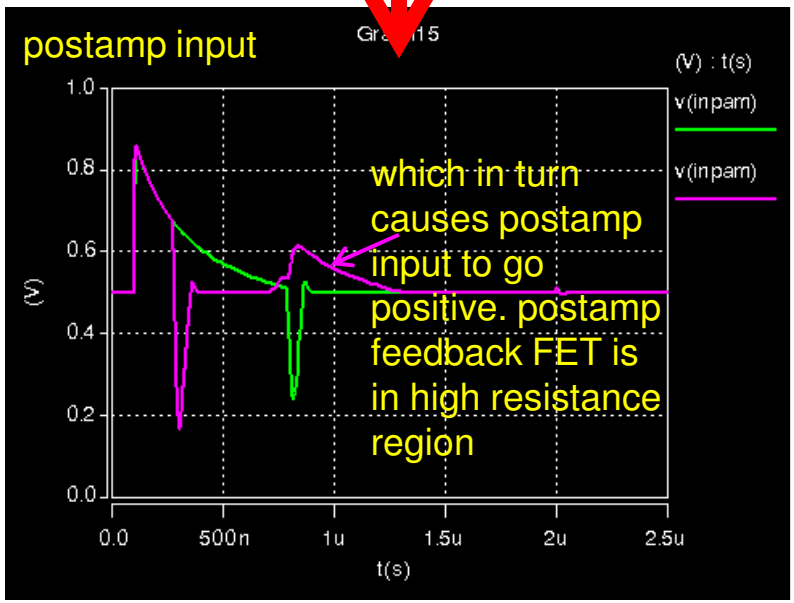
+ve going overshoot region
source swaps to output side
V_{GS} increases as postamp output overshoot increases

why is nearest neighbour hips deadtime worse than centre chan?

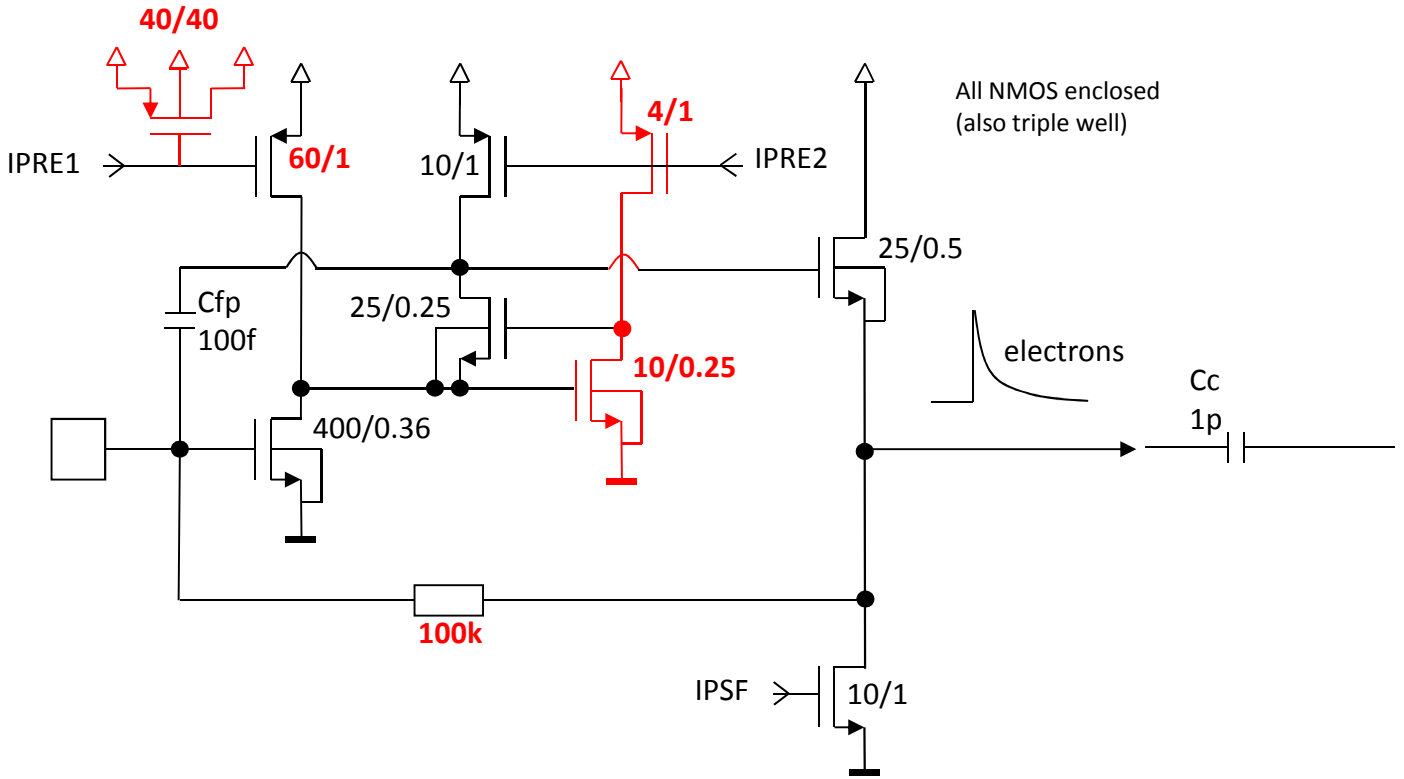


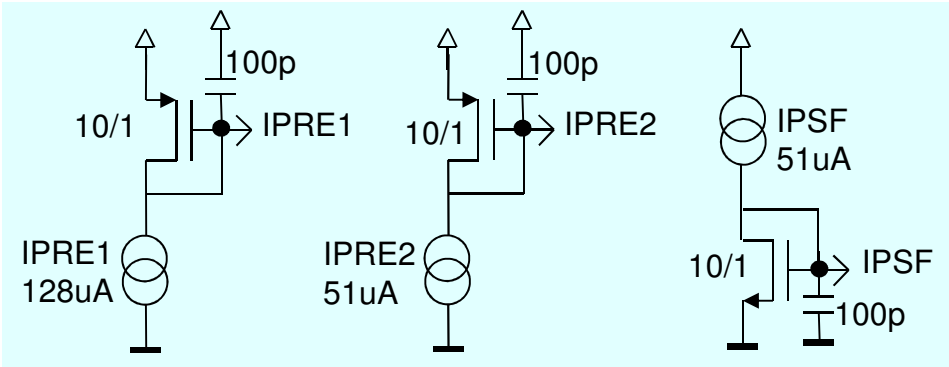




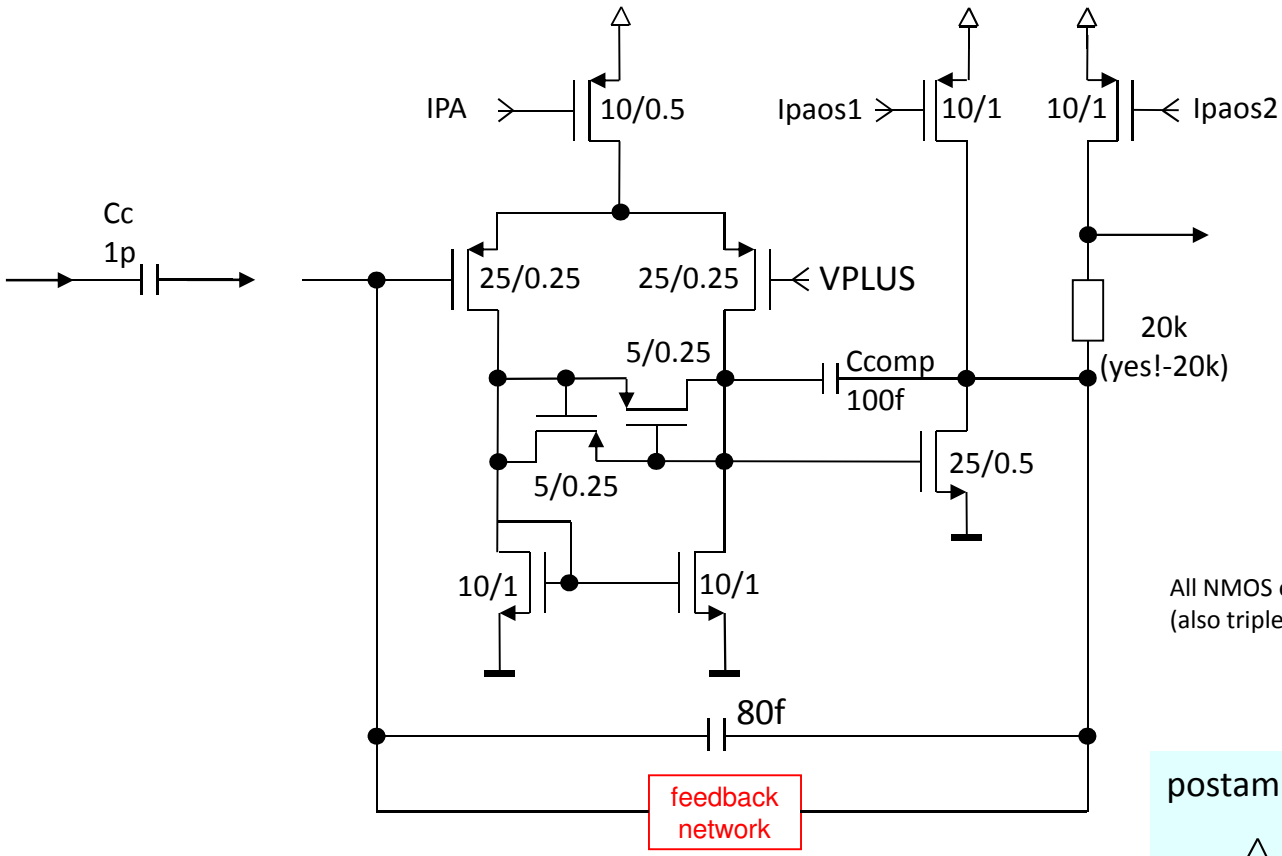


CBC3 Preamp with regulated cascode



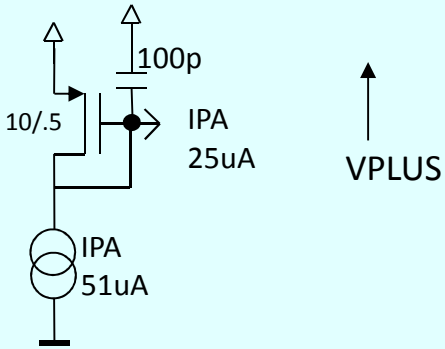


CBC3 Postamp

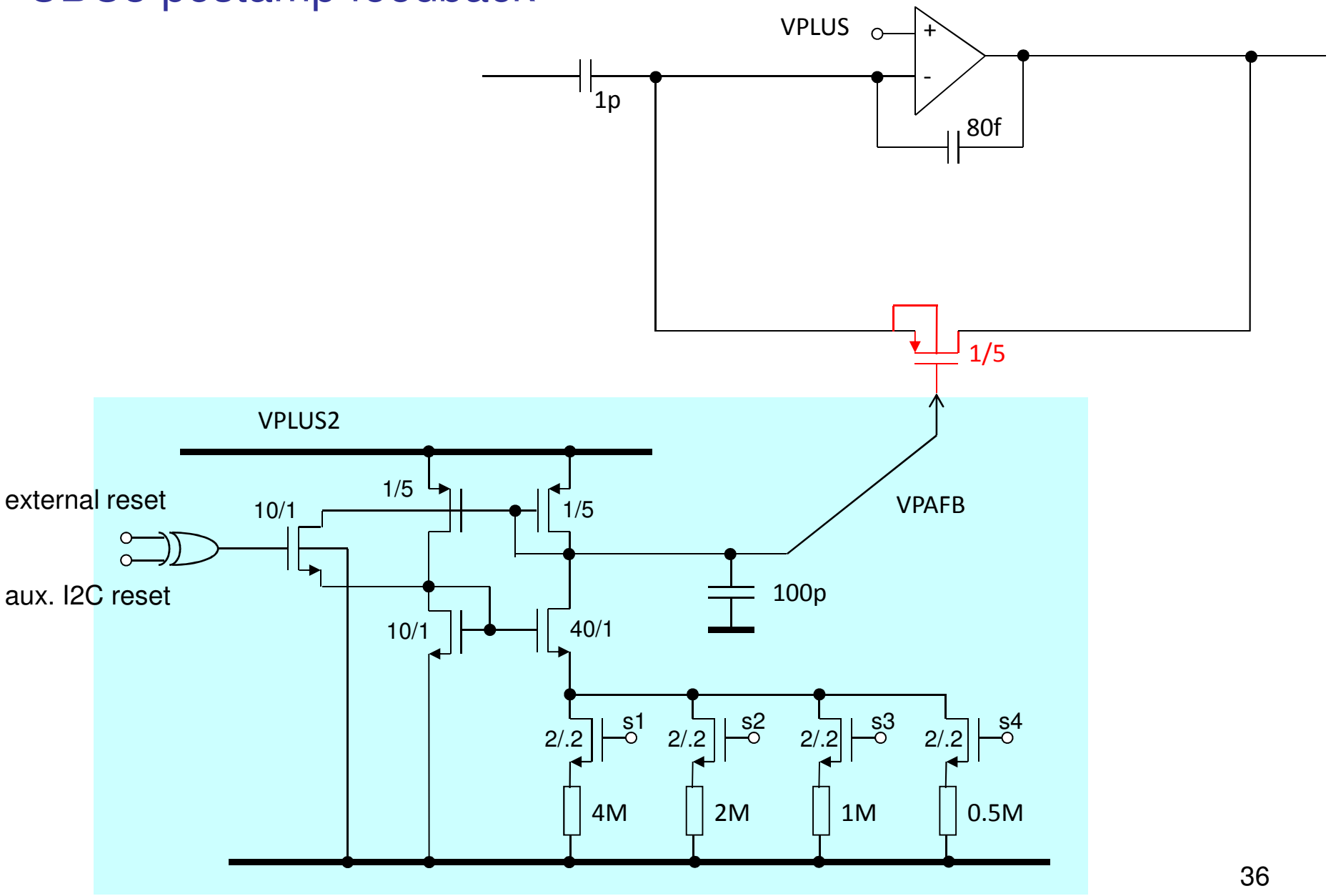


All NMOS enclosed
(also triple well)

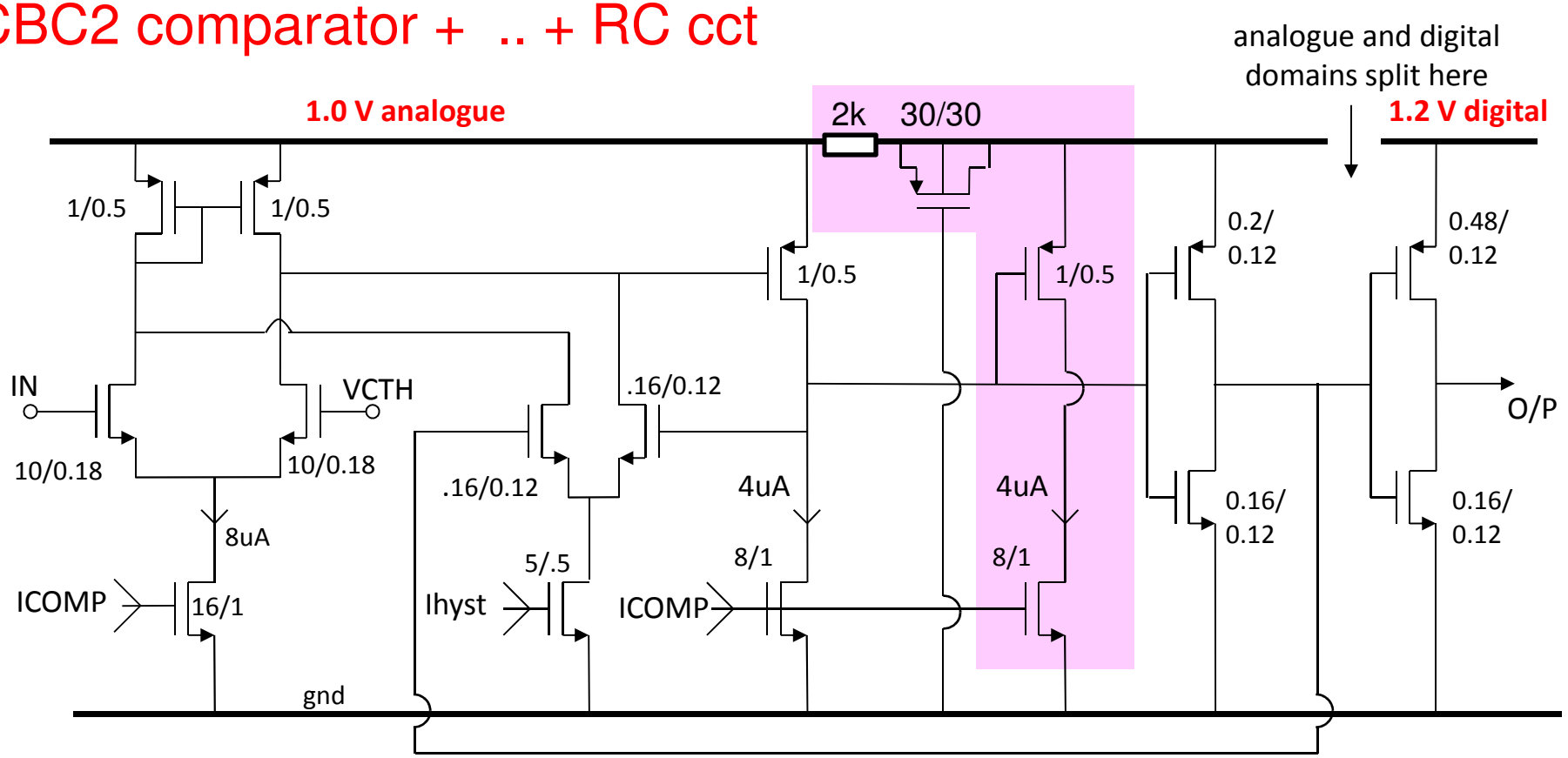
postamp bias (1 per chip)

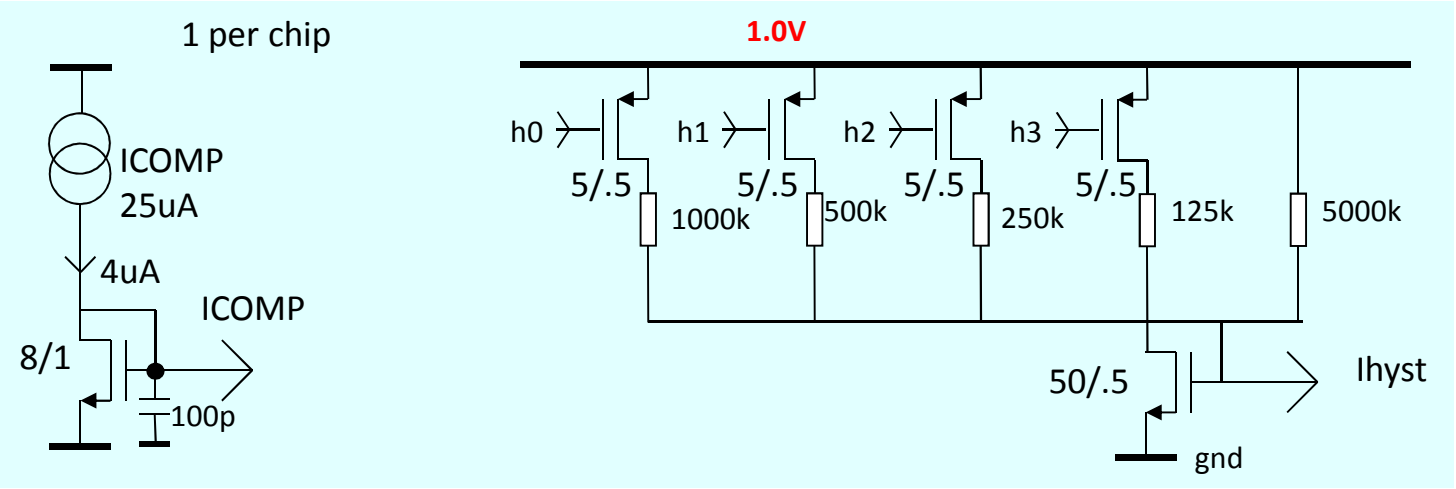


CBC3 postamp feedback



CBC2 comparator + .. + RC cct





30/30 -> ~10pF

not yet confirmed as final design