CBC3 progress (2)

front end progress
HIPs deadtime calculations
powering and voltage reference thoughts

systems meeting, 23rd September, 2015.

CBC3 design progress - previous presentations

preamplifier changes

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3%20Progress_Apr_15%20.pdf

increased input FET bias current range, reg. cascode, 100k feedback resistor, electrons only

postamp changes

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_FE_status_June2015.pdf

electrons only, new feedback bias circuit

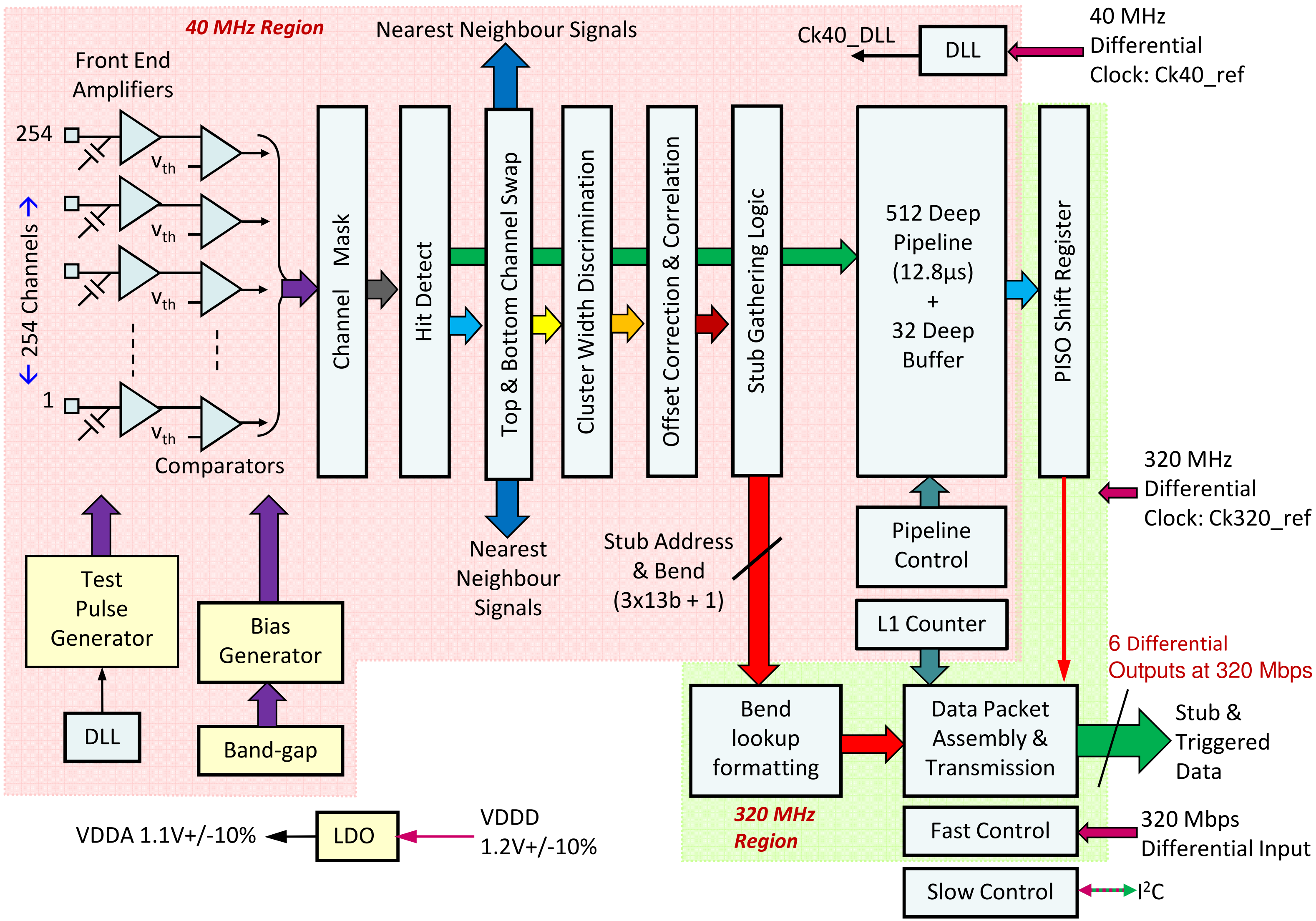
digital blocks

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_systems_July2015.pdf

progress through to layout & post layout simulations of:

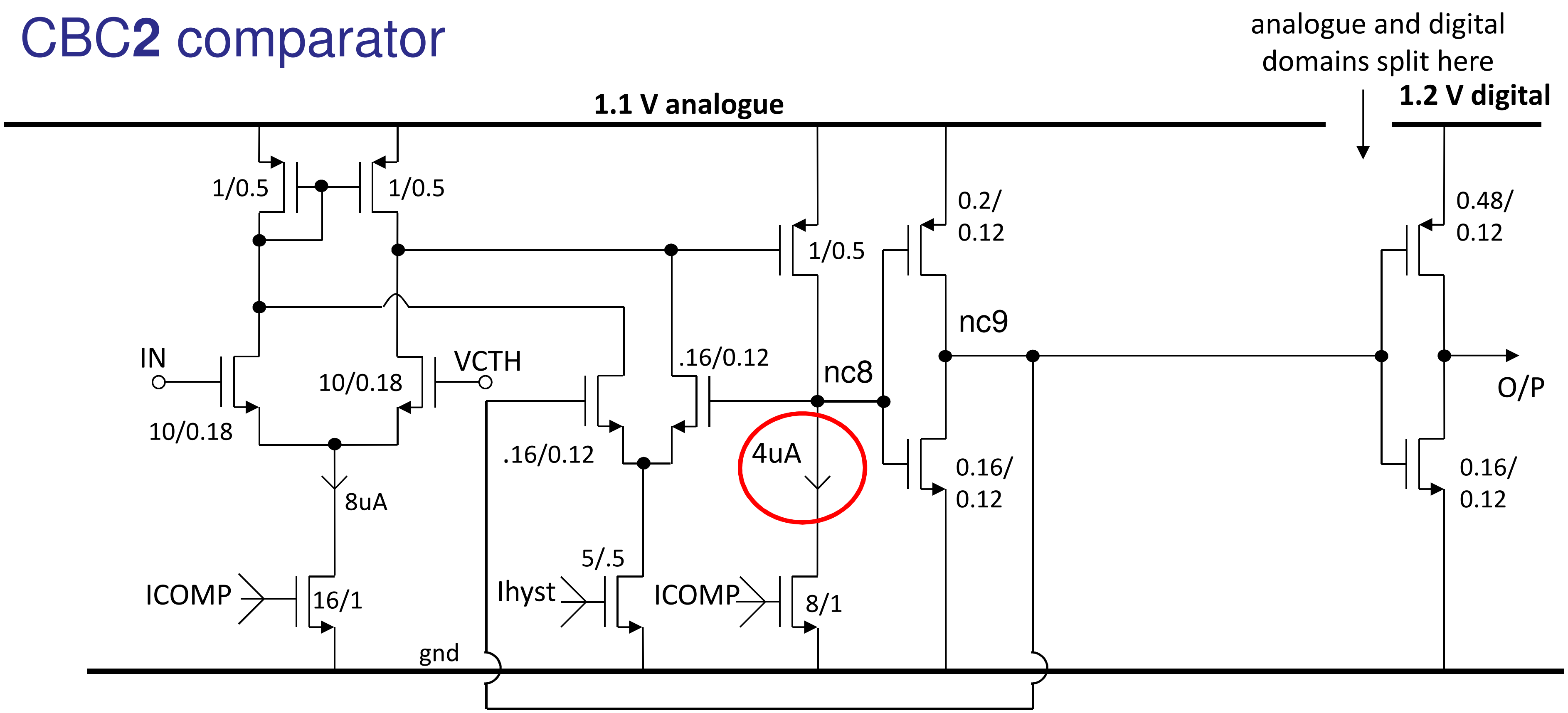
- hit detect
- stub gathering logic
- data packet assembly & transmission
- output (PISO) shift register, L1 counter
- fast control interface

for reference

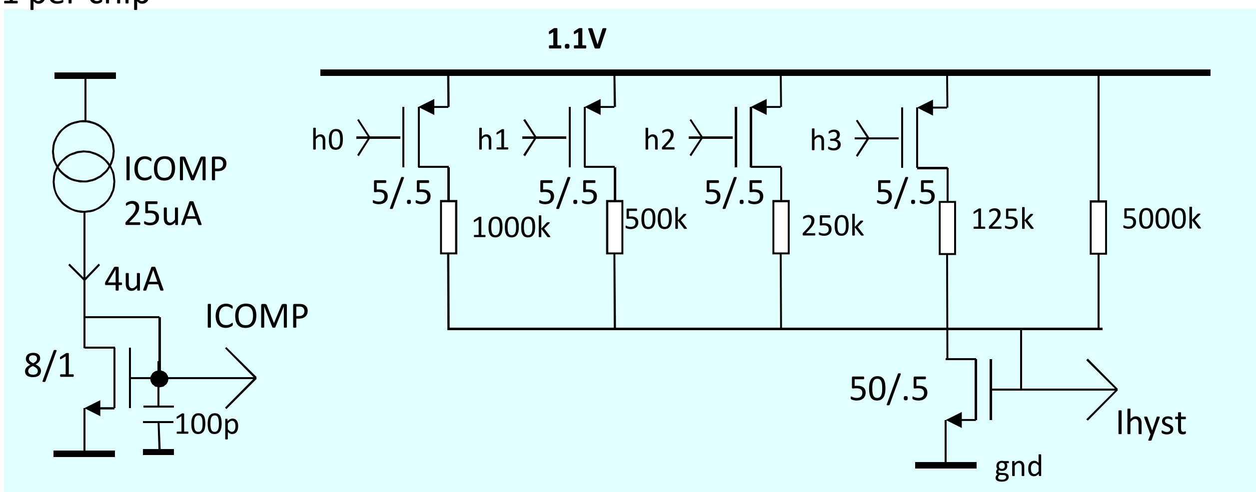


CBC3 comparator progress

CBC2 comparator



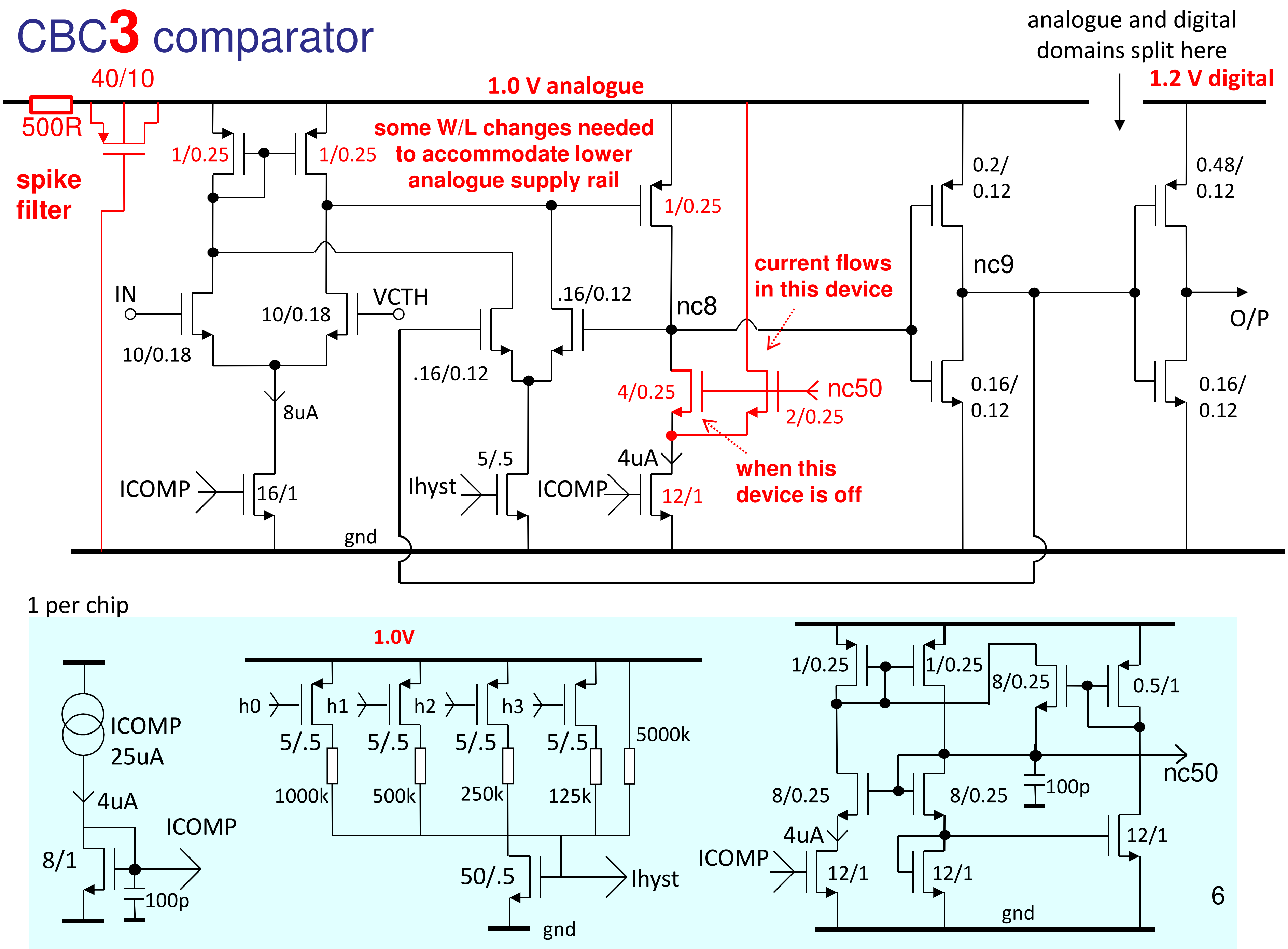
1 per chip



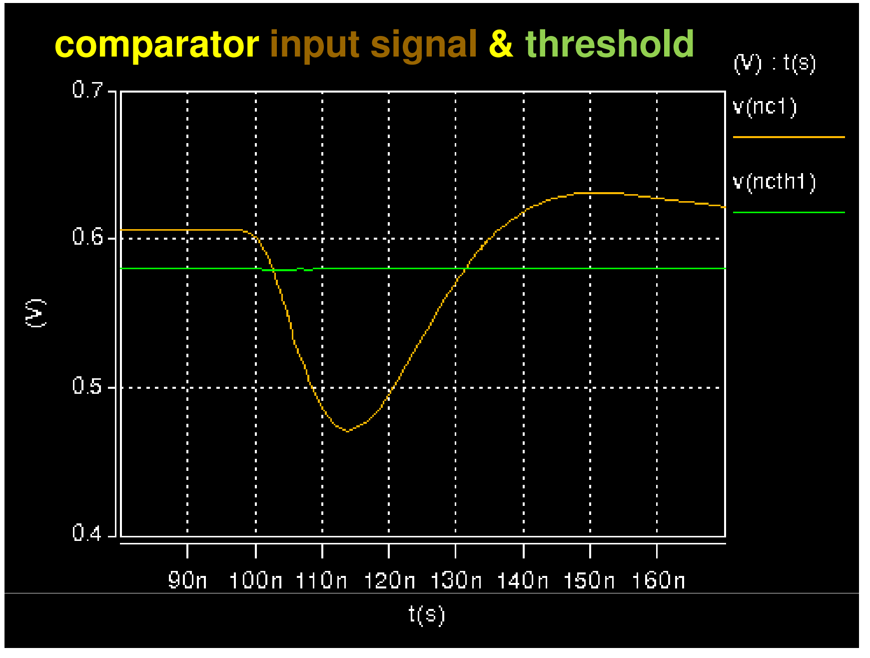
problem: when comparator switches overall current changes

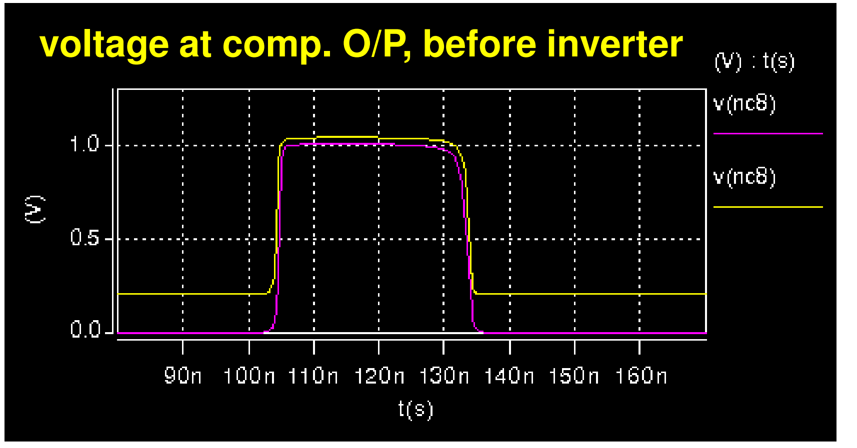
not so good when lots of channels switching at same time

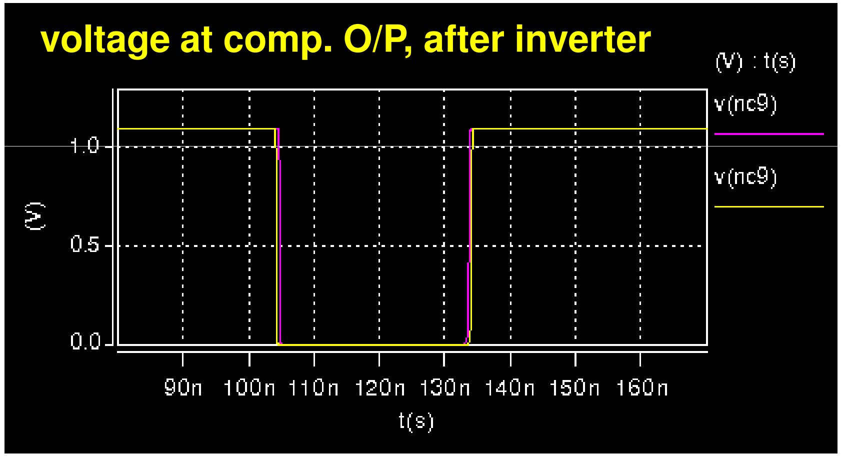
CBC3 comparator

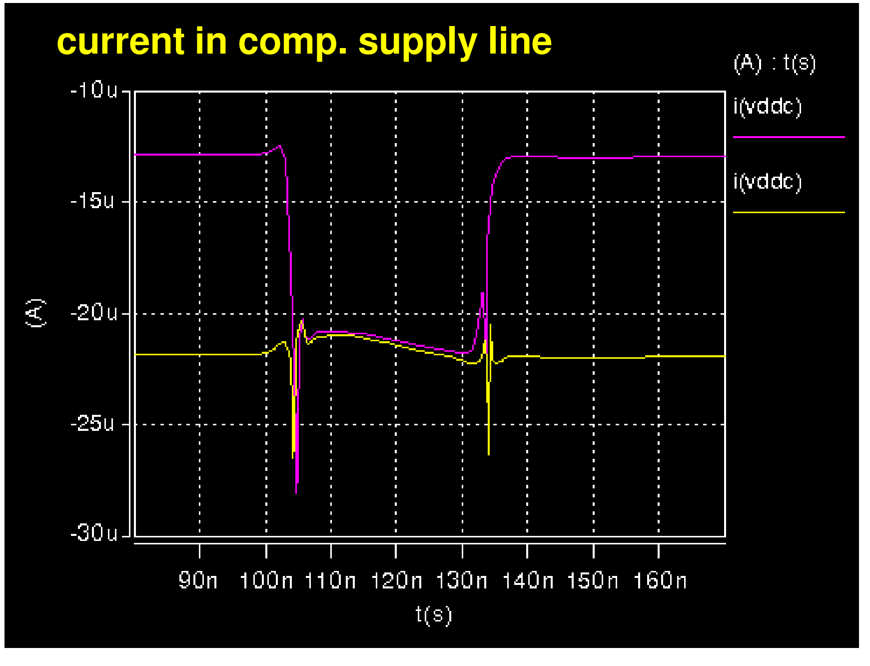


transient analysis: T=0, process=tt, VDD=1.1, ICOMP=6u



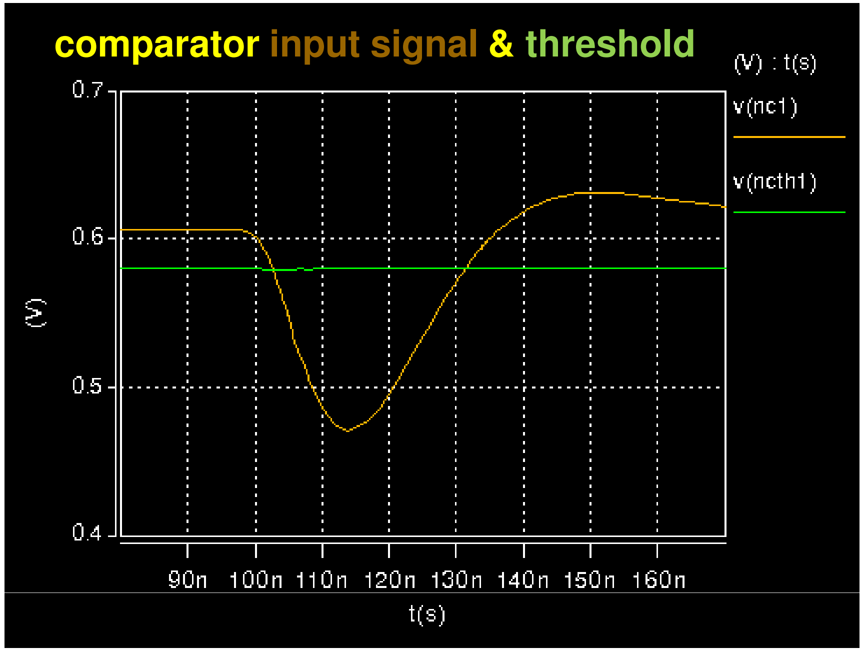


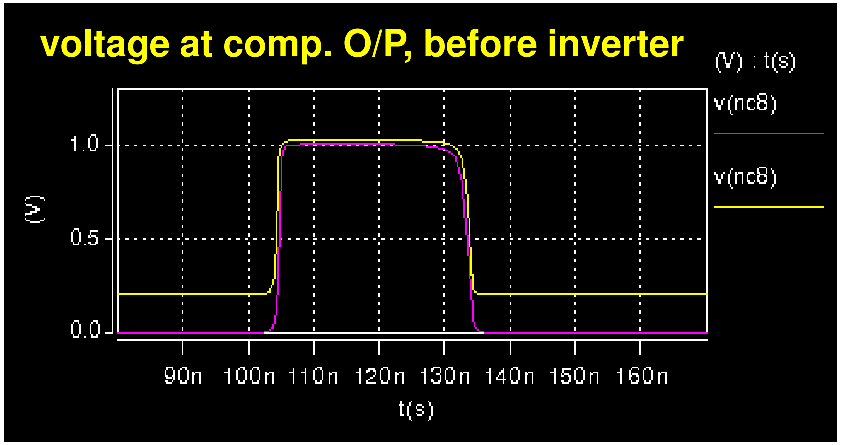


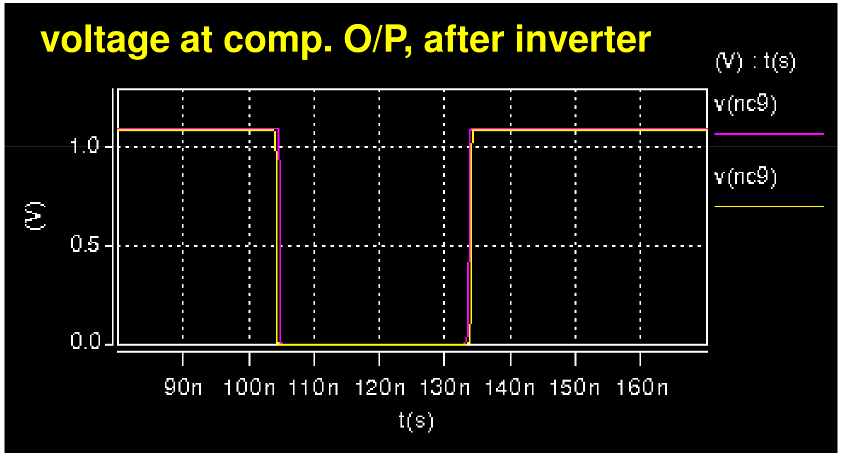


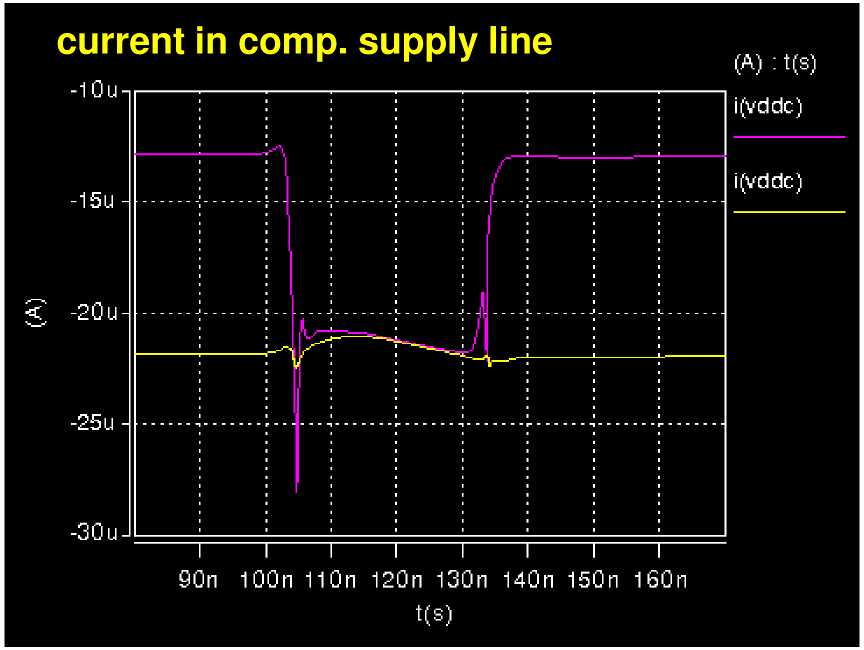
O/P stage modification solves the current switch problem
response shown here **without** the RC filter - some sharp current spikes

transient analysis: T=0, process=tt, VDD=1.1, ICOMP=6u





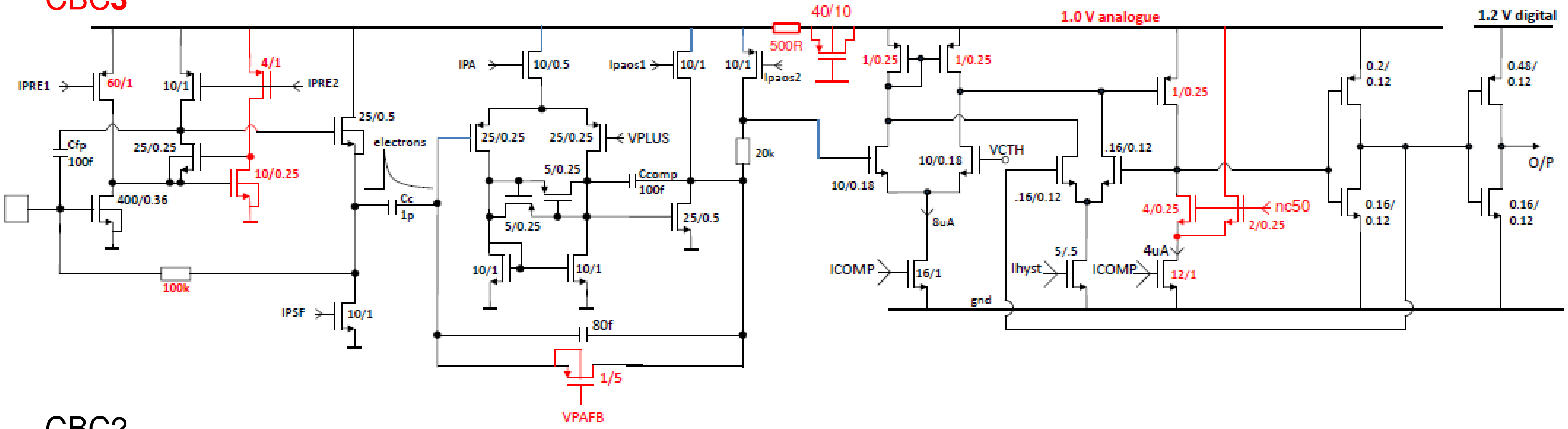




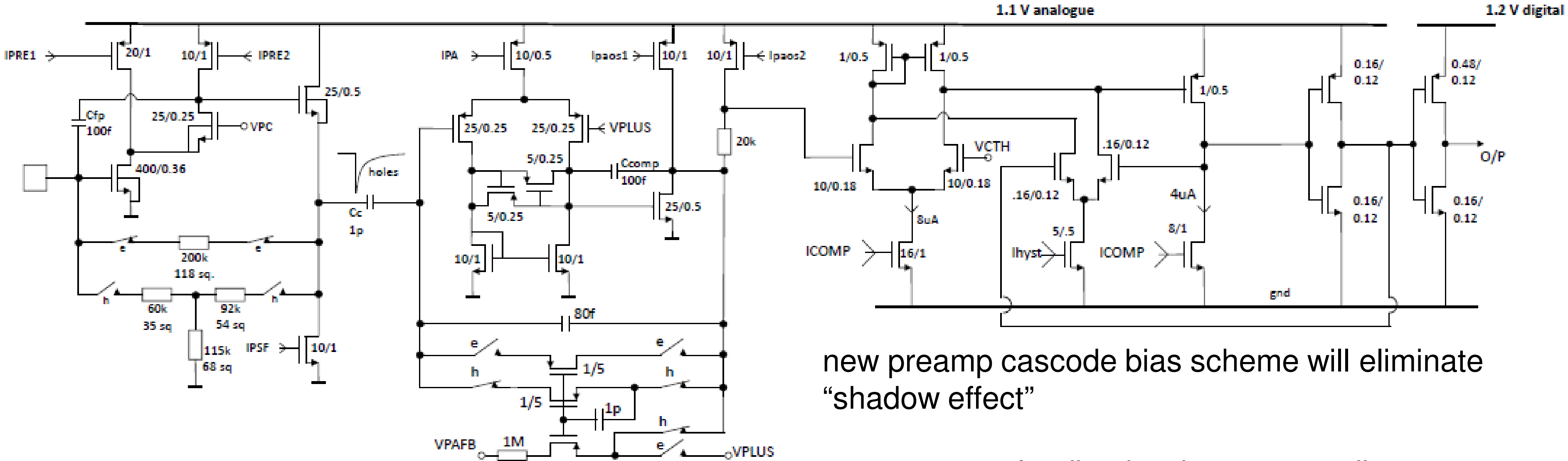
O/P stage modification solves the current switch problem
response shown here **with** the RC filter - sharp spikes filtered out

front end design changes complete

CBC3



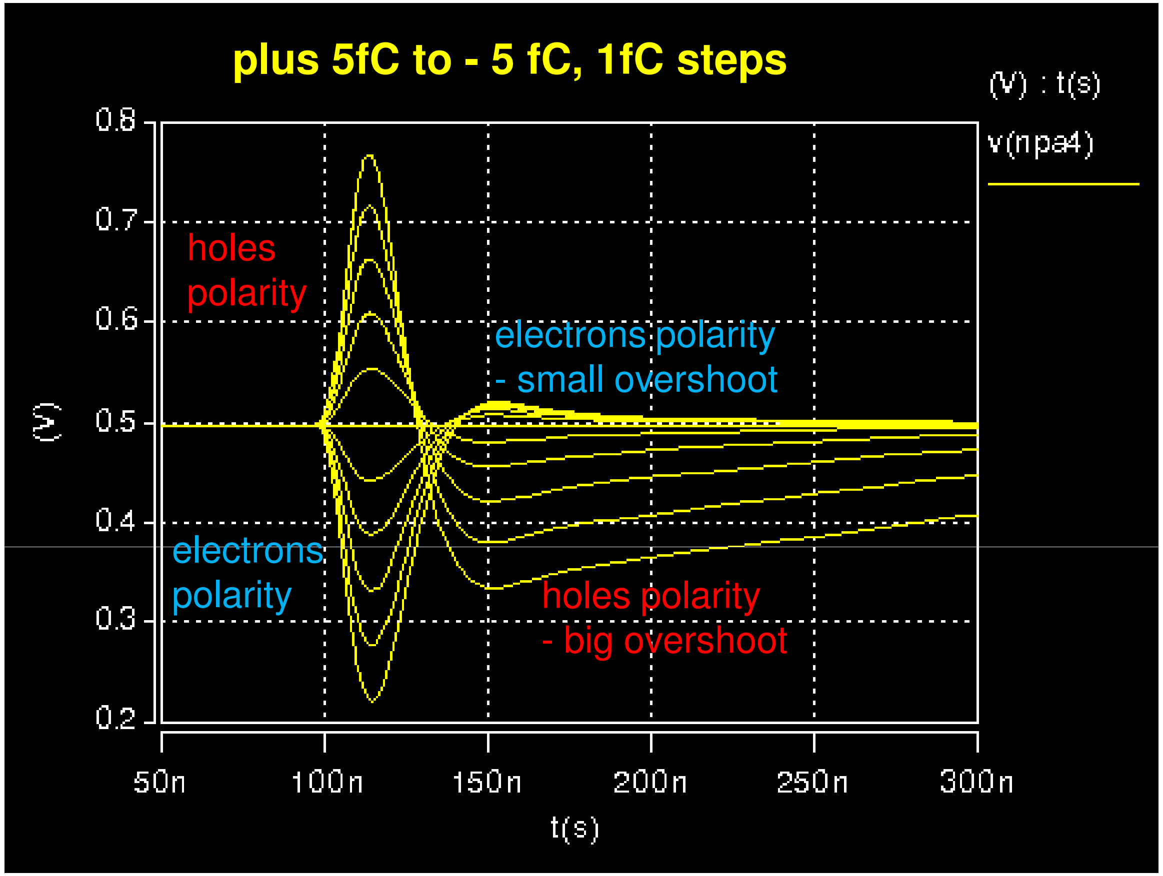
CBC2



new preamp cascode bias scheme will eliminate "shadow effect"

new postamp feedback scheme, as well as current neutral comparator will address CM effects observed when many channels fire

holes polarity response



(for info only - chip not designed for holes polarity)

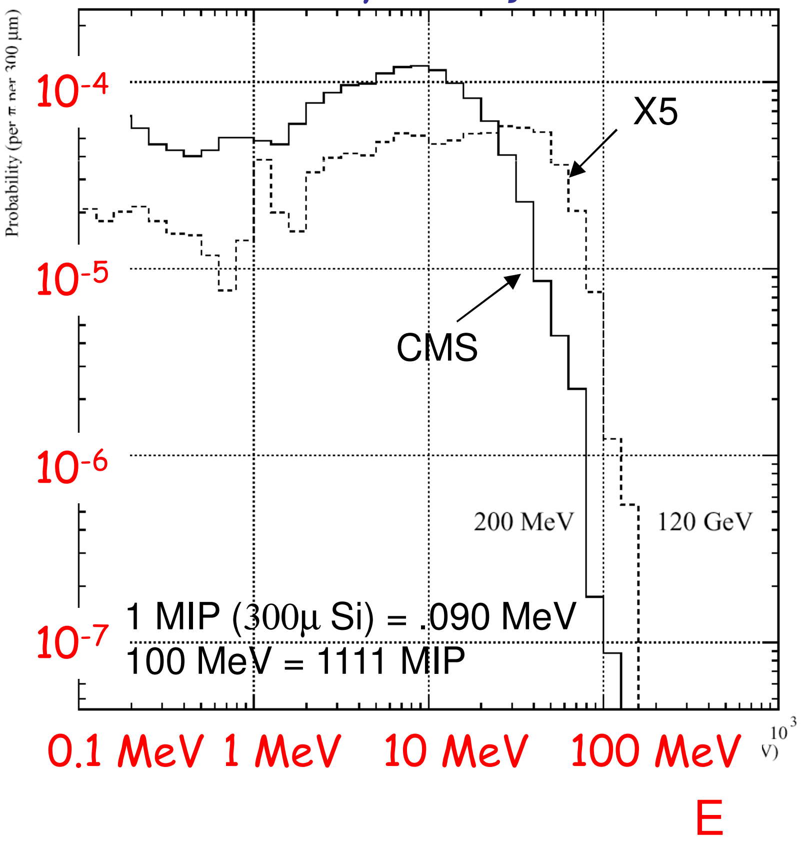
HIPs effect calculations

details of electronics HIPs response shown last time

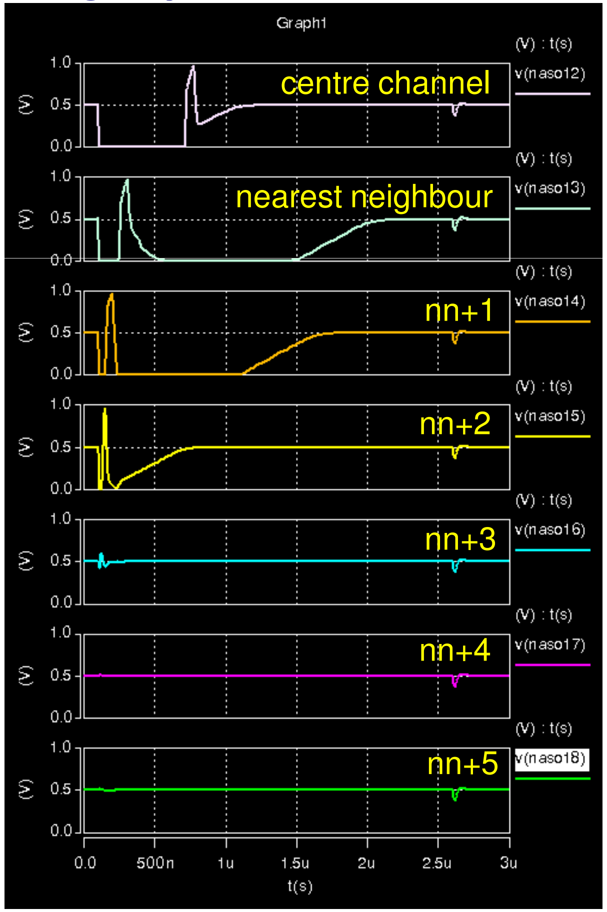
http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_systems_July2015.pdf

will today show calculation of hit loss

probability/incident pion of depositing energy E in 300μm Si layer

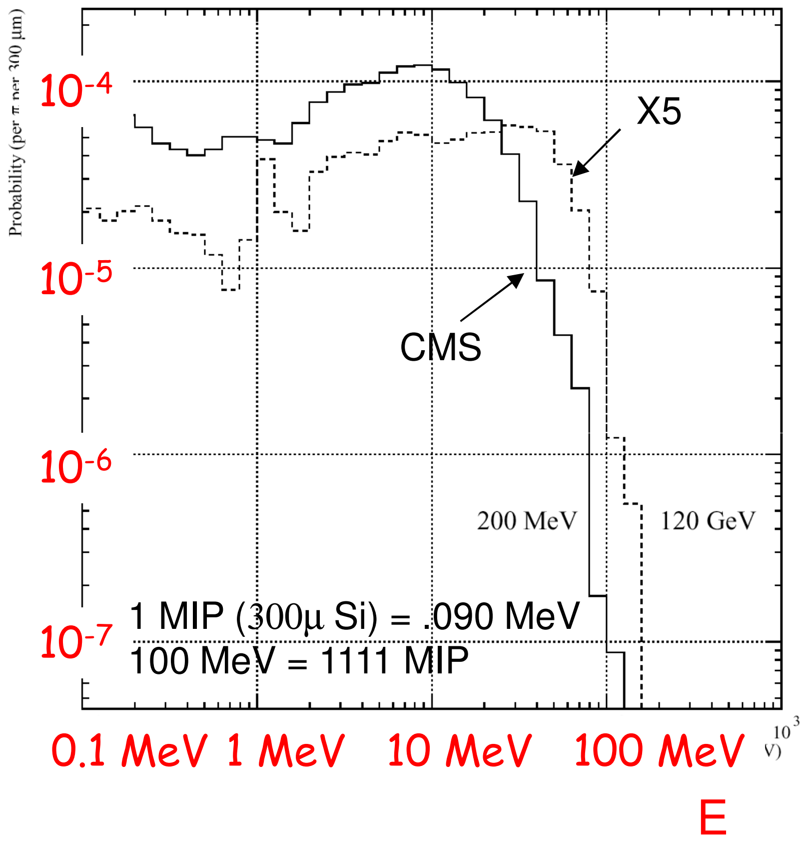


postamp output response to 4pC charge injected on centre channel



HIPs energy spectrum - M.Huhtinen simulations

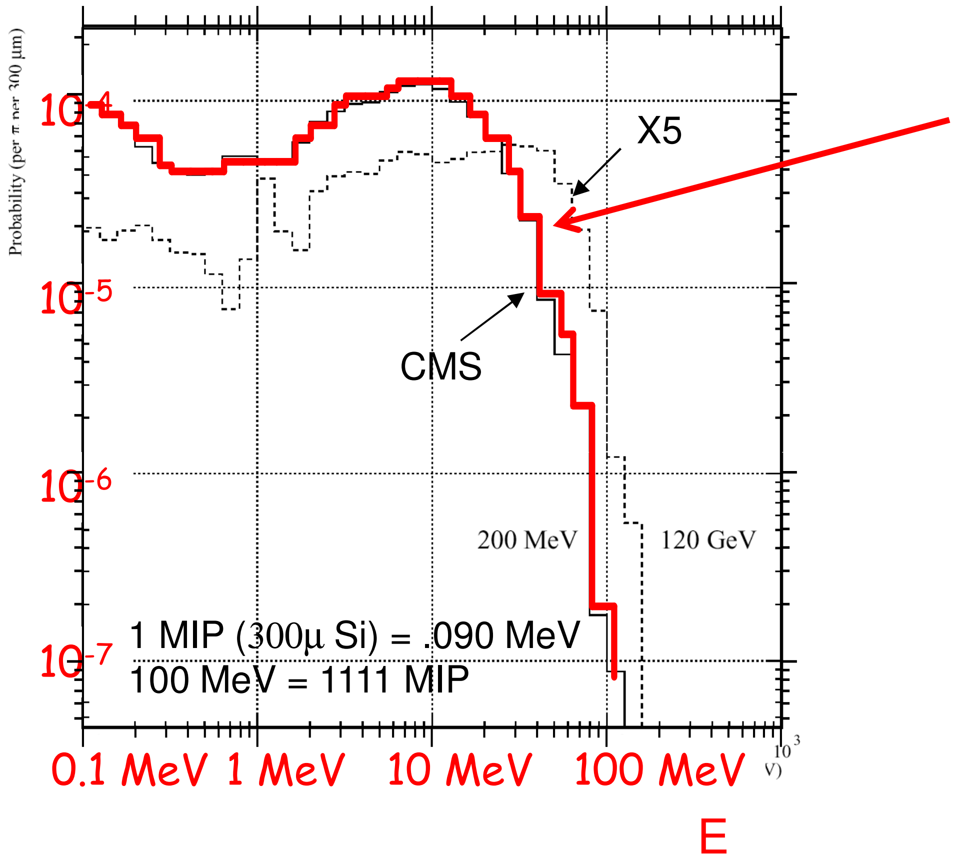
Probability/incident pion of depositing energy E in 300µm Si layer



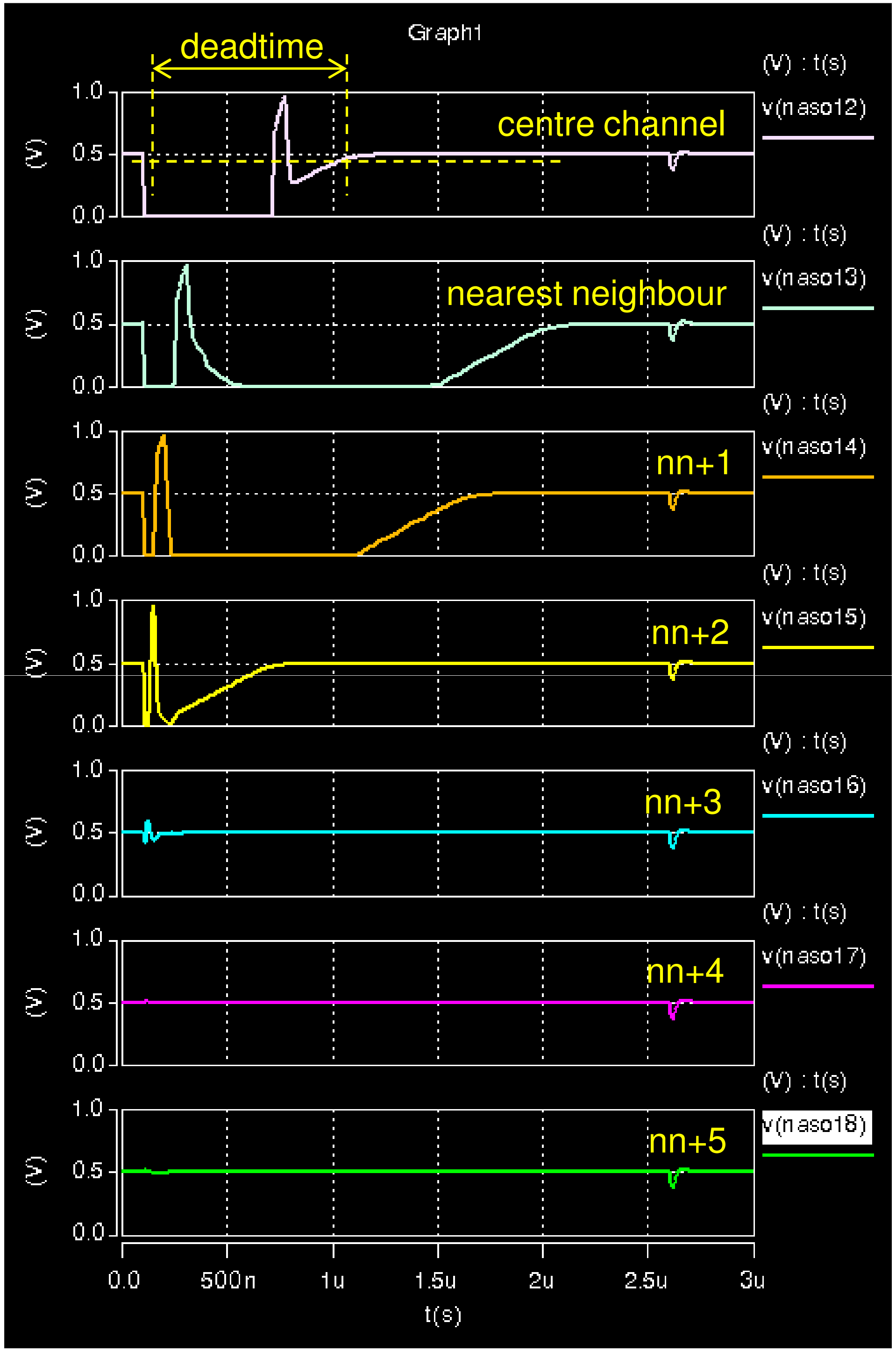
use this distribution to be conservative
but should be lower for thinner sensor

HIPs energy spectrum - M.Huhtinen simulations

Probability/incident pion of depositing energy E in 300µm Si layer



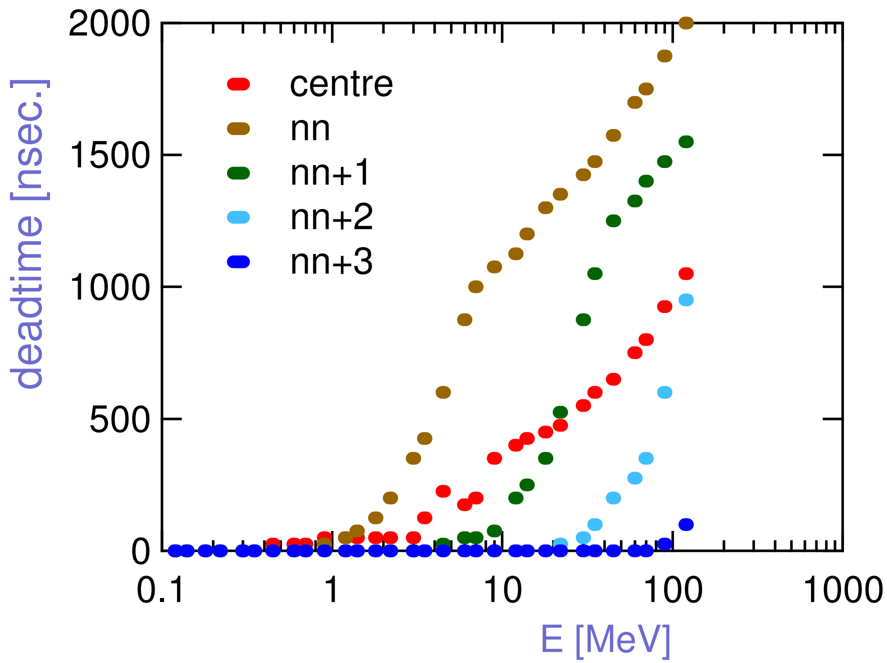
for calculations here, take numbers directly from graph



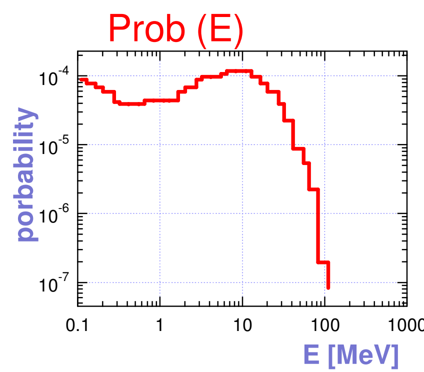
parameterizing hips deadtime

deadtime quantified (in simulation) by duration of saturation time

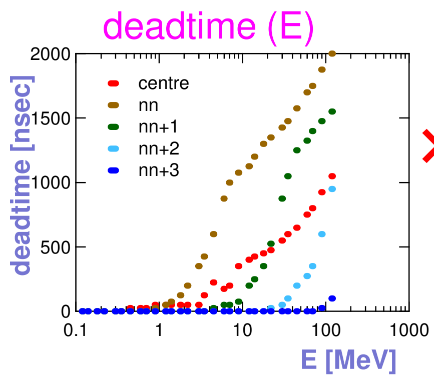
saturation taken to be signal over ~ 1fC threshold



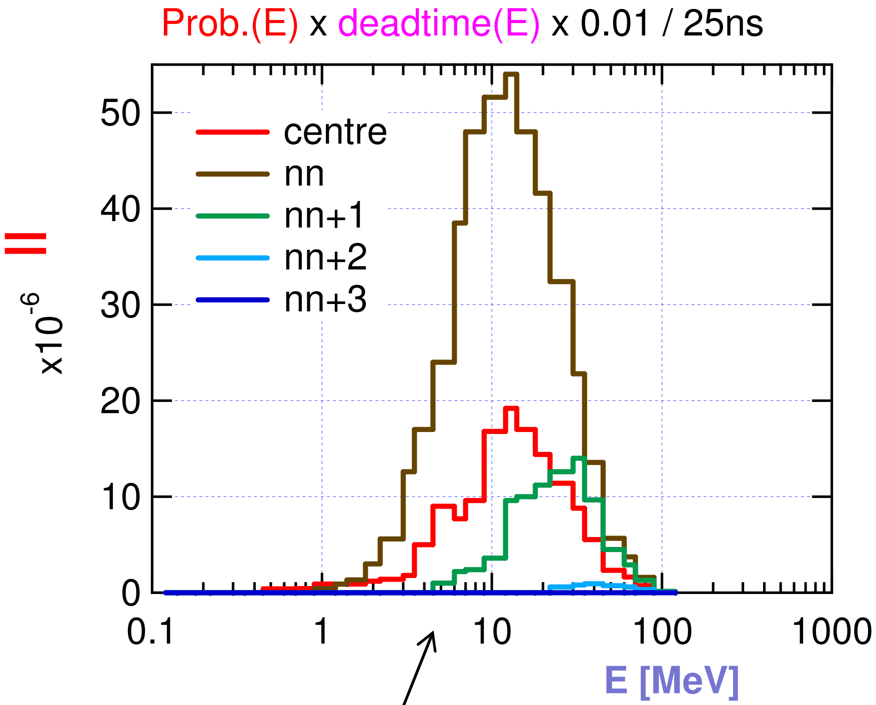
hit loss rate predictions - method



×



× $\frac{0.01}{25\text{ns}}$ =



fraction of time channel is dead (in BX's)
= prob. of particle interacting x occupancy
x deadtime (in BX's)

use 1%

sum bins to get
total hit loss probability

	Σbins	multiplier	result
centre	1.37e-4	x1	2.74e-4
NN	4.27e-4	x2	8.54e-4
NN+1	8.51e-5	x2	1.70e-4
NN+2	4.05e-6	x2	8.1e-6
NN+3	5.4e-9	x2	1.1e-8

1.31e-3

1.31×10^{-3} is probability of losing a single hit on a track because it has passed through a channel temporarily disabled due to a previously occurring HIPs event (in itself or neighbouring channels)

(remember that this is per % occupancy)

current thinking on LDO and powering

previous thoughts:

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_powering_June2015.pdf
http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_systems_July2015.pdf

discussed last time possibility to use PMOS based bandgap (Jan Kaplon)

more stable to radiation (ionizing and displacement)

but stronger process dependence
=> need mechanism to trim

possibility to use e-fuses to do this

also e-fuses can be used to provide unique chip identifier at wafer probe time

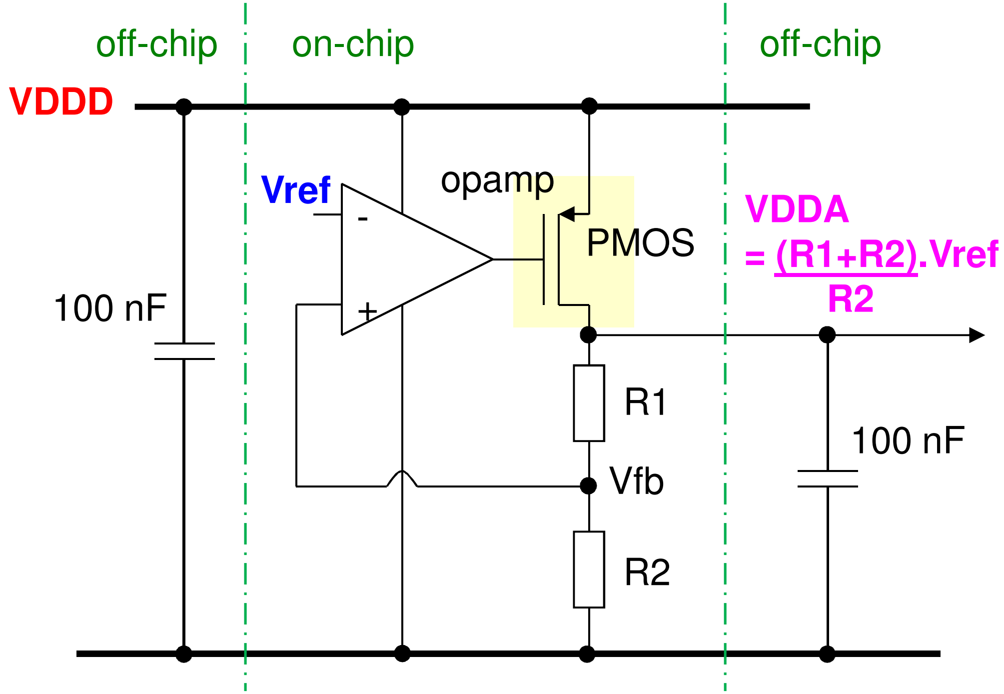
current thinking on LDO and powering

take Vref from PMOS bandgap

trim using I2C register (somehow)

use e-fuses to fix default value of
I2C register during wafer test

(note: default I2C value could be
overwritten later if so desired)



for example

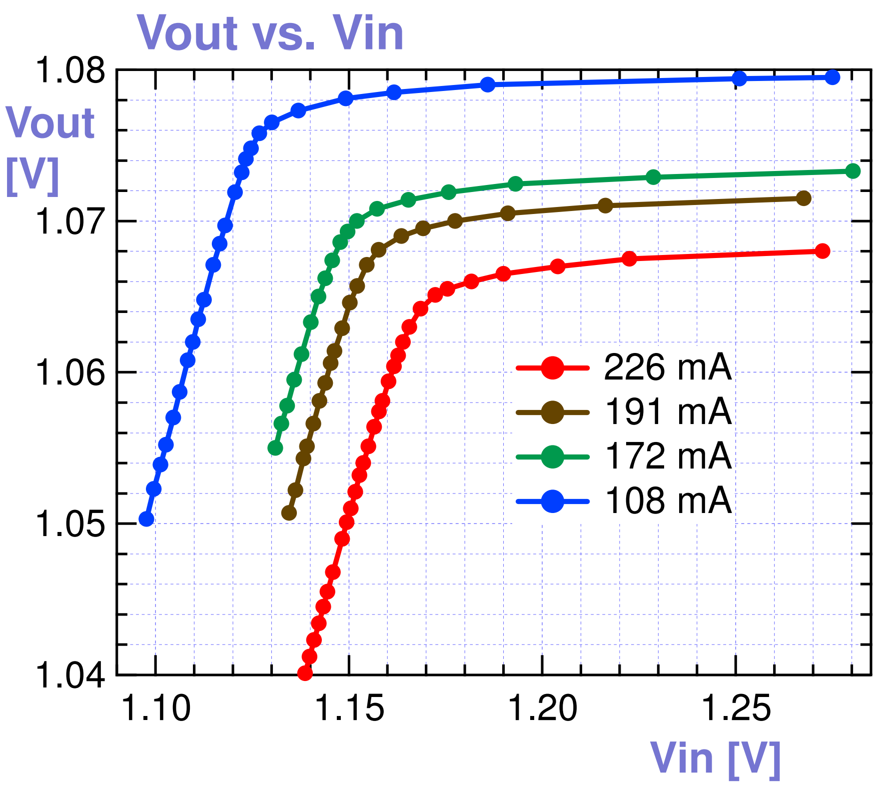
set LDO gain to 2

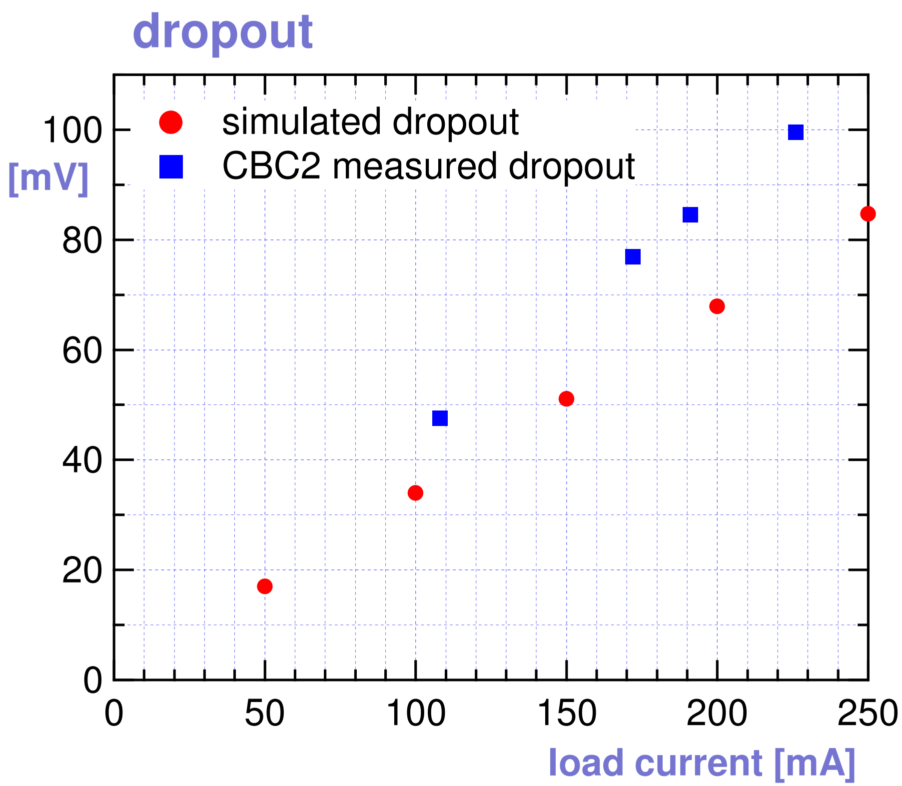
choose (trim) Vref to be 0.5

=> VDDA = 1.0 V

VDDD > 1.1 V allows 100mV headroom for LDO

CBC2 LDO measurements





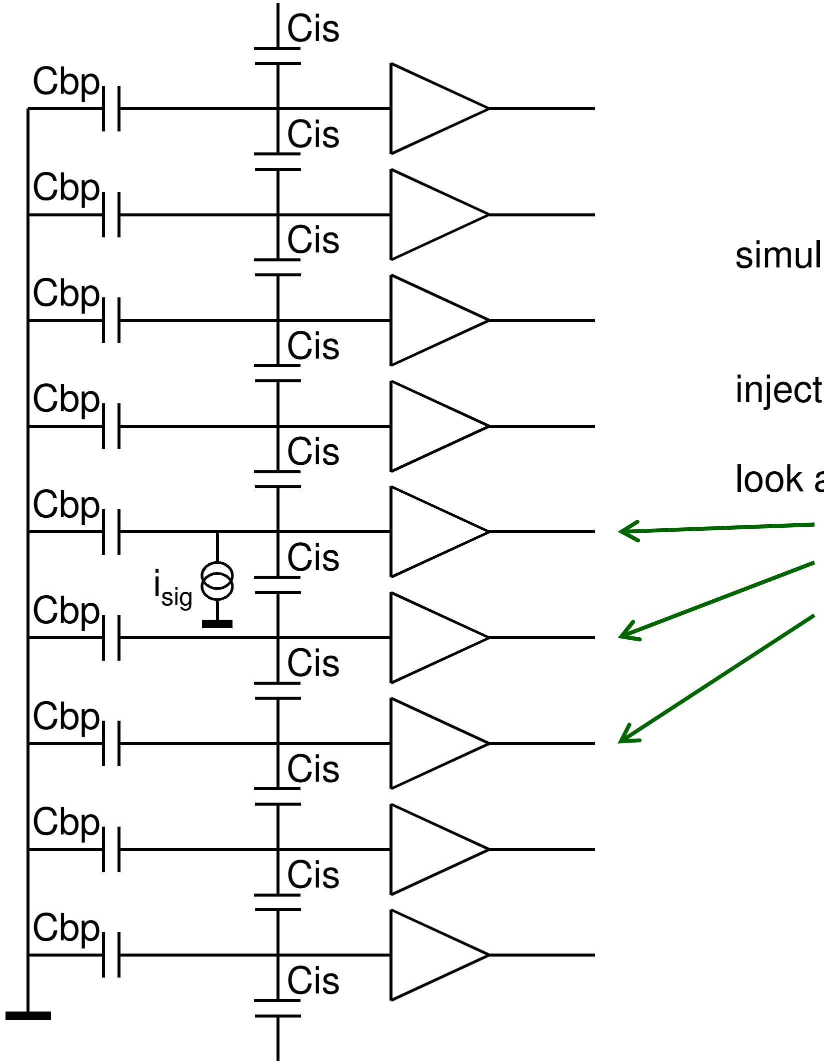
analogue current consumption
~ 300uA / chan. for 5 cm strips
=> ~80 mA / chip
=> ~40 mV dropout => plenty of headroom

analogue current consumption
~ 700uA / chan. for **8** cm strips
=> ~180 mA / chip
=> ~80 mV dropout => just enough headroom

=> no need to change core LDO design (only feedback resistor tweaks)

BACKUP

multi-channel behaviour



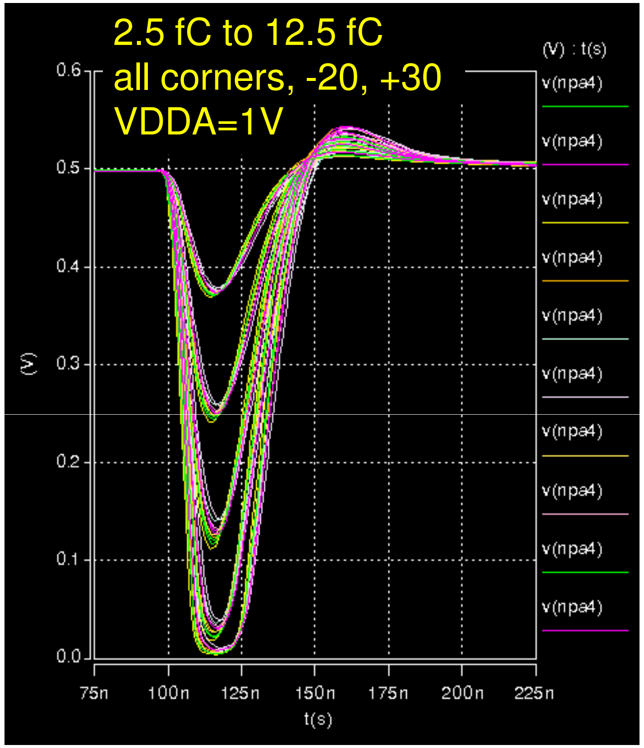
simulations here for Cis = 2.5pF, Cbp = 2pF, Cstray = 2pF
=> Ctot = 9 pF

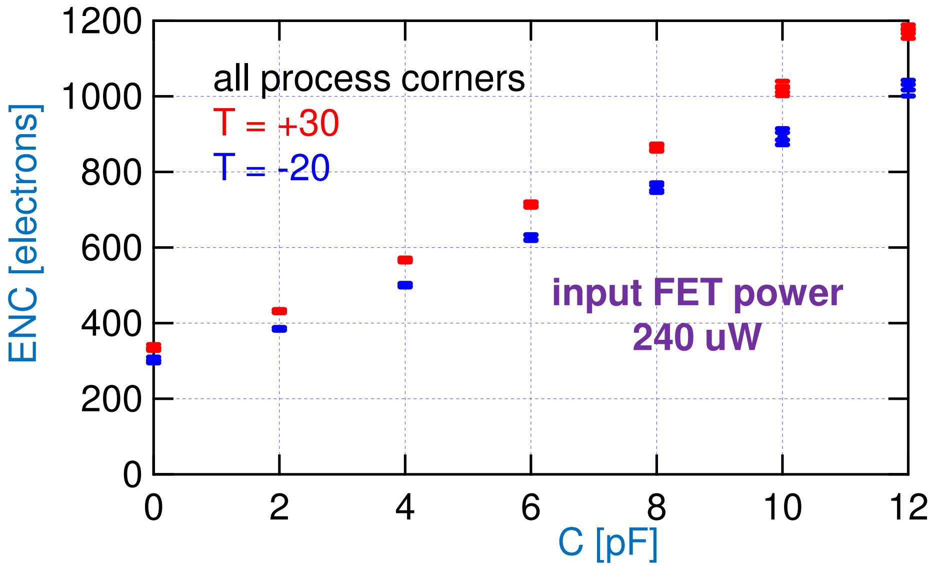
inject charge into central channel

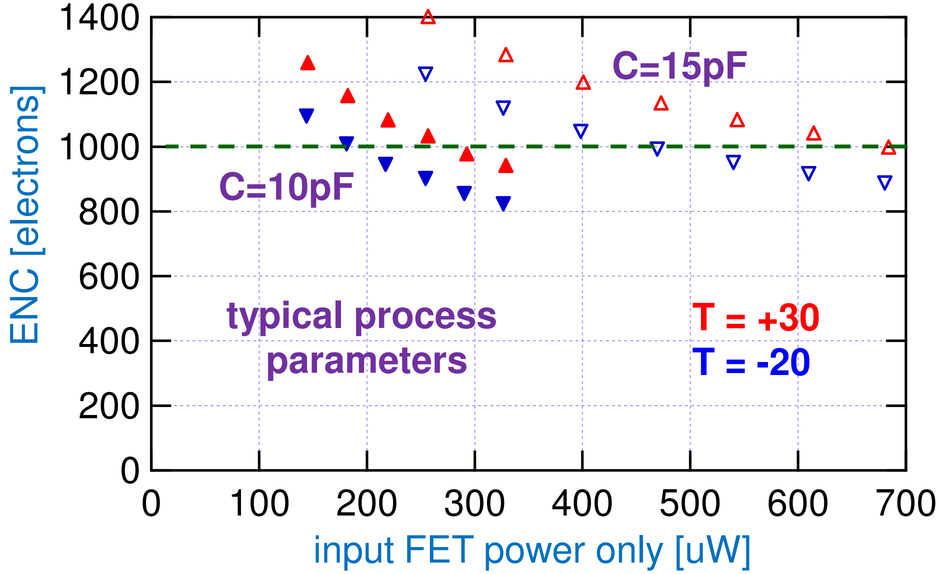
look at postamp output for
central channel
nearest neigbour,
nearest neighbour +1
….

CBC3 front end progress

details of changes to preamp/postamp circuits and performance shown last time*



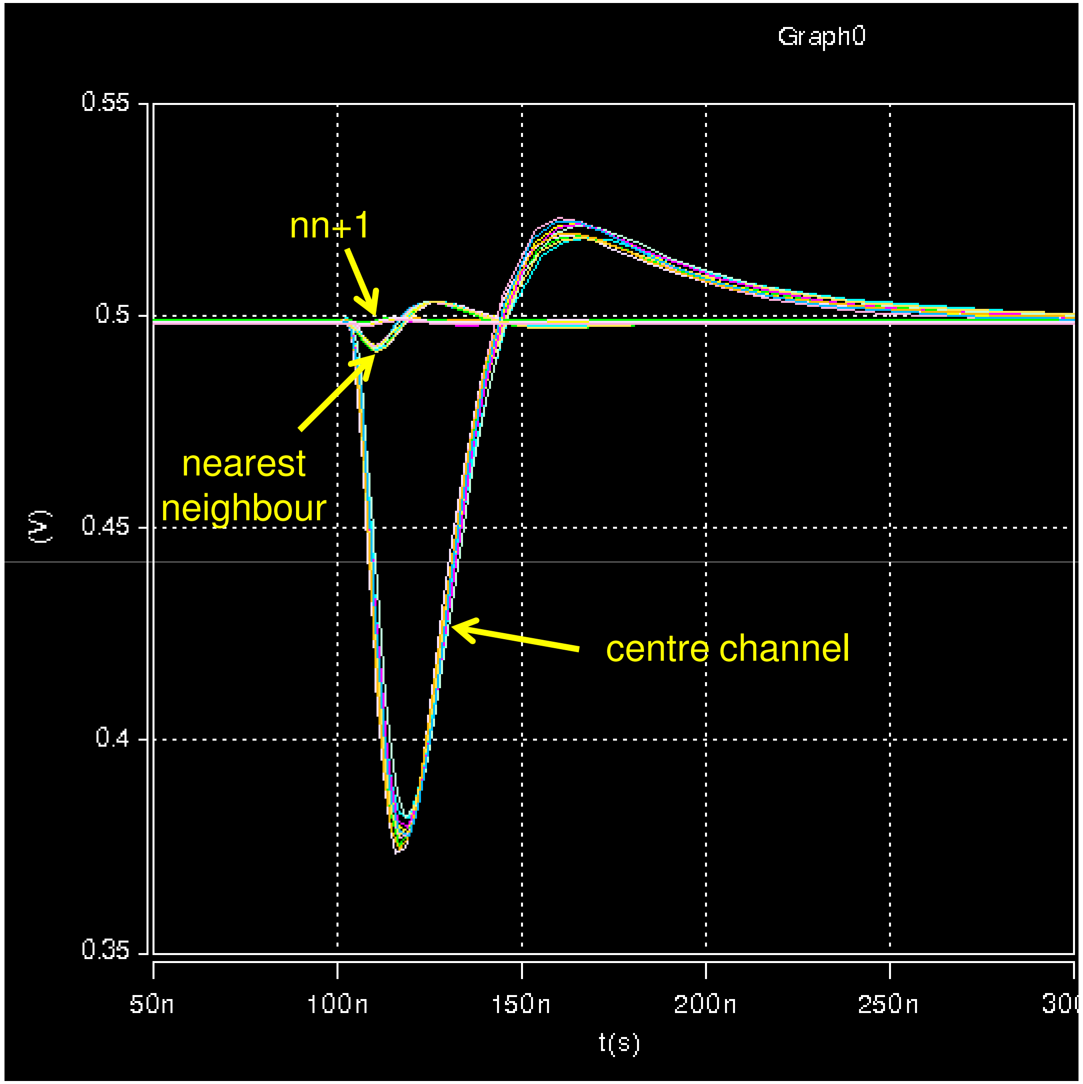




no time to present multi-channel and hips response simulations last time

* http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_FE_status_June2015.pdf

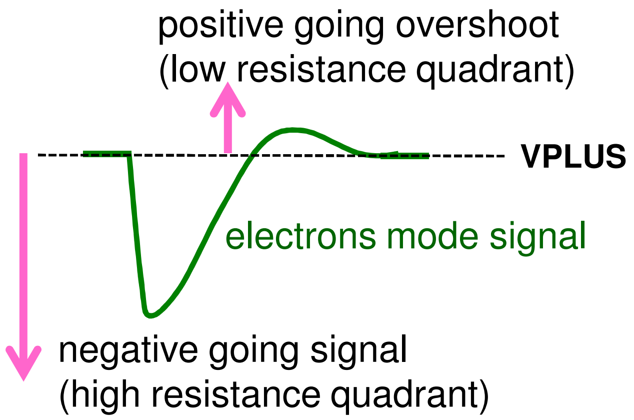
interstrip crosstalk

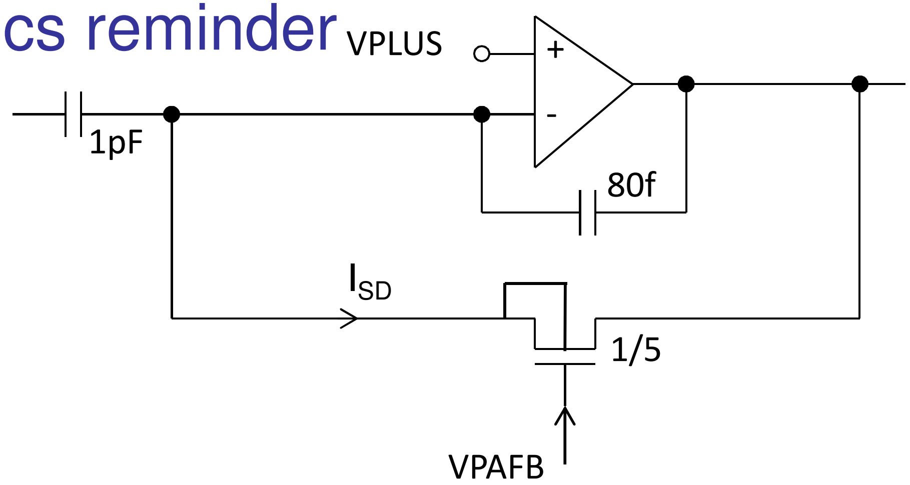


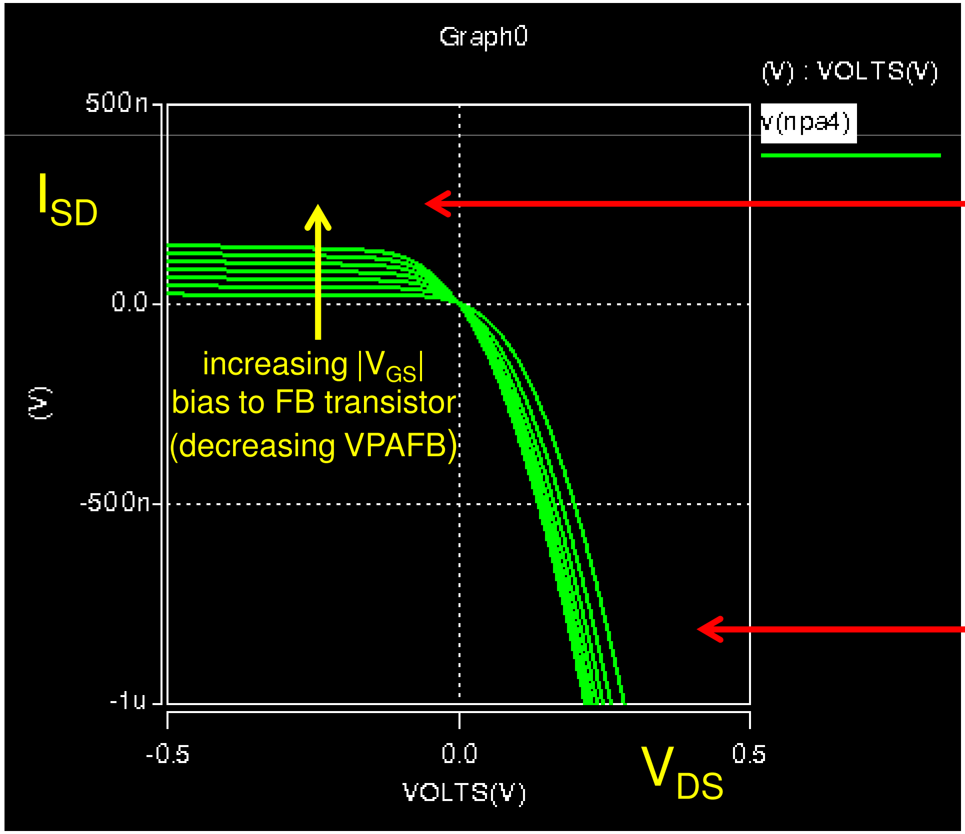
2.5 fC charge injected
T=-20/+30
all corners
nominal biases

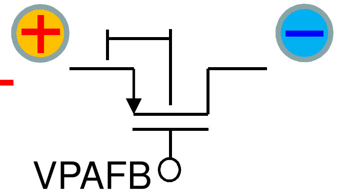
nearest neighbour peak
crosstalk ~ 5 %

postamp feedback characteristics reminder

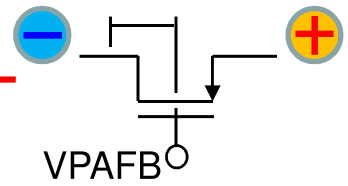






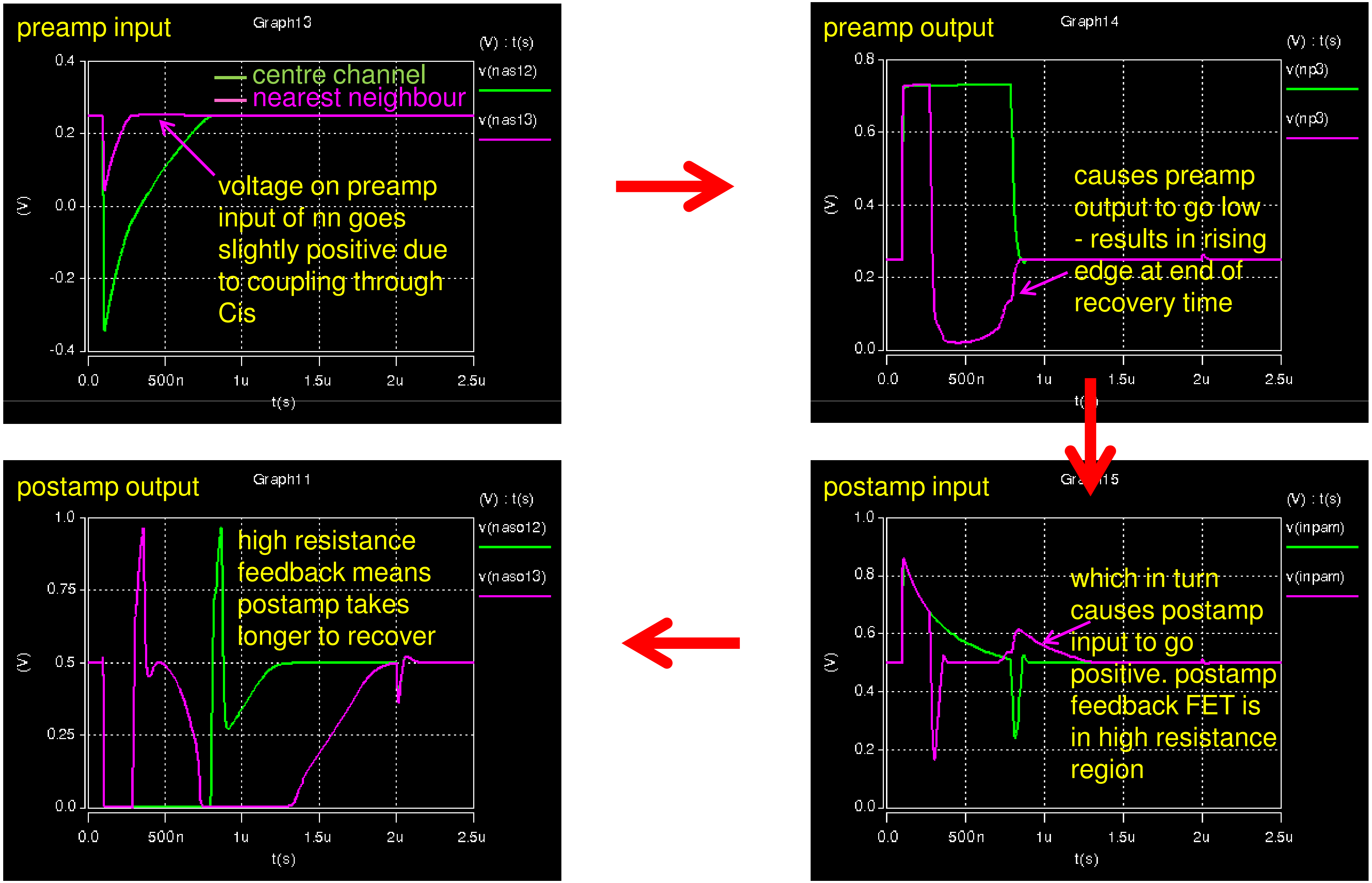


-ve going signal region
source at input side of postamp
V_{GS} ~ constant
only V_{DS} varies

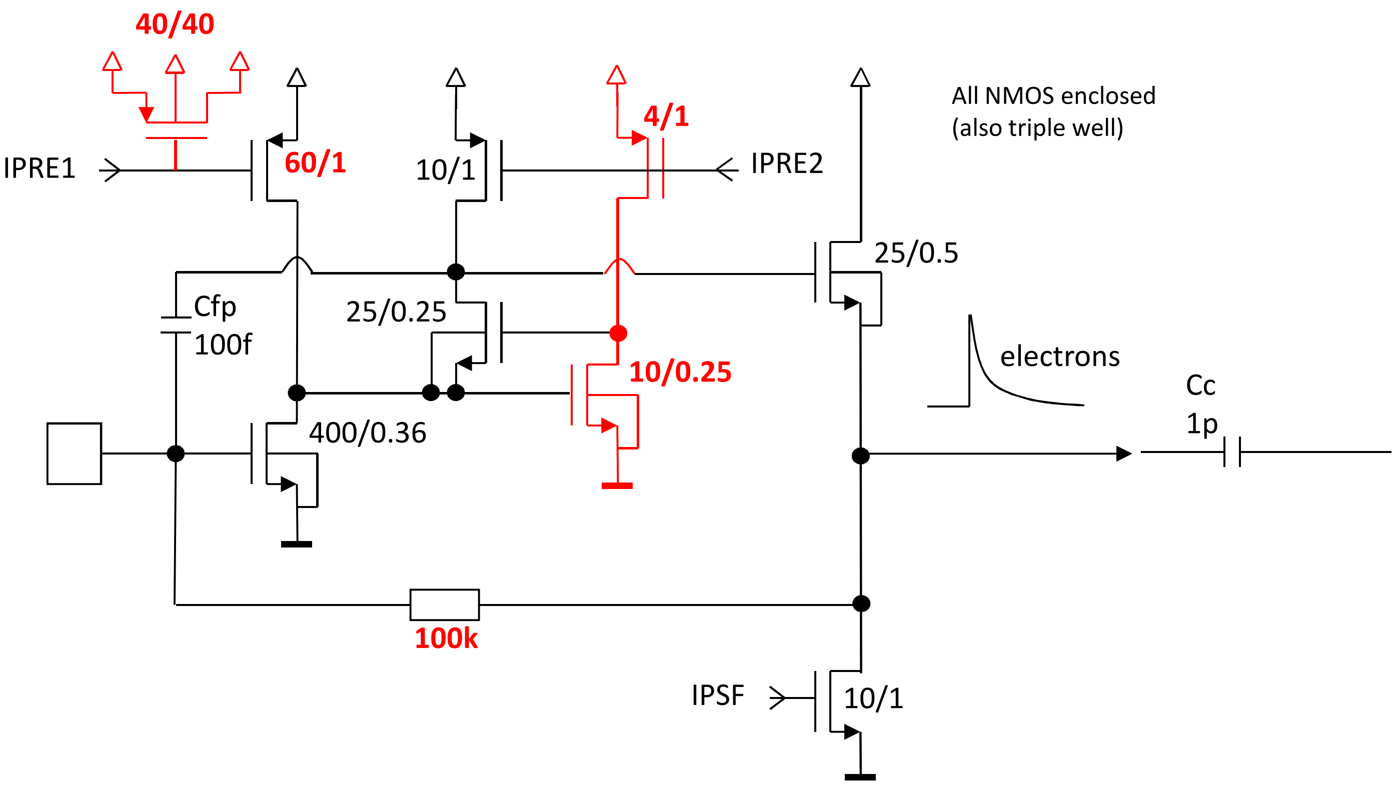


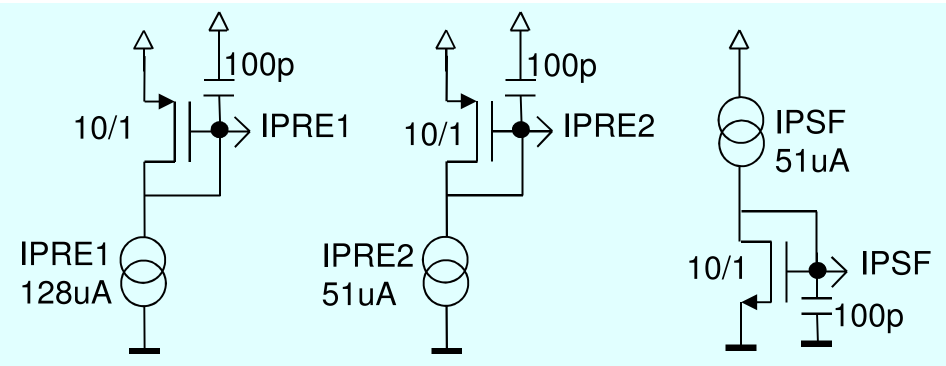
+ve going overshoot region
source swaps to output side
V_{GS} increases as postamp output overshoot increases

why is nearest neighbour hips deadtime worse than centre chan?

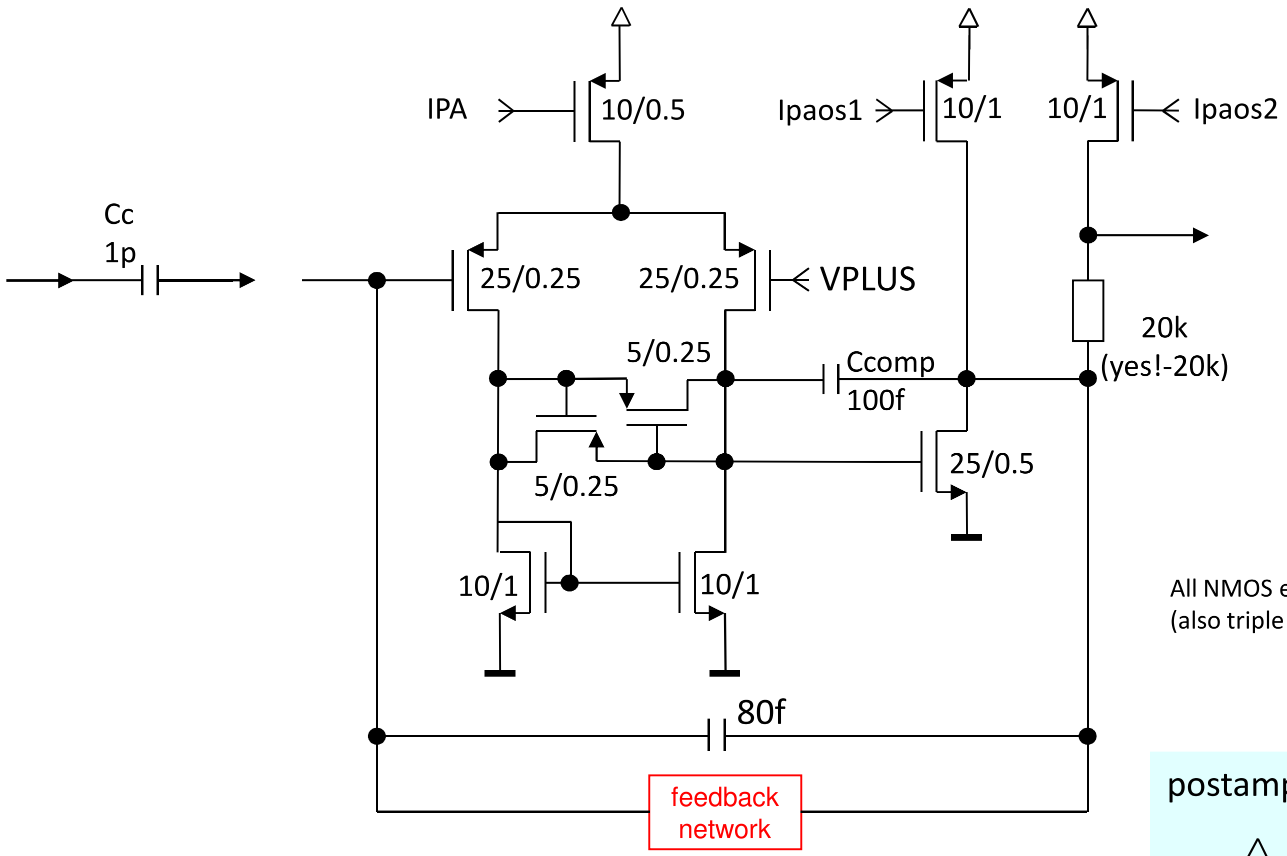


CBC3 Preamp with regulated cascode

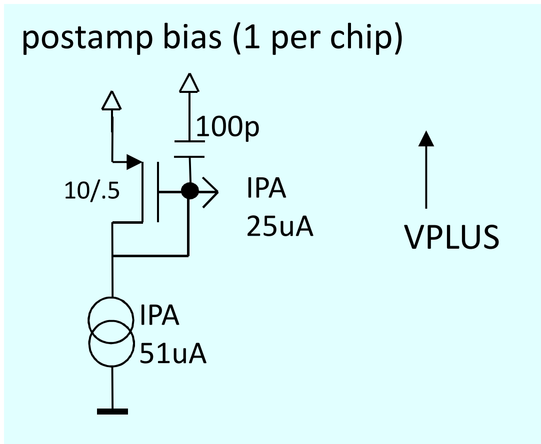




CBC3 Postamp



All NMOS enclosed
(also triple well)



CBC3 postamp feedback