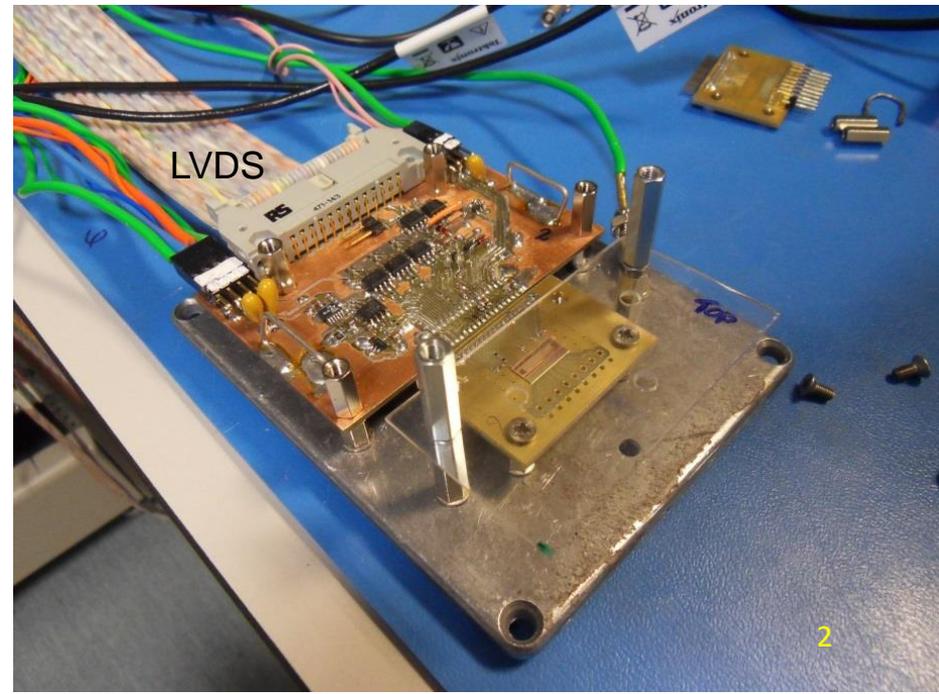
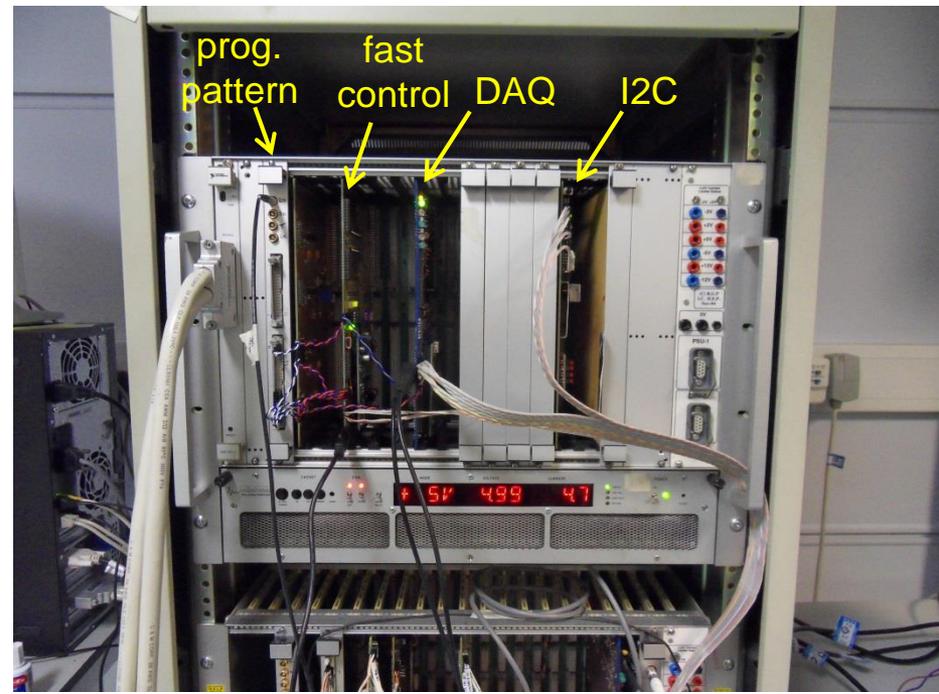
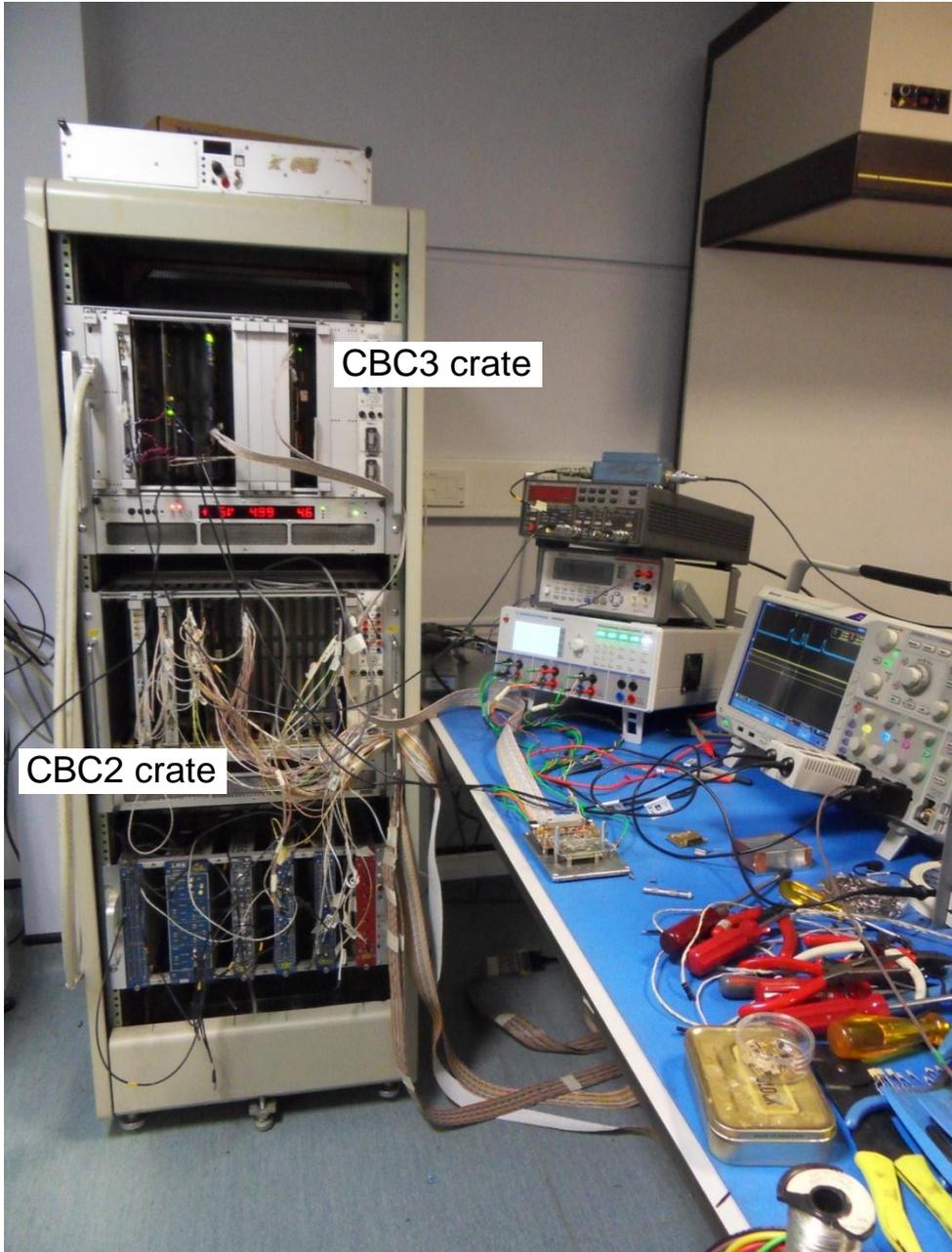


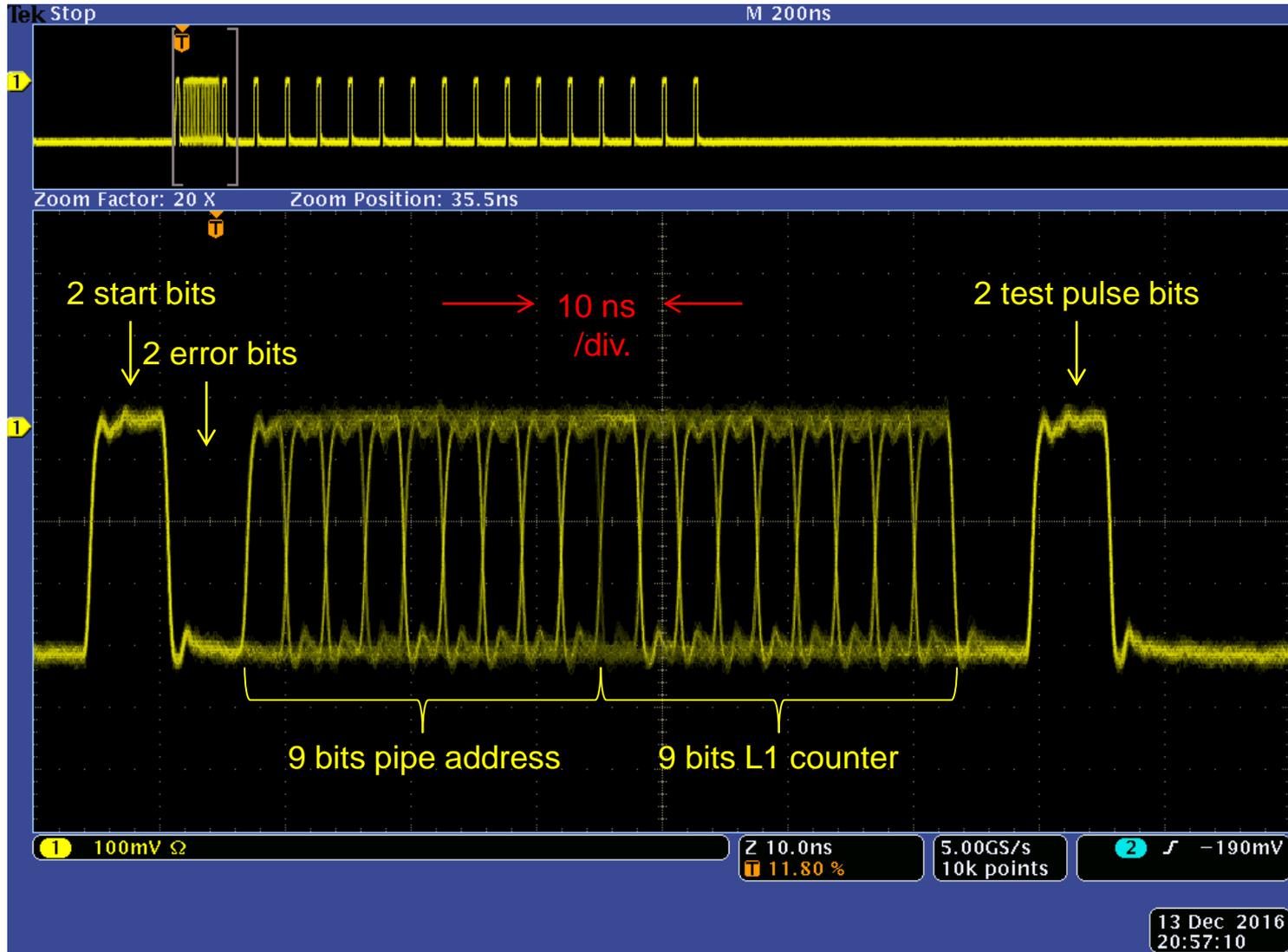
CBC3 first results

systems meeting, 16th December, 2016.

VME test setup



scope picture of L1 triggered data



differential probe close to chip output, scope on persistence

CBC3 I2C front panel

observations

“quite” complicated - more so than CBC2

relatively easy to get a bit set wrongly somewhere

GUI helps to spot incorrect setting

not just a list of addresses
& data values

The screenshot displays the CBC3 I2C front panel GUI. At the top, there are controls for 'write and readall' (YES), 'bus speed' (5), and 'status' (1101110). Below these are fields for 'CBC address (binary)' (b1011111) and 'I2C done' (1). An 'error out' window shows 'no error' and 'code 3600'. The main interface consists of a list of registers on the left, each with a dropdown menu (all set to 'NOP') and a value field. The registers include: FEC Register (page 1 fixed), Latency Register, beta multiplier & SLVS, IPRE1, IPRE2(CASC), IPSF, IPA, IPAOS, ICOMP, VPLUS/VPLUS2, HIP & Test Mode, TP Pot Node Select, TP Del & Test Chan Grp, TP Cntrl & Analogue Mux, CAL_I, CAL_VCASC, Pipe/Stub logic I/P select & Pt width, Coinc. Win. O/S 4 & 3, Coinc. Win. O/S 2 & 1, Layer Swap & Cluster Width, 40 MHz Clock & OR254, Fast CMD Interface & error flags, and VCTH. To the right of the registers are various control panels for 'Value to write', 'comparator hysteresis', 'Beta multiplier', 'SLVS current', 'discrepancy', 'Test Pulse amplitude', 'Analogue Mux Setting', 'Pt width', 'offset', 'Lswap', 'C Width', 'TPG Ck sel', 'Ck40 DLL', 'FCI delay', and 'Error Flags'. A green sphere icon is labeled 'discrepancy only valid if write and read all'. A legend for 'error flags meaning' is provided at the bottom: Buffer RAM overflow / Latency Error / Sync lost / Sync stat / Bad code. The VCTH register is highlighted in yellow, with its value field showing b1000 and b10.

other control panels

channel offsets

channel mask

bend LUTs

		0 = unmasked 1 = masked (inverted internally)									
		Array to write	Array read back								
8	7	6	5	4	3	2	1	b	11111111	b	0
16	15	14	13	12	11	10	9	b	11111111	b	0
24	23	22	21	20	19	18	17	b	11111111	b	0
32	31	30	29	28	27	26	25	b	11111111	b	0
40	39	38	37	36	35	34	33	b	11111111	b	0
48	47	46	45	44	43	42	41	b	11111111	b	0
56	55	54	53	52	51	50	49	b	0	b	11111111
64	63	62	61	60	59	58	57	b	0	b	11111111
72	71	70	69	68	67	66	65	b	0	b	11111111
80	79	78	77	76	75	74	73	b	0	b	11111111
88	87	86	85	84	83	82	81	b	0	b	11111111
96	95	94	93	92	91	90	89	b	0	b	11111111
104	103	102	101	100	99	98	97	b	0	b	11111111
112	111	110	109	108	107	106	105	b	11111111	b	0
120	119	118	117	116	115	114	113	b	11111111	b	0
128	127	126	125	124	123	122	121	b	11111111	b	0
136	135	134	133	132	131	130	129	b	11111111	b	0
144	143	142	141	140	139	138	137	b	11111111	b	0
152	151	150	149	148	147	146	145	b	11111111	b	0
160	159	158	157	156	155	154	153	b	11111111	b	0
168	167	166	165	164	163	162	161	b	11111111	b	0
176	175	174	173	172	171	170	169	b	11111111	b	0
184	183	182	181	180	179	178	177	b	11111111	b	0
192	191	190	189	188	187	186	185	b	11111111	b	0
200	199	198	197	196	195	194	193	b	11111111	b	0
208	207	206	205	204	203	202	201	b	11111111	b	0
216	215	214	213	212	211	210	209	b	11111111	b	0
224	223	222	221	220	219	218	217	b	11111111	b	0
232	231	230	229	228	227	226	225	b	11111111	b	0
240	239	238	237	236	235	234	233	b	11111111	b	0
248	247	246	245	244	243	242	241	b	11111111	b	5
-	-	254	253	252	251	250	249	b	11111111	b	11000000

FEC register automatically set to page 2 and then restored to original value

248	247	246	245	244	243	242	241	b	11111111	b	5
-	-	254	253	252	251	250	249	b	11111111	b	11000000

running the chip

many things to set up correctly

user manual will explain

draft exists - not ready for circulation yet

spec. document already goes some way

test pulse allows to exercise most features

same as CBC2 - arrangement of channels allows to generate stubs

can limit number of stubs generated using channel mask

write address: A000

accessparms: x1, width: d2

write and readall: YES, bus speed: 5

status: 1101110, I2C done: 1

error out: no error, code: 3600

milliseconds to wait: 0

Value to write: page, CompPol, Beta multiplier, SLVS current, discrepancy, Comparator Hysteresis, SLVS current

FEC Register (page 1 fixed): NOP, b1000000, 1, elecs, CH3, CH2, CH1, CH0, off, zero, b1000000, d64

Latency Register: NOP, d32, b100000, d32

beta multiplier & SLVS: NOP, b11000111, B3, B2, B1, B0, B3, B2, B1, B0, b11000111, d199

IPRE1: NOP, d50, b110010, d50

IPRE2(CASC): NOP, d120, b1111000, d120

IP5F: NOP, d130, b10000010, d130

IPA: NOP, d210, b11010010, d210

IPAOS: NOP, d20, b10100, d20

ICOMP: NOP, d90, b1011010, d90

VPLUS/VPLUS2: NOP, VPLUS: d7, VPLUS2: d7, combined: b1110111, b1110111, d119

HIP & Test Mode: NOP, count: d0, suppress: disabled, source: sampled, SLVS: ON, b1000, d8

TP Pot Node Select: NOP, b1100011, test pulse amplitude: 60, b1000011, d195

TP Del & Test Chan Grp: NOP, b111001, test pulse delay: 14, test chan group: 6, b110011, d115

TP Cntrl & Analogue Mux: NOP, b1100000, b1100000, d96

CAL_I: NOP, d240, b11110000, d240

CAL_VCASC: NOP, d63, b111111, d63

Pipe/Stub logic I/P select & Pt width: NOP, b1010111, Pipeline, Stub logic, b1010111, d87

Coinc. Win. O/S 4 & 3: NOP, b0, offset 4: 0, offset 3: 0, b0, d0

Coinc. Win. O/S 2 & 1: NOP, b0, offset 2: 0, offset 1: 0, b0, d0

Layer Swap & Cluster Width: NOP, b100, Lswap=0, C Width: 4, b100, d4

40 MHz Clock & OR254: NOP, b10010000, TPG Ck sel: EN_OR254, 1 = normal, OFF, OFF, Ck40 DLL: 1, b10010000, d144

Fast CMD Interface & error flags: NOP, b0, FCI delay: 0, Error Flags: b0, d0

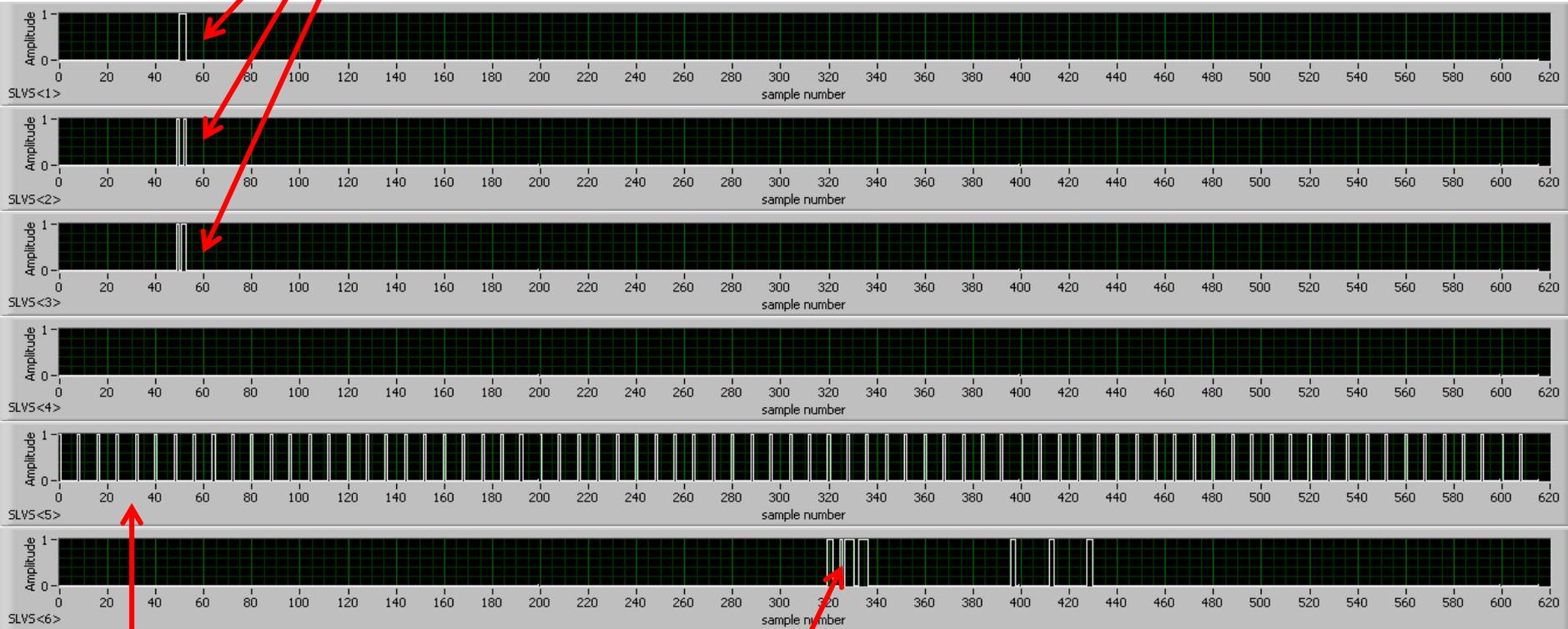
VCTH: NOP, b1000, VCTH 2: 520, VCTH read back: b1000, d8

error flags meaning: Buffer RAM overflow / Latency Error / Sync lost / Sync stat / Bad code

running the chip example

example here shows activity on 6 output lines for 3 stubs generated

SLVS<1>, <2> & <3> shows stub address data



SLVS<5> shows sync pulse every 25 nsec

SLVS<6> shows digital header followed by 3 pairs of hits

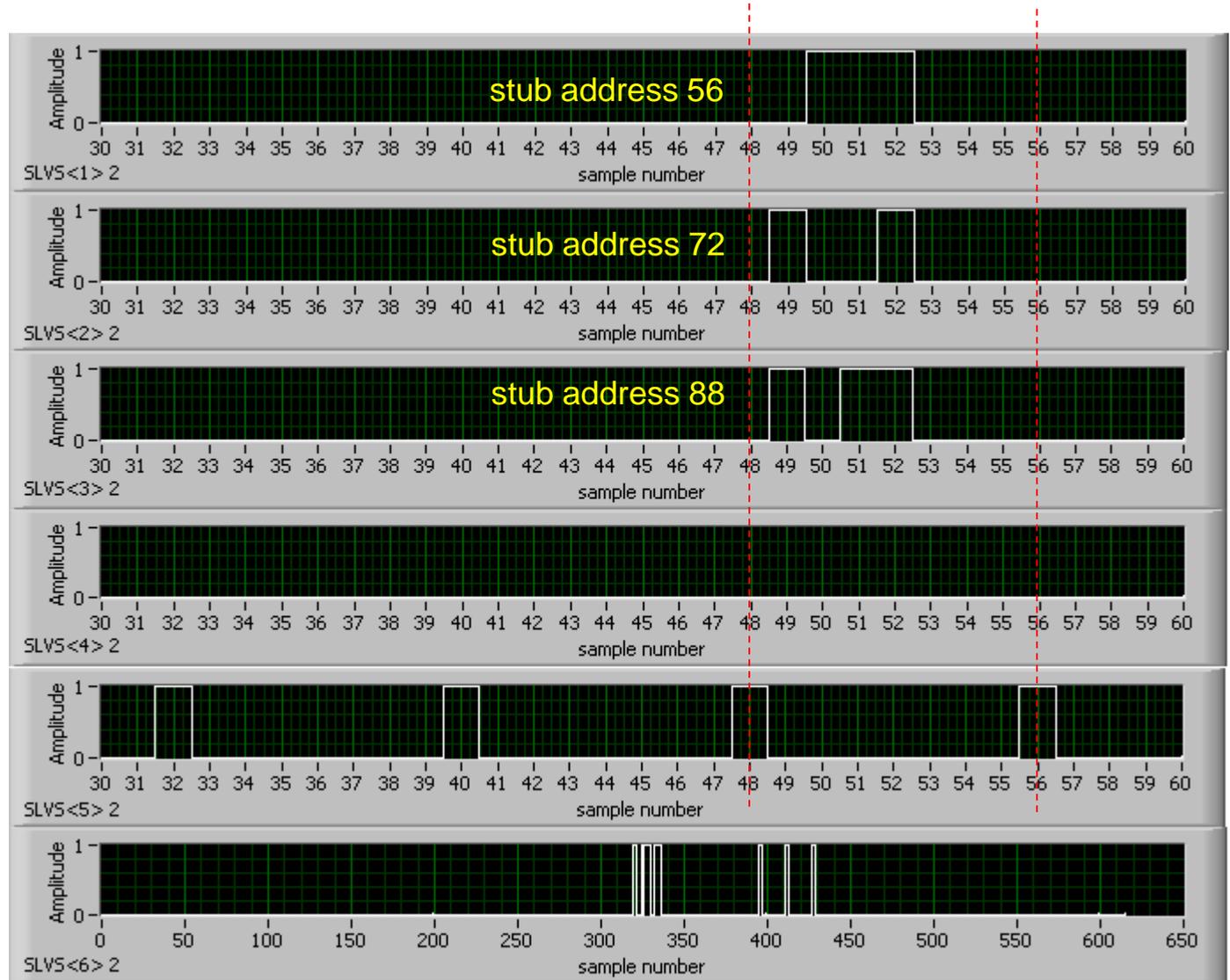
note: no bend information, because test pulse fires channels directly above each other (seed channel and channel in centre of window => bend = 0)

zooming in

test pulse timing set up so that hit confined to one timeslot

stub addresses 16 channels apart as expected from test pulse

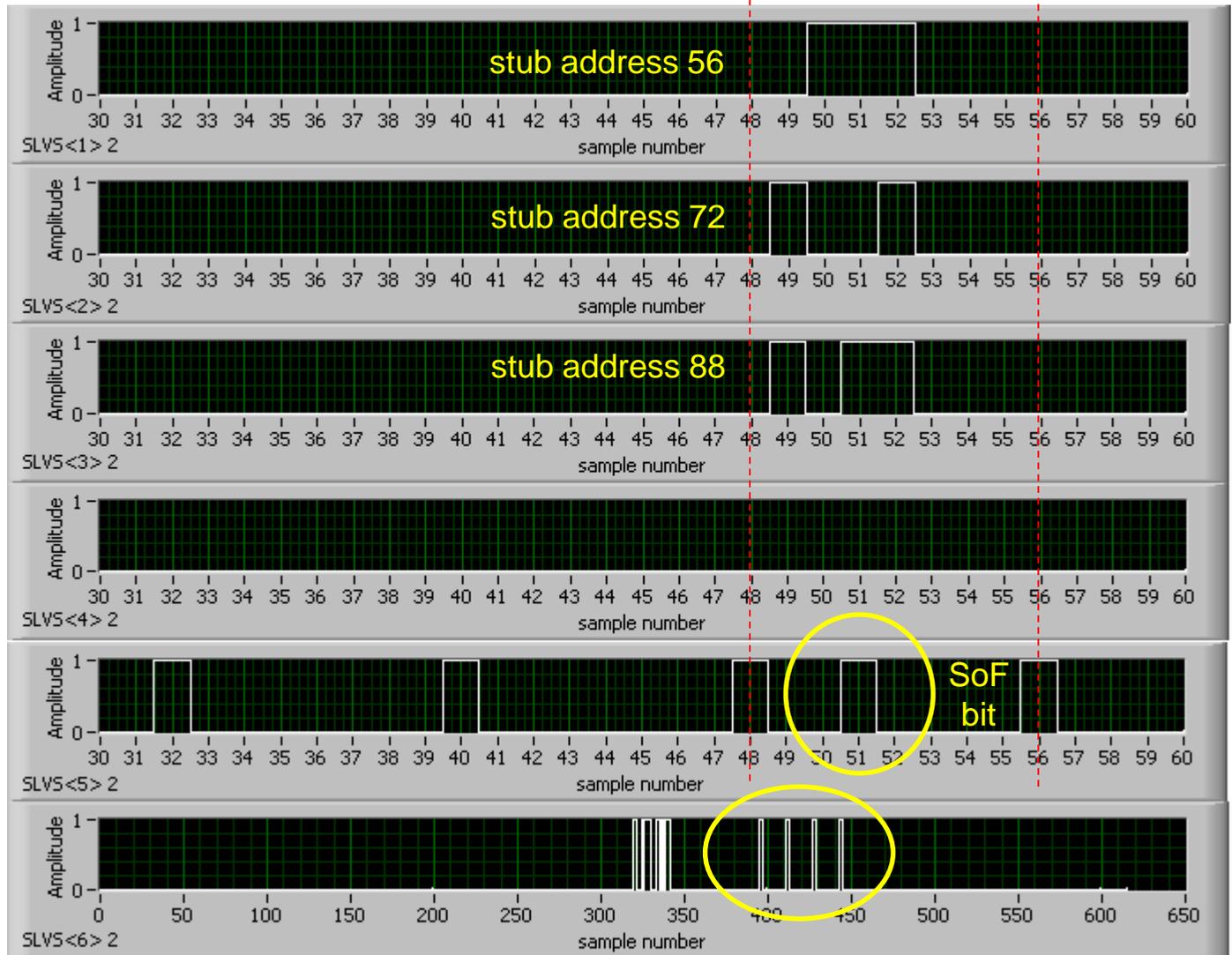
only get even stub addresses as odd values require adjacent hits on the same layer (test pulse can't do that)



now unmask another pair of channels to generate a 4th stub

4 stubs

stub overflow bit set in SLVS<5>

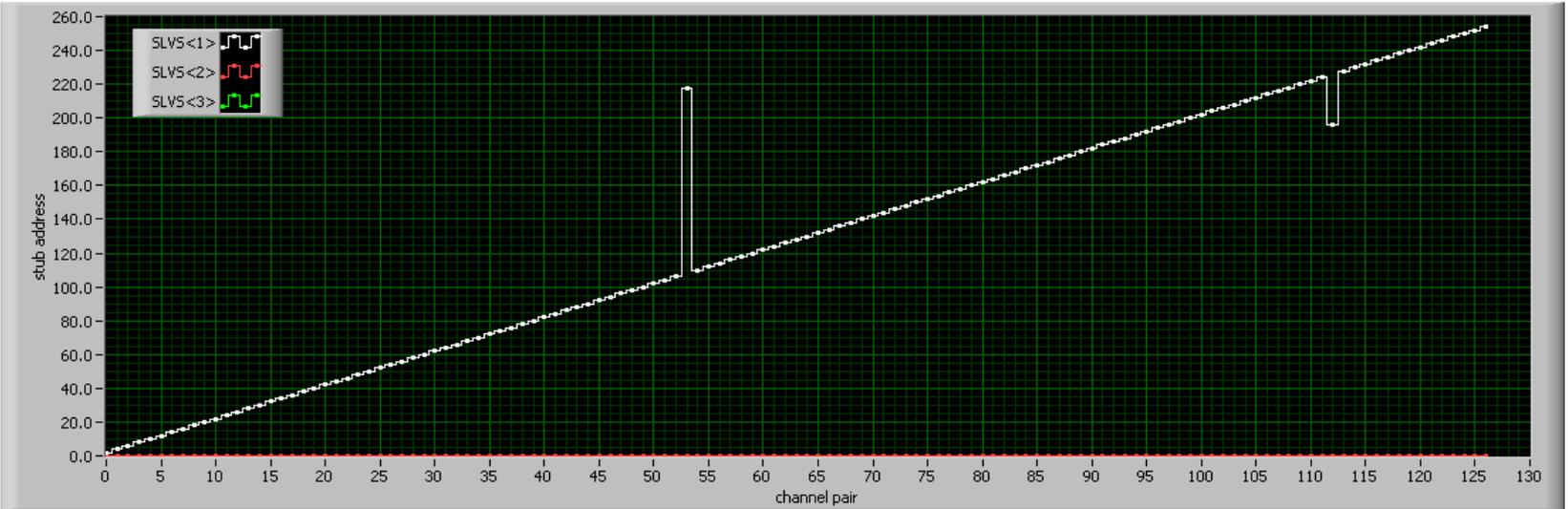


4 pairs of channels
in triggered data stream

everything appears to be working - can programmatically sweep test pulse through all channels and check to see all stub addresses present

sweep single stub through all channels

Waveform Graph 7



stub address
generated
by chip

channel pair fired by test pulse (127 channel pairs altogether)

stub address sweeps between 2 and 254

2 stub addresses not correct

get 218 instead of 106

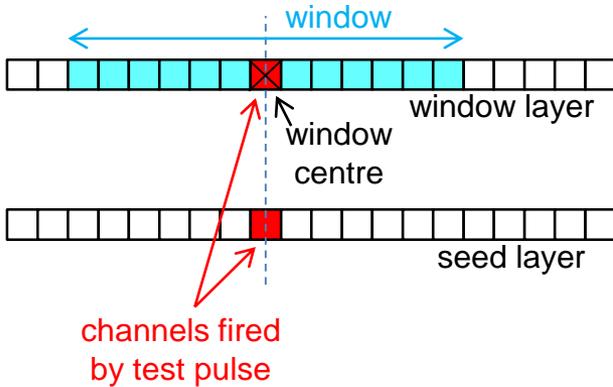
196 instead of 226

=> get address 218 and 196 twice

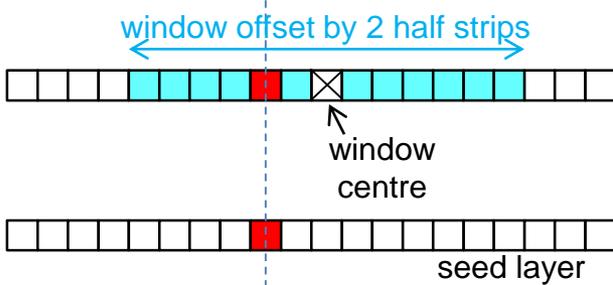
can also get bend info

test pulse fires seed layer channel and window layer channel immediately above

=> bend value 0 should be returned if no offset applied



but can change bend value by offsetting window



should see non-zero bend value

Screenshot of a control panel for a test pulse. The 'offset 4' and 'offset 2' fields are circled in red. The 'discrepancy' section shows a green sphere and text: 'discrepancy only valid if write and read all', 'Comparator Hysteresis 1111 = minimum', 'SLVS current 0000 = maximum'. Other fields include 'write address', 'write and readall', 'bus speed', 'status', 'error out', 'FEC Register', 'Latency Register', 'beta multiplier & SLVS', 'IPRE1', 'IPRE2(CASC)', 'IPSF', 'IPA', 'IPAOS', 'ICOMP', 'VPLUS/VPLUS2', 'HIP & Test Mode', 'TP Pot Node Select', 'TP Del & Test Chan Grp', 'TP Cntrl & Analogue Mux', 'CAL_I', 'CAL_VCASC', 'Pipe/Stub logic I/P select & Pt width', 'Coinc. Win. O/S 4 & 3', 'Coinc. Win. O/S 2 & 1', 'Layer Swap & Cluster Width', '40 MHz Clock & OR254', 'Fast CMD Interface & error flags', 'VCTH', 'VCTH 2', 'VCTH read back', 'error flags meaning: Buffer RAM overflow / Latency Error / Sync lost / Sync stat / Bad code'.

choose window offsets appropriately

for example to see bend values of

0, 1, 2, 3 (decimal)

program window offsets to

0, 14, 12, 10



desired offset [strips]	value to program [decimal]	bend value expected for test pulse hits [binary]
-3	6	1101
-2½	5	1101
-2	4	1110
-1½	3	1110
-1	2	1111
-½	1	1111
0 (centre)	0	0000 (0)
+½	15	0000
+1	14	0001 (1)
+1½	13	0001
+2	12	0010 (2)
+2½	11	0010
+3	10	0011 (3)

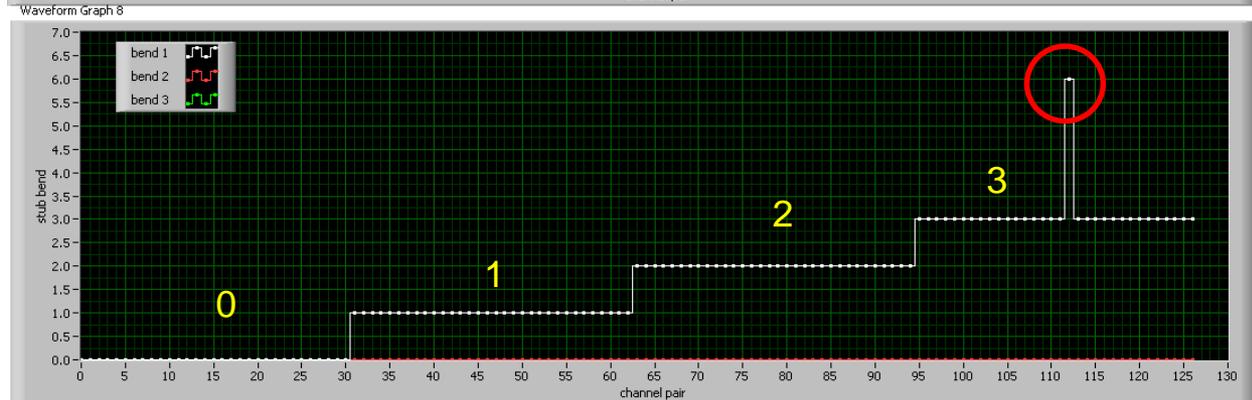
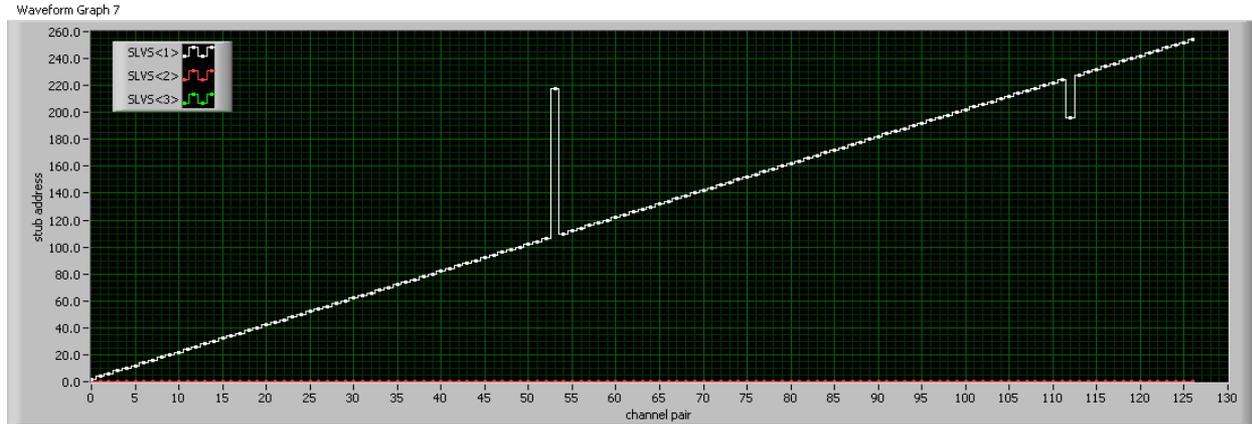
sweep stub again

sweeping single stub through
all channel pair locations

see 4 groups of channels
with expected bend values

but one channel not returning
expected bend value

same channel that also returns
incorrect stub address



31 chans

32 chans

32 chans

32 chans

explanation of incorrect stub addresses & bend

- Verilog code for the Stub Gathering Logic has some typos that slipped through the checking process.

Extra 1 appended to 7-bit address, so truncation occurs

```
assign Stub_Info_52_Half_int = {7'b0110100, 1'b1, Bend[259:255]};
wire [12:0] Stub_Info_53_int;
assign Stub_Info_53_int = {7'b0110101, 1'b0, Bend[264:260]};
wire [12:0] Stub_Info_53_Half_int;
assign Stub_Info_53_Half_int = {7'b0110101, 1'b1, Bend[264:260]};
wire [12:0] Stub_Info_54_int;
assign Stub_Info_54_int = {7'b01101101, 1'b0, Bend[269:265]};
wire [12:0] Stub_Info_54_Half_int;
assign Stub_Info_54_Half_int = {7'b0110110, 1'b1, Bend[269:265]};
wire [12:0] Stub_Info_55_int;
```

```
wire [12:0] Stub_Info_111_int;
assign Stub_Info_111_int = {7'b1101111, 1'b0, Bend[554:550]};
wire [12:0] Stub_Info_111_Half_int;
assign Stub_Info_111_Half_int = {7'b1101111, 1'b1, Bend[554:550]};
wire [12:0] Stub_Info_112_int;
assign Stub_Info_112_int = {7'b1110000, 1'b0, Bend[559:555]};
wire [12:0] Stub_Info_112_Half_int;
assign Stub_Info_112_Half_int = {7'b1110000, 1'b1, Bend[559:555]};
wire [12:0] Stub_Info_113_int;
assign Stub_Info_113_int = {7'b1110001, 1'b0, Bend[564:559]};
wire [12:0] Stub_Info_113_Half_int;
assign Stub_Info_113_Half_int = {7'b1110001, 1'b1, Bend[564:559]};
wire [12:0] Stub_Info_114_int;
assign Stub_Info_114_int = {7'b1110010, 1'b0, Bend[569:565]};
wire [12:0] Stub_Info_114_Half_int;
```

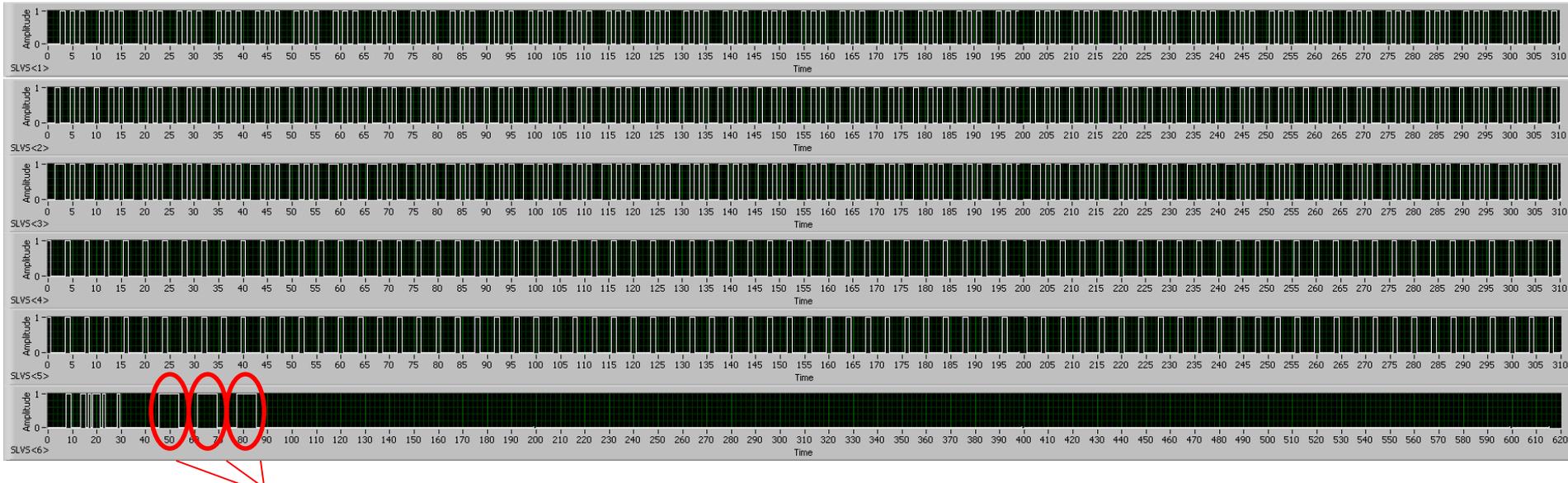
Should have been Bend [564:560]

- These channels can be masked on the existing chips and if necessary/desirable the issue can be corrected with a metal-mask-only change.
- We will review how this occurred and tighten-up our procedures to prevent future occurrences.

force continuous stub generation

set VCTH threshold so all channels constantly firing

selectively unmask channels to generate clusters



3 x 4 strip seed and window clusters

can use this technique to generate fixed pattern in SLVS output lines
also to verify cluster width discrimination logic, Pt window width logic, layer swap, ...
(principle proven - exhaustive check not yet implemented)

Ck40 test

can switch output of DLL to a test pad

test feature only - to verify DLL performance

for normal operation leave OFF

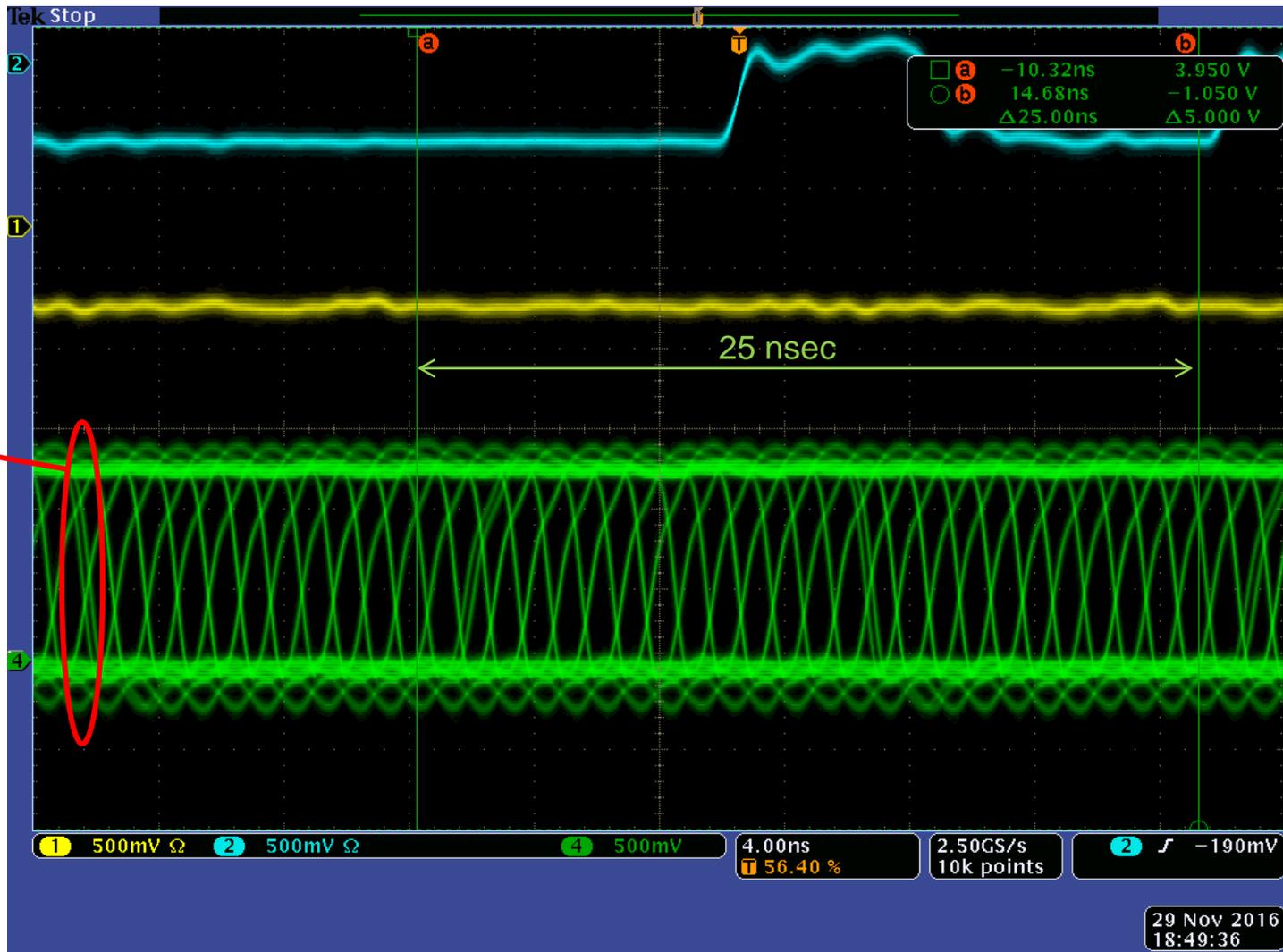
write and readall YES bus speed 5 status 1101110
CBC address (binary) b1011111 10xxxxx I2C done 1
error out status code no error 3600 source
milliseconds to wait 0 Value to write comparator hysteresis min hysteresis = buttons out beta M reset MSB Value read back decimal value
page CompPol
FEC Register(page 1 fixed) NOP b1000000 1 elecs CH3 CH2 CH1 CH0 off zero b1000000 64
Latency Register NOP d32 Beta multiplier SLVS current b100000 d32
beta multiplier & SLVS NOP b10000111 B3 B2 B1 B0 B3 B2 B1 B0 b10000111 d135
IPRE1 NOP d50 discrepancy b110010 d50
IPRE2(CASC) NOP d120 Comparator Hysteresis 1111 = minimum b1110000 d120
IPSF NOP d130 SLVS current 0000 = maximum b10000010 d130
IPA NOP d210 discrepancy only valid if write and read all b11010010 d210
IPAOS NOP d20 b10100 b20
ICOMP NOP d90 b1011010 d90
VPLUS/VPLUS2 NOP VPLUS d7 VPLUS2 d7 combined b1110111 b1110111 d119
HIP & Test Mode NOP count d0 suppress disabled source sampled SLVS ON b1000 d8
Test Pulse amplitude
TP Pot Node Select NOP b10110111 72 b10110111 d183
TP Del & Test Chan Grp NOP b11100000 test pulse delay 7 test chan group 0 b11100000 d224
TP Cntrl & Analogue Mux NOP b1100000 elecs En Gnd 0 Analogue Mux Setting b1100000 d96
4 3 2 1 0 nowt
CAL_I NOP d240 b11110000 d240
CAL_VCASC NOP d63 b1111111 d63
00 = sampled
11 = fixed pulse width
01 = OR of above
10 = HIP suppressed Pt width
Pipe/Stub logic I/P select & Pt width NOP b11 B1 B0 B1 B0 B3 B2 B1 B0 b11 d3
Pipeline Stub logic
Coinc. Win. O/S 4 & 3 NOP b11111111 offset 4 15 offset 3 15 b11111111 d255
Coinc. Win. O/S 2 & 1 NOP b11111111 offset 2 15 offset 1 15 b11111111 d255
Layer Swap & Cluster Width NOP b100 Lswap=0 C Width 4 b100 d4
40 MHz Clock & OR254 NOP b10110011 1 = normal OFF ON Ck40 DLL 25 b10110011 d179
Ck40 test 0=bypass
Fast CMD Interface & error flags NOP b0 FCI delay 0 Error Flags b0 d0
error flags meaning: Buffer RAM overflow / Latency Error / Sync lost / Sync stat / Bad code
VCTH NOP b1000 VCTH 2 520 VCTH read back b1000 d8
b10 d2

Ck40 test

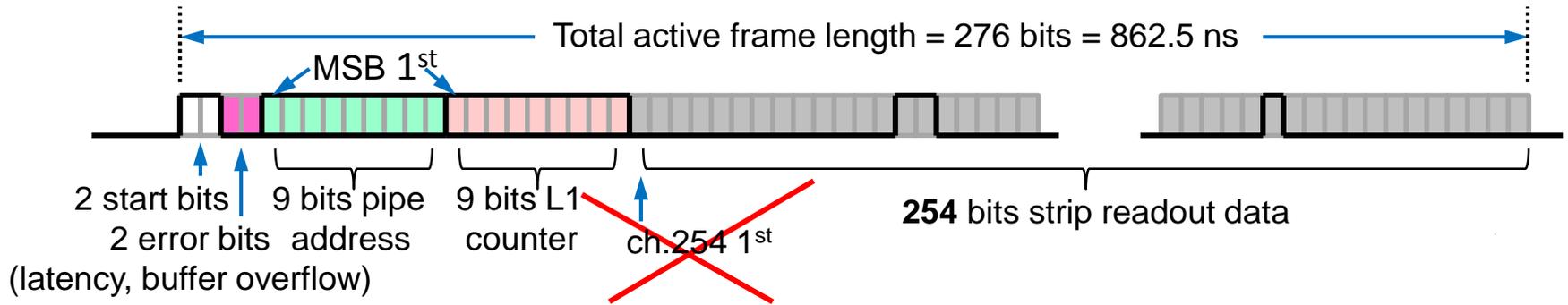
scope on infinite persistence

select Ck40DLL taps one at a time

small difference between 25 nsec delay and bypass due to different signal path lengths



deviation from specification



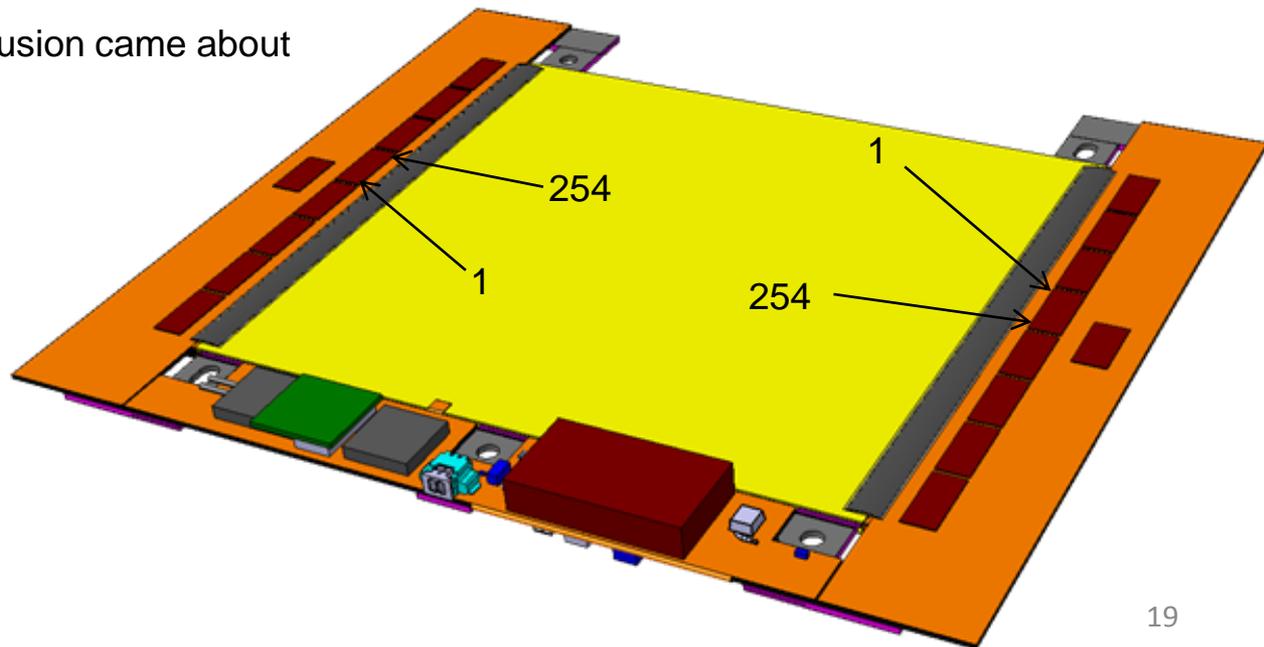
specification says channel 254 first

chip **actually** produces channel 1 first (same as CBC2)

not clear to me how this confusion came about

is it a big problem? (for CIC)

can we just modify spec.?



conclusions on digital functionality so far

chip is working well

a few bugs (that will have to be fixed) but nothing disastrous

plenty left to test ...

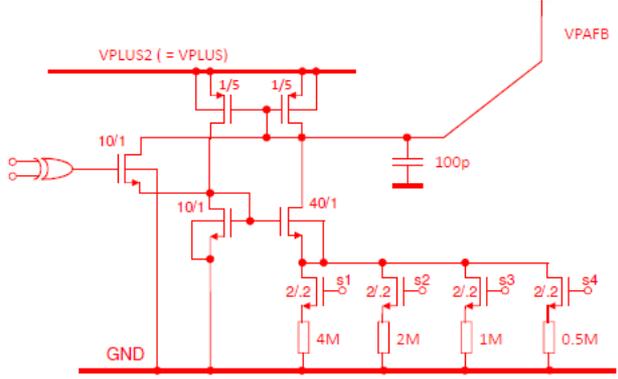
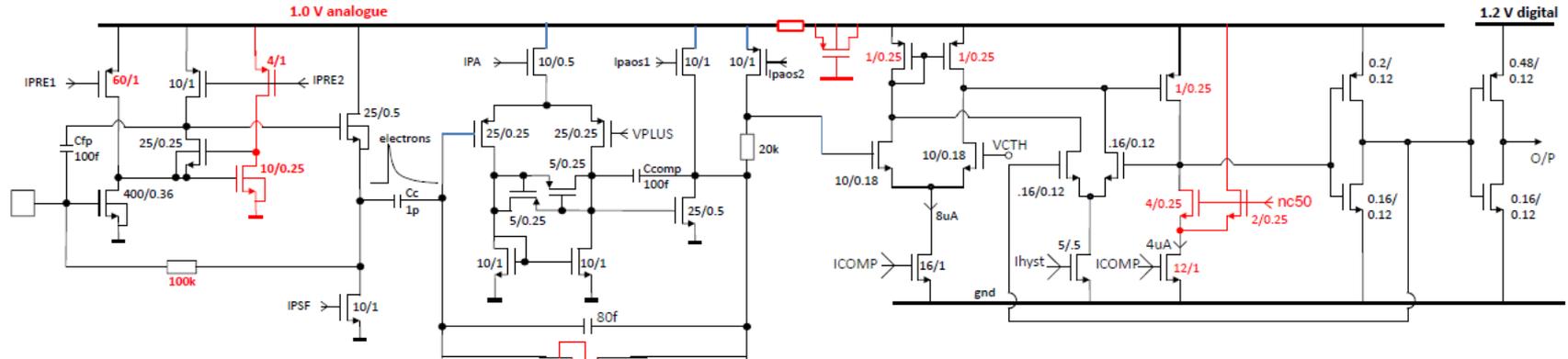
move now onto some analogue results

main analogue changes from CBC2

provision to run more current in input device if required

new preamp cascode bias scheme to eliminate "shadow effect"

pre & postamp polarity switch options removed



new postamp feedback bias scheme & current neutral comparator addresses CM effects observed when many channels fire

global comparator threshold voltage VCTH generated by 10-bit resistor ladder DAC for linearity & monotonicity

bandgap and VDDA

bandgap has 6 bits tuning register to compensate for process variations

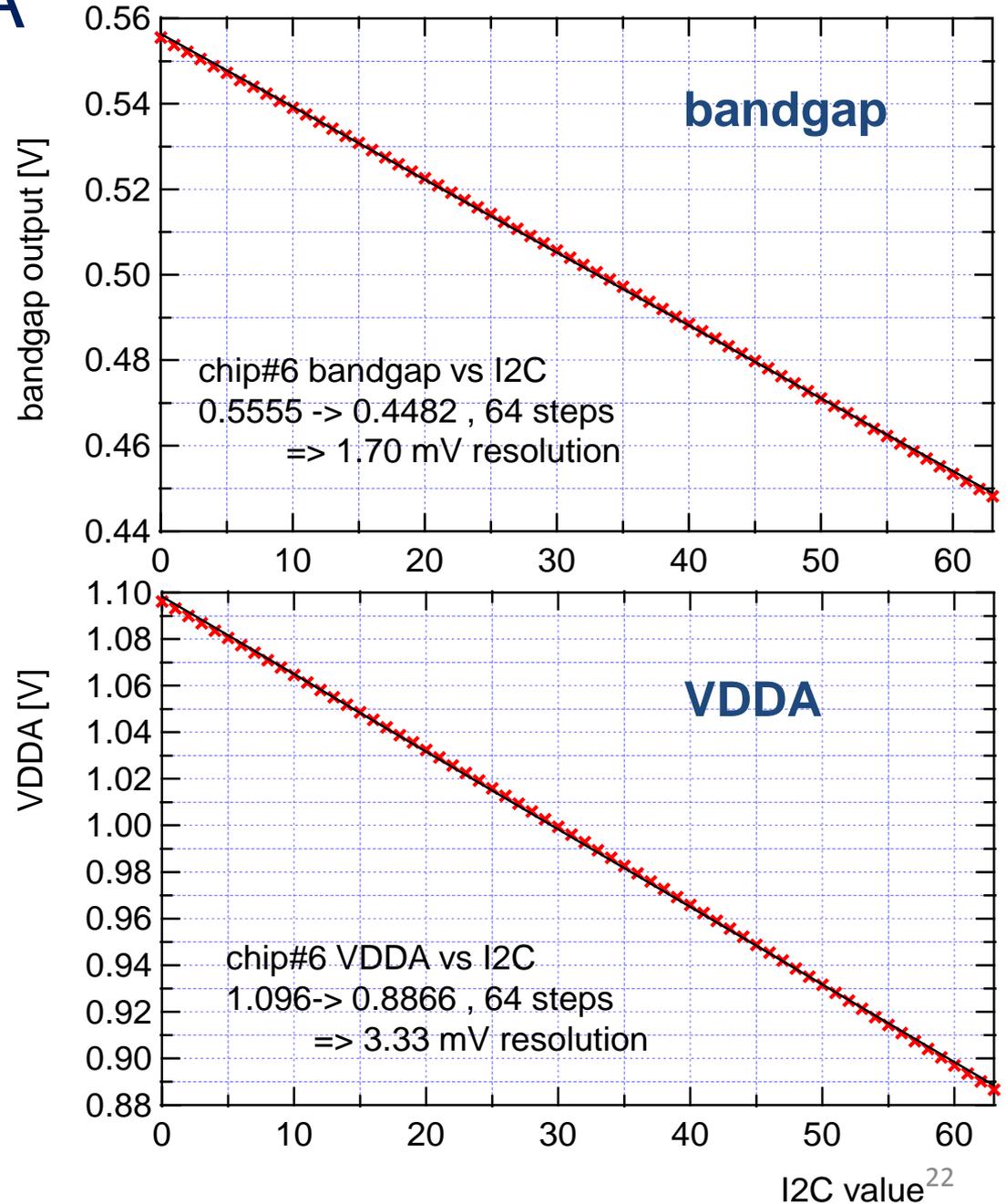
once value is chosen, can blow fuses to store it as default

e-fuse operation not yet looked at

LDO provides VDDA

value = 2x bandgap

LDO clearly working, but no detailed studies yet

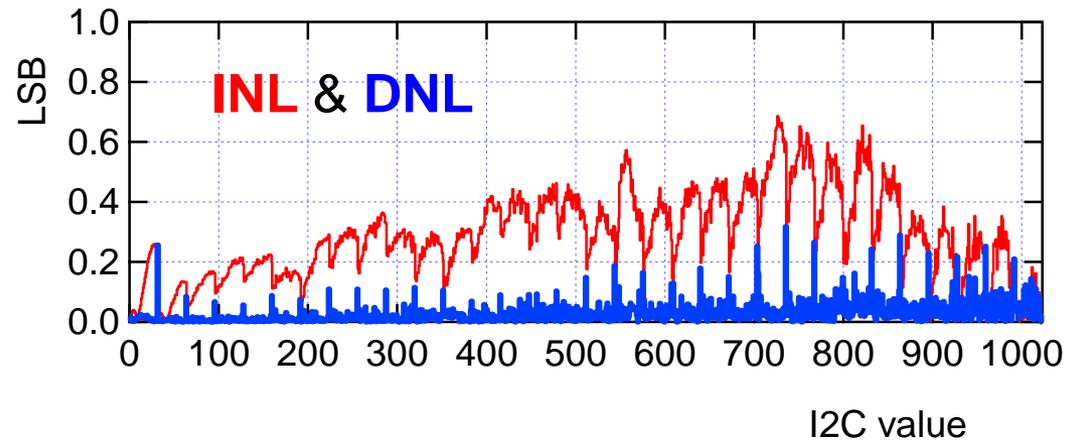
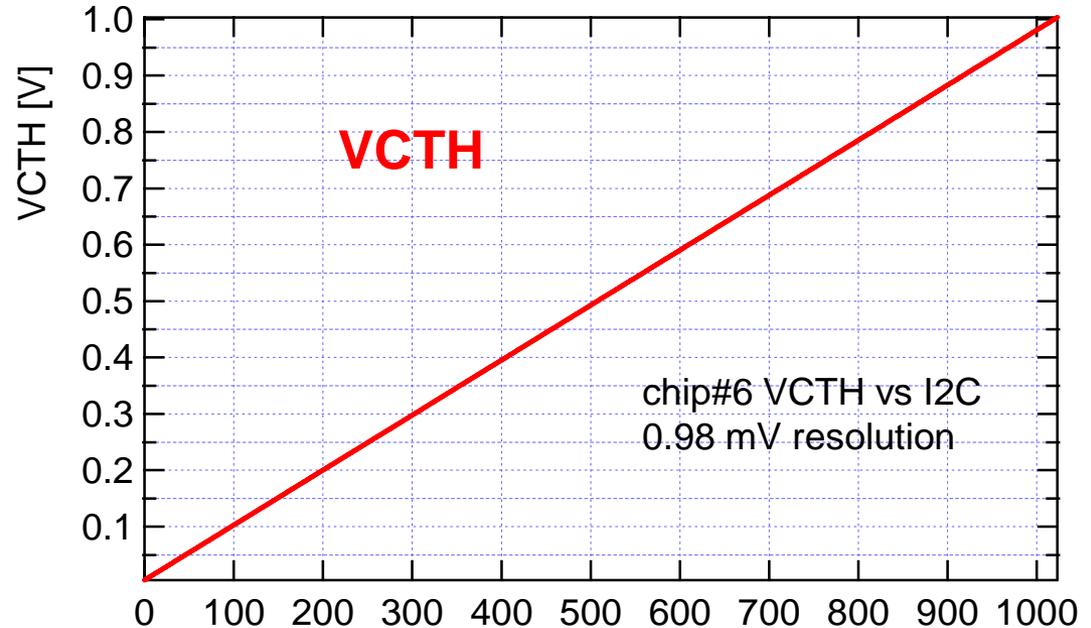


VCTH

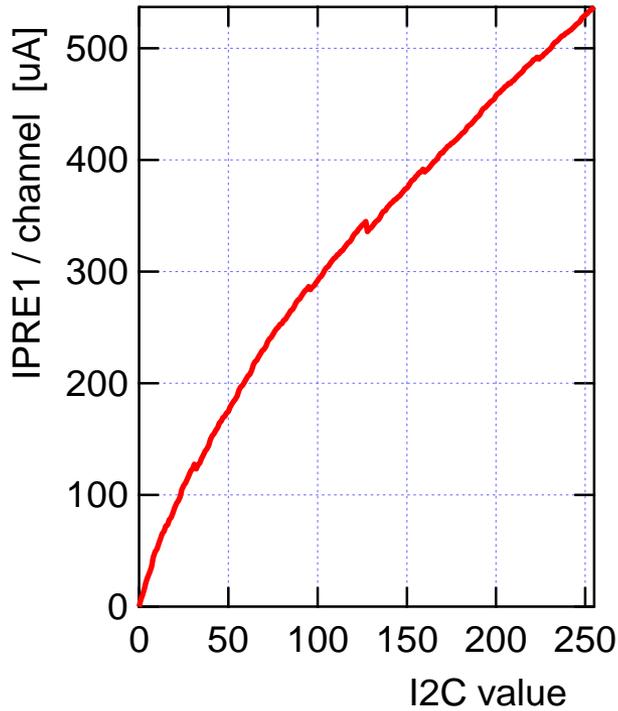
VCTH now generated by 10-bit resistor ladder DAC

~ 1 mV resolution (~ 150 electrons)

$$\text{INL} = \left| \frac{\begin{pmatrix} V_{\text{meas}} - V_{\text{zero}} \\ V_{\text{LSB-IDEAL}} \end{pmatrix} - \text{I2C}_{\text{value}}}{1} \right|$$
$$\text{DNL} = \left| \frac{\begin{pmatrix} V_{m+1} - V_m \\ V_{\text{LSB-IDEAL}} \end{pmatrix} - 1}{1} \right|$$



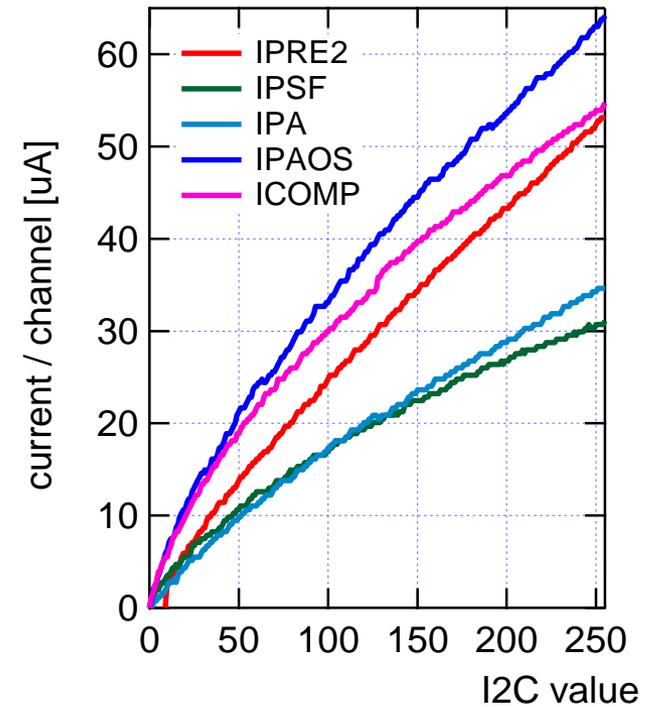
bias currents



IPRE1 (main source of current in input transistor)
now has ~3x fullscale range compared with CBC2

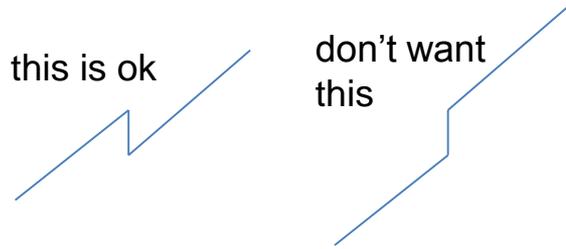
=> can cope with larger sensor capacitance

other current biases
also ok

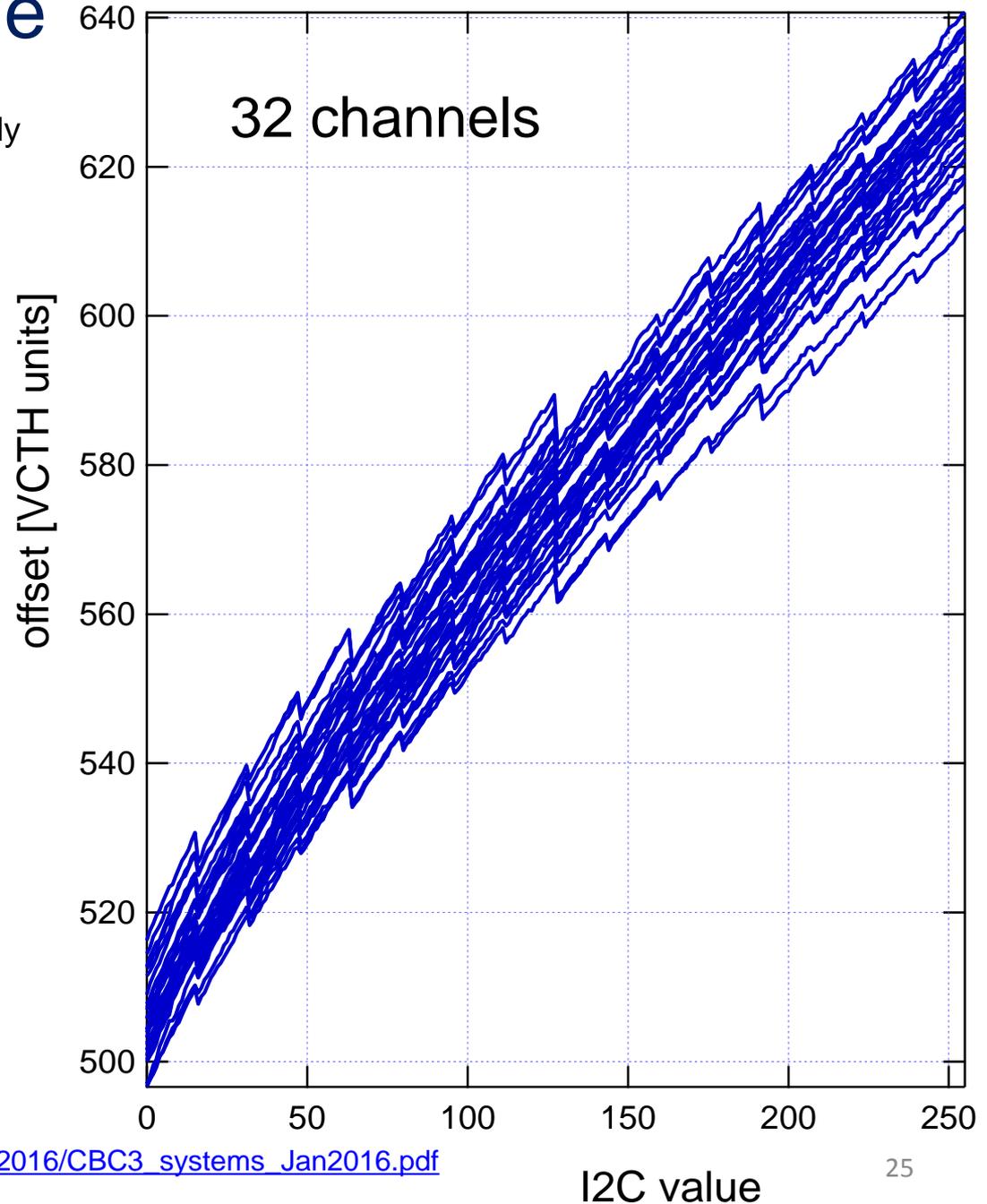


offsets tuning change

CBC2 offsets tuning mechanism deliberately made non-monotonic to avoid gaps where can't set offset accurately

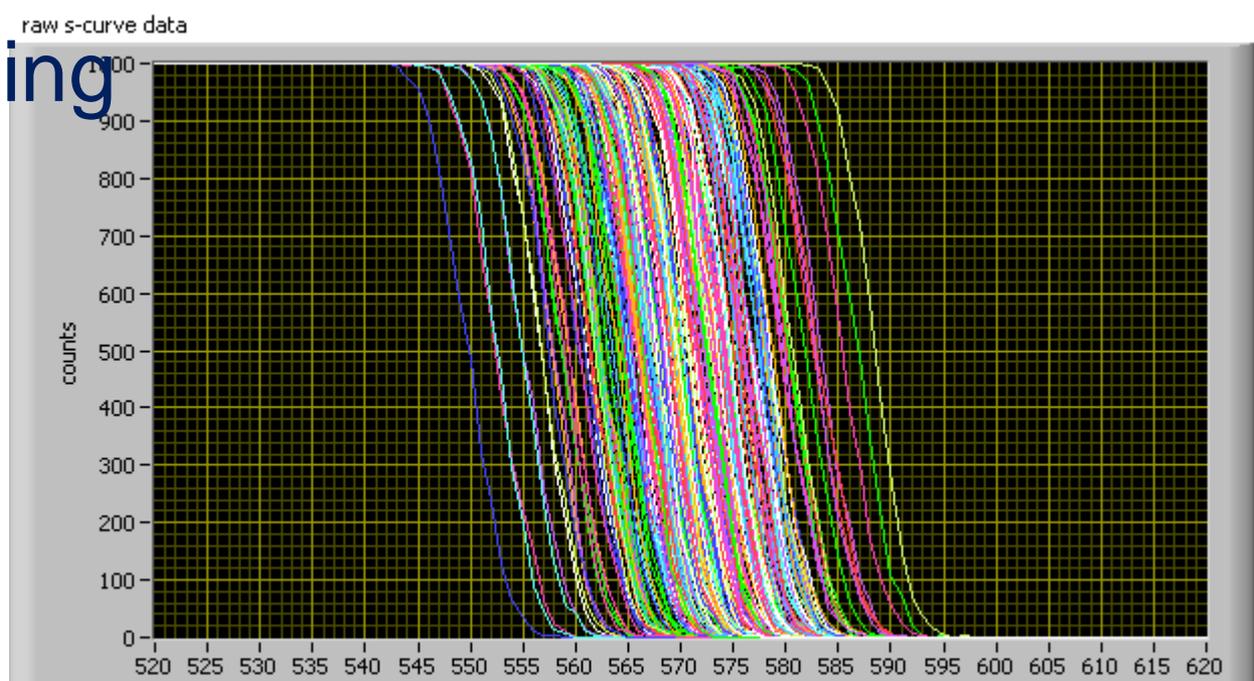


see * for more details

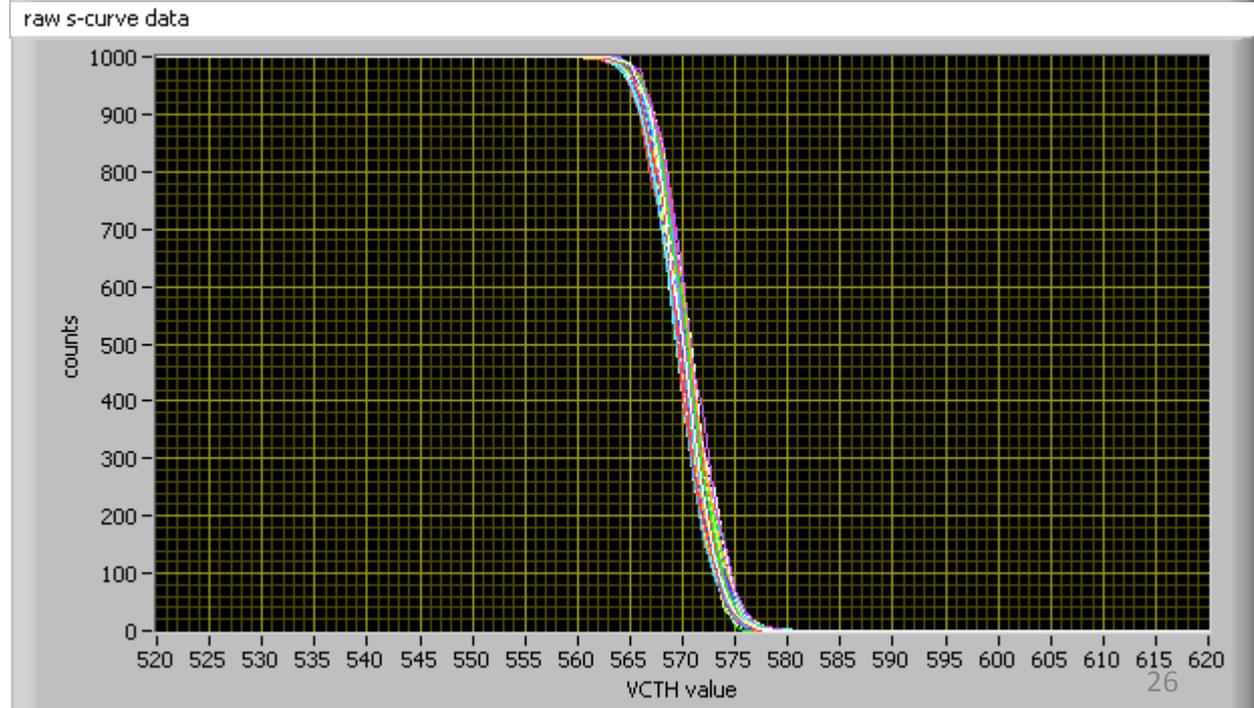


scurves and tuning

all channel offsets set to same value (110 in this case) ➤



after tuning →
32 channels at a time



scurves and tuning

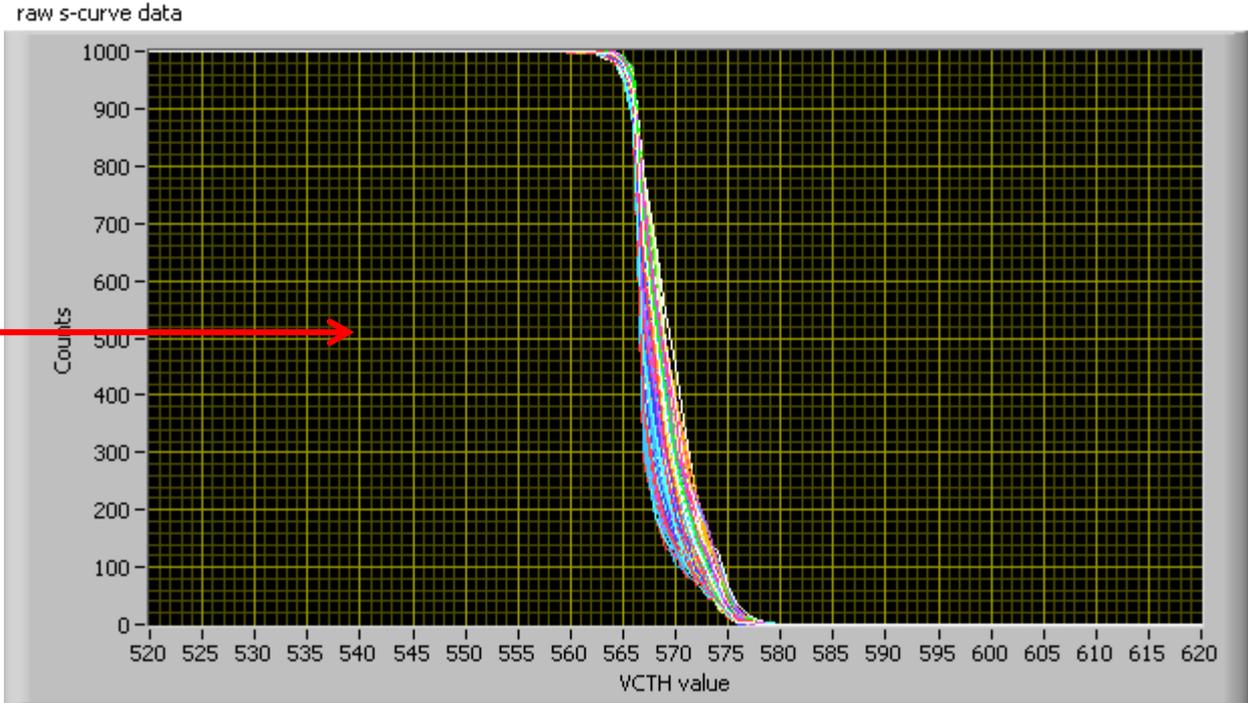
can s-curves be acquired for all channels simultaneously?

not without some distortion

~12 mA increase in VDDD current consumption during period of maximum channels firing activity

but should work better when chip is bump-bonded

=> promising for antenna tests on hybrids



hit detect cct tests

hit detect sensitive to short pulses that only exceed comp. thresh. for short period between clock edged

-> *Fixed Pulse Width*

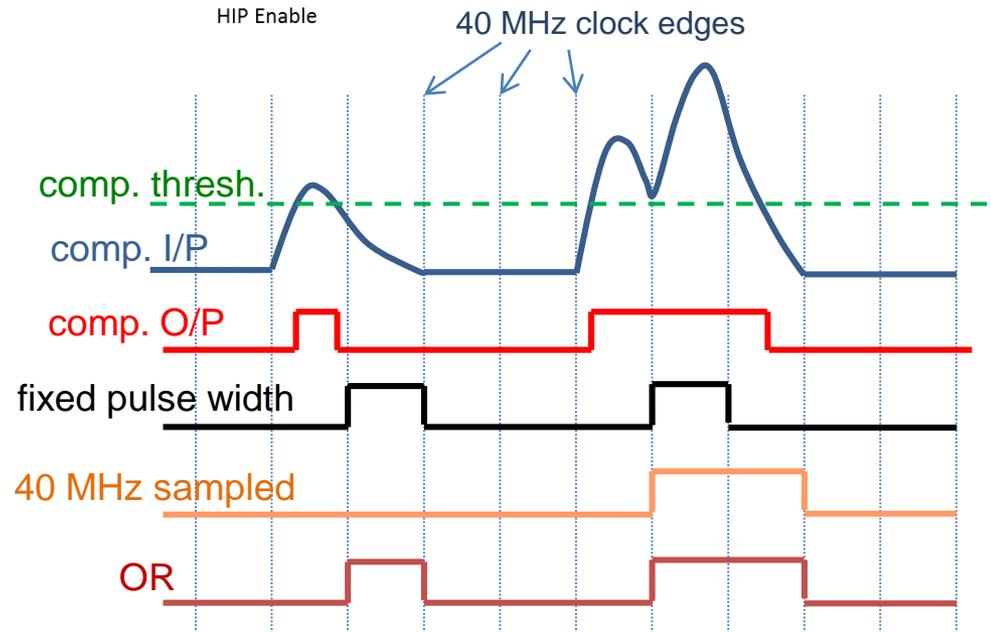
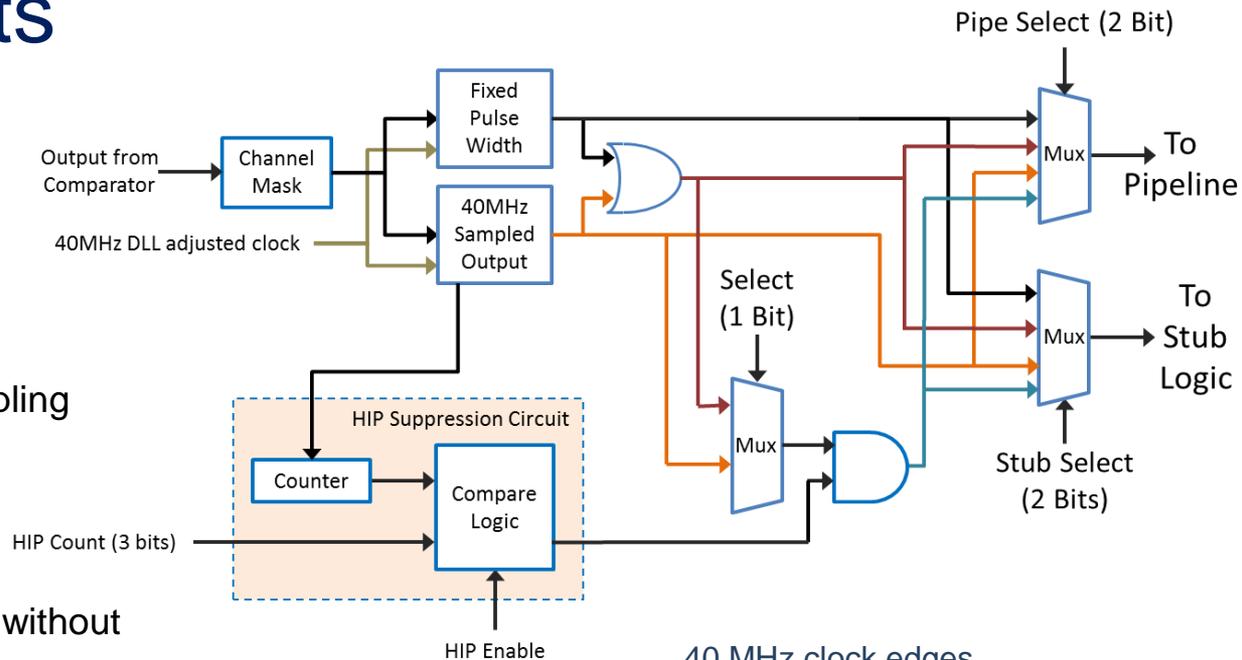
also performs simple 40 MHz sampling

-> *40 MHz Sampled Output*

combining the two by simple OR gives efficiency for piled up pulses without inefficiency for smaller signals

2 separate multiplexers gives flexible choice of which signals can be fed to pipeline and stub logic

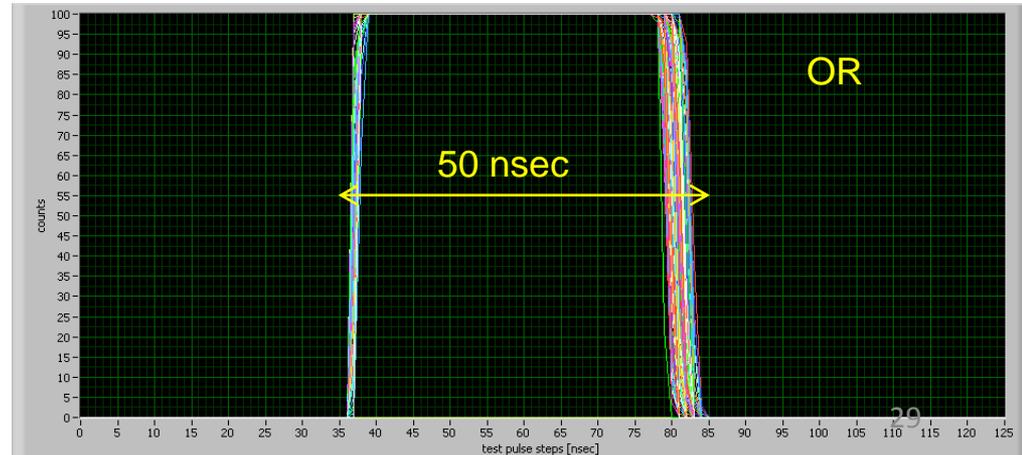
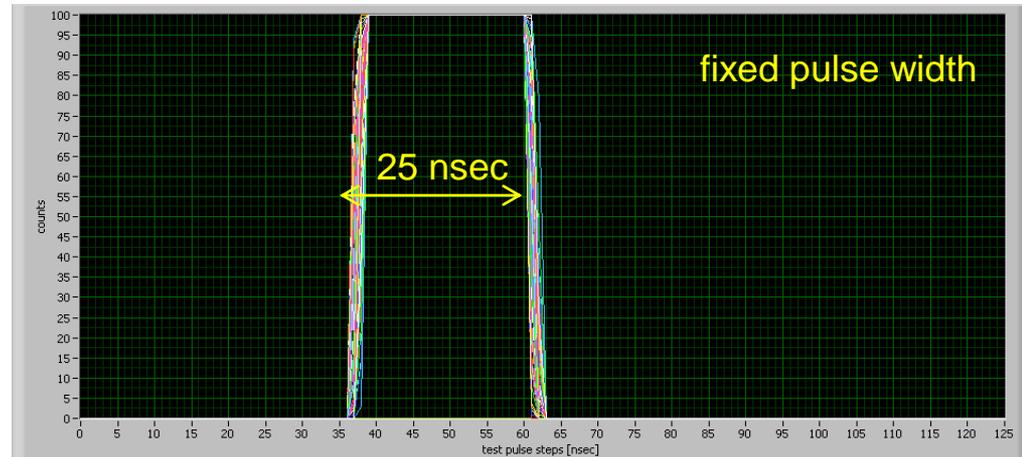
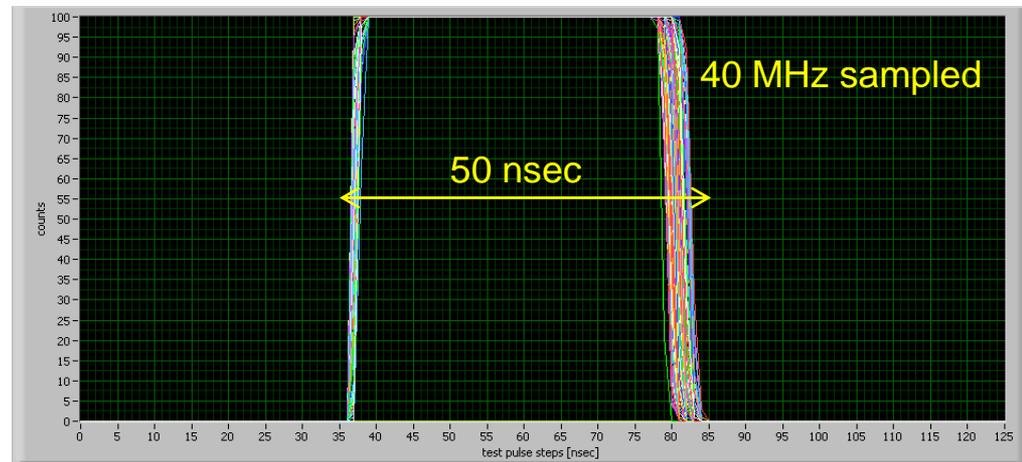
(for normal operation choose OR output to both **and** enable HIP suppression)



hit detect cct tests

verify operation using test pulse, sweeping test pulse trigger in 25 nsec steps, using test pulse DLL to give finer steps of 1 nsec.

pictures here for test pulse amplitude of 60 (decimal), ~ 5 fC



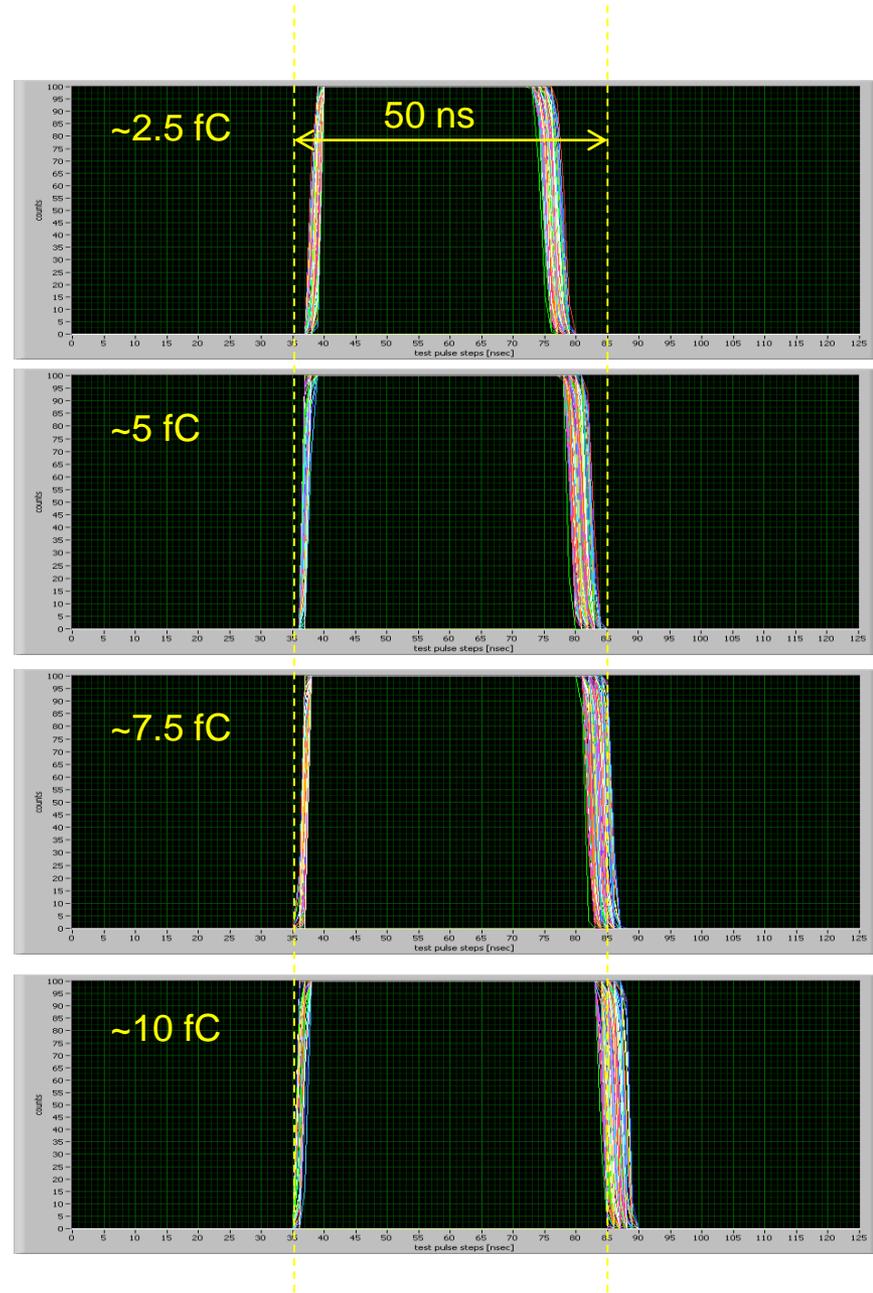
test pulse sweeps

use test pulse to look at signal duration

test pulse amplitudes approximate only

VCTH set to ~ 1.25 fC

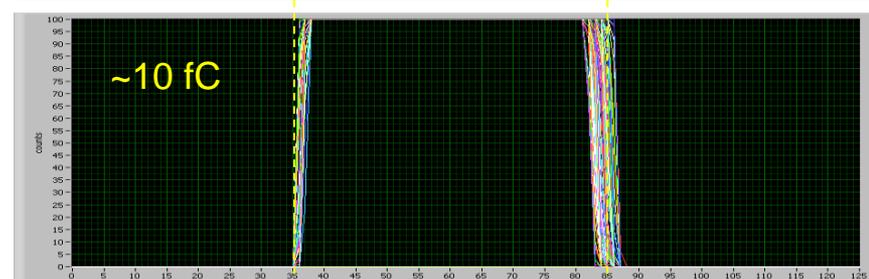
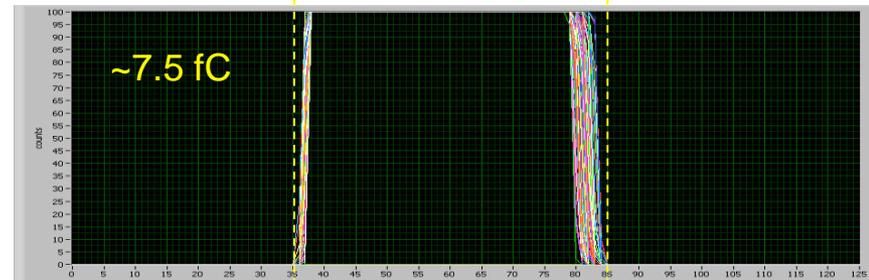
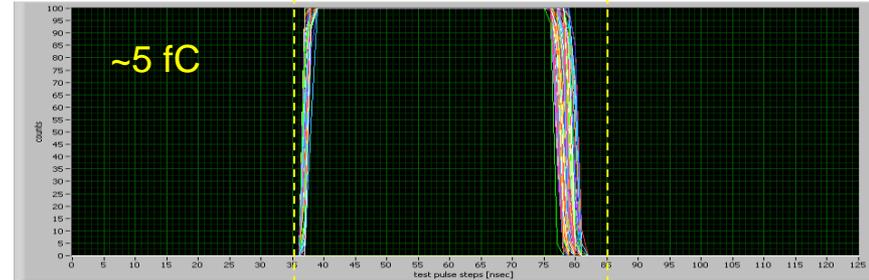
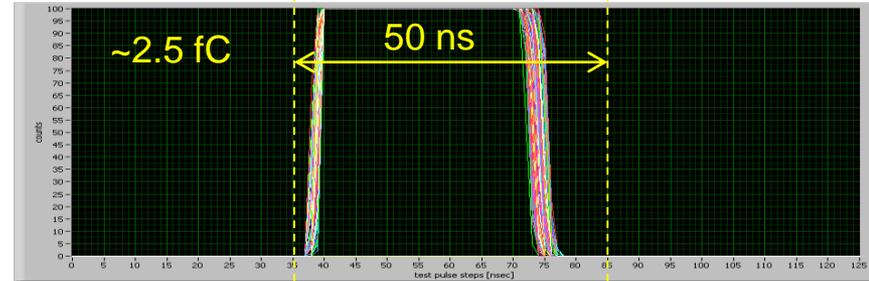
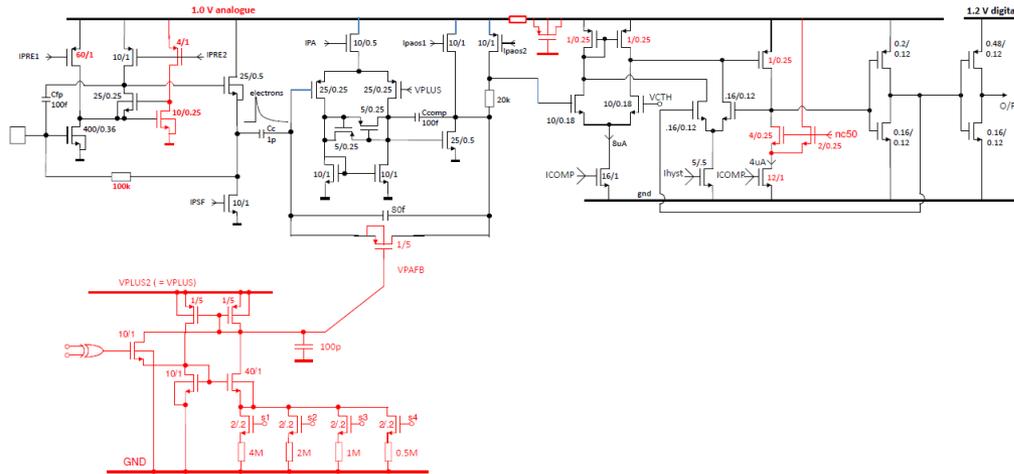
pulse width \sim ok for nominal postamp feedback settings



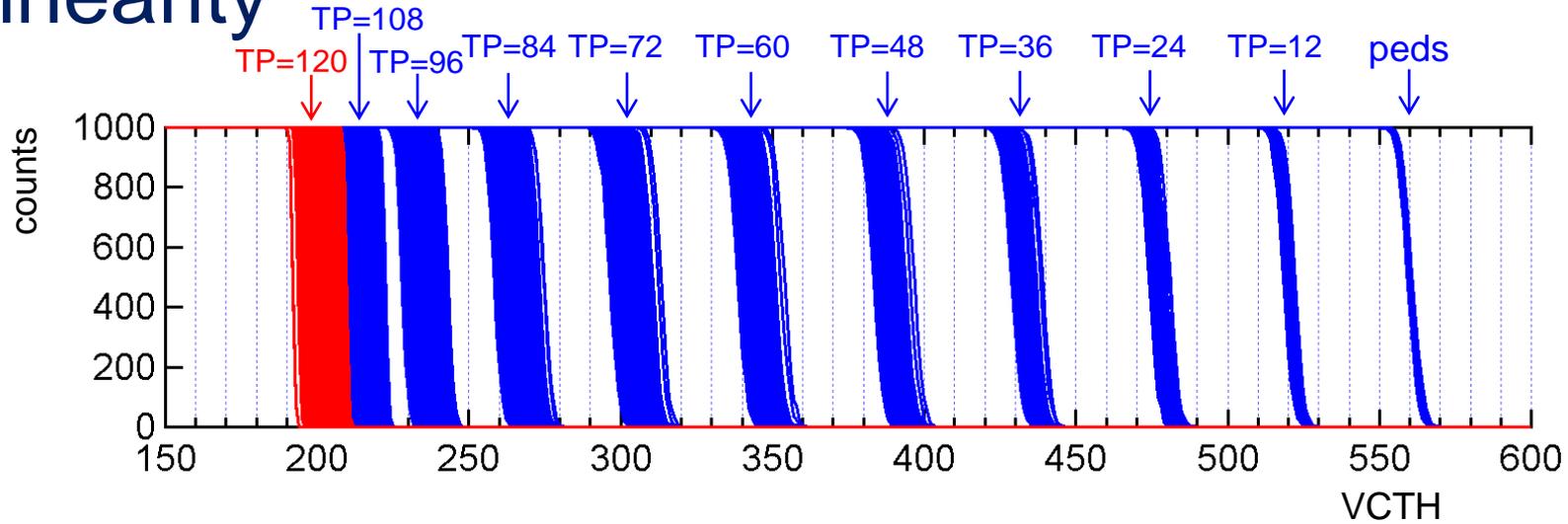
test pulse sweeps

adjustment of pulse width possible using post-amplifier feedback value VPAFB

result for minimum resistance →



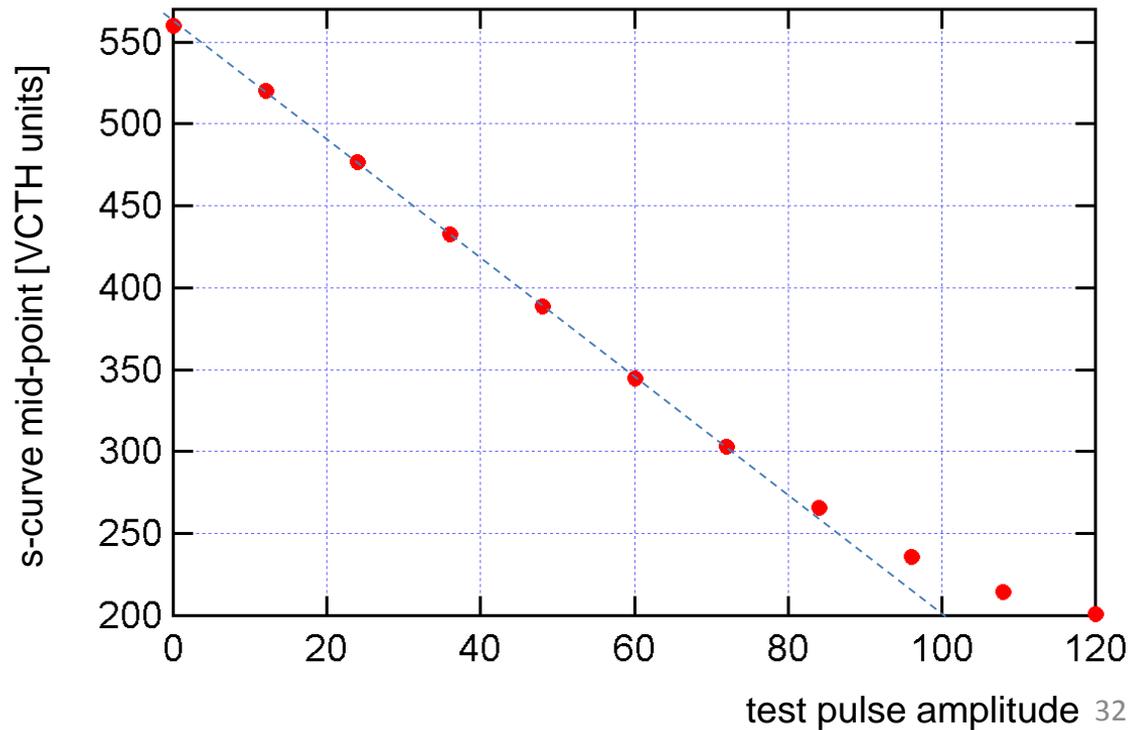
gain & linearity



using approximate calibration

(TP value of 12 = 1 fC)

get ~ 40 mV / fC



power

digital power higher than hoped

for VDDD = 1.2V measure 33.6 mA, equivalent to 160 uW / channel

(if switch SLVS drivers off get 20.7 mA)

=> overall chip power goes to ~ 510 uW/channel, unless sacrifice some analogue power

note: analogue power calculations based on 1.2V (not 1.25)

CBC3 spec. "The target power consumption for 5cm strips (~8pF) is 450 μ W/Channel, assuming 350 μ W/Channel analogue and 100 μ W/Channel digital power consumption."

yield

1st batch of 9 chips bonded

5 ok, 4 had problems

3 drew no power, showed no activity

1 drew high current

2nd batch of 9 chips

all ok (power, I2C ok, produce data)

summary

still early days, but CBC3 is working

some digital issues to work around, but nothing to stop progress

analogue front end appears ok

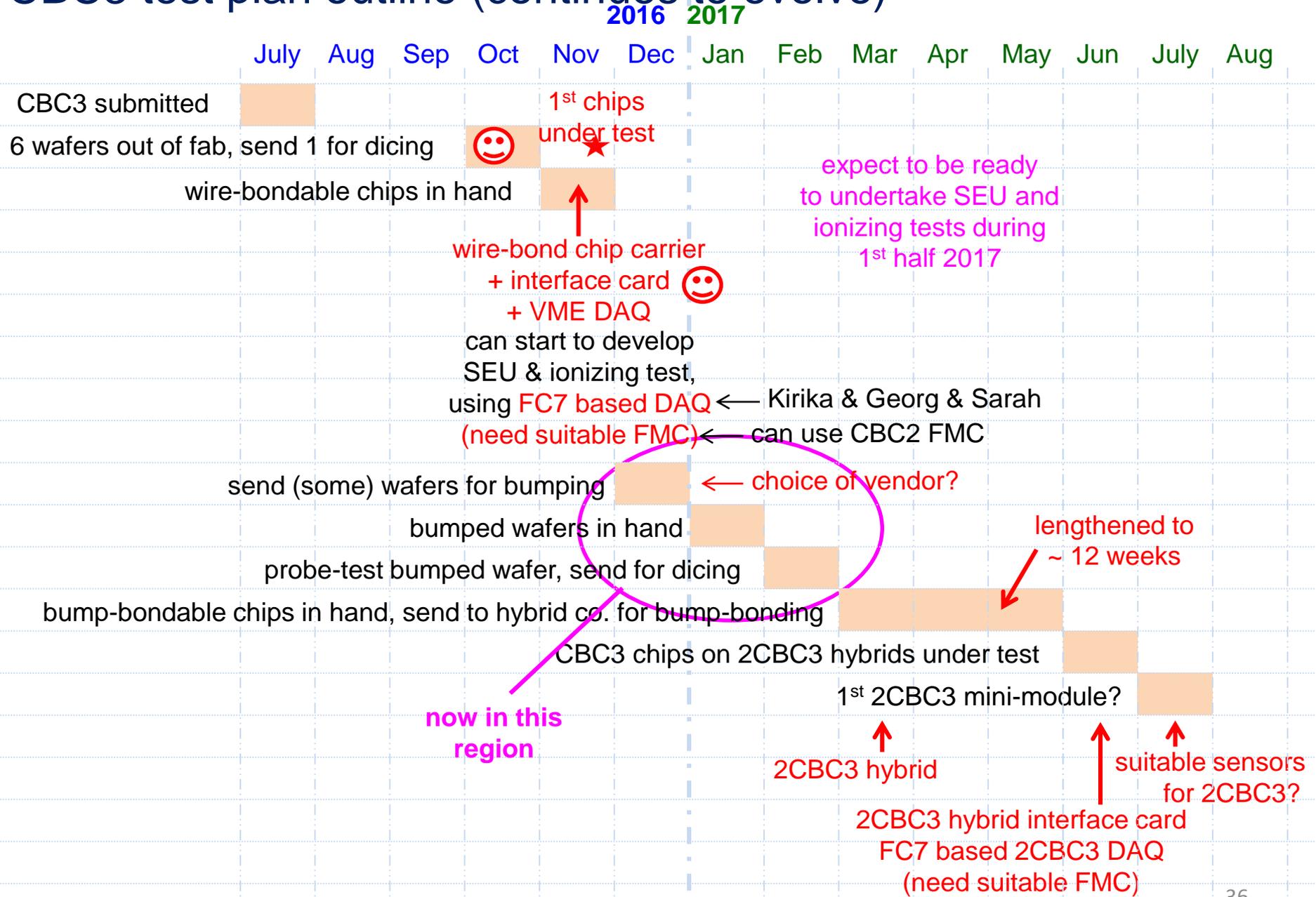
more to investigate, but need to bump-bond and connect to sensors to get true performance

SEU & ionizing irradiation test procedures can now be developed based on wirebonded single chip setup

next priority to develop wafer probe test

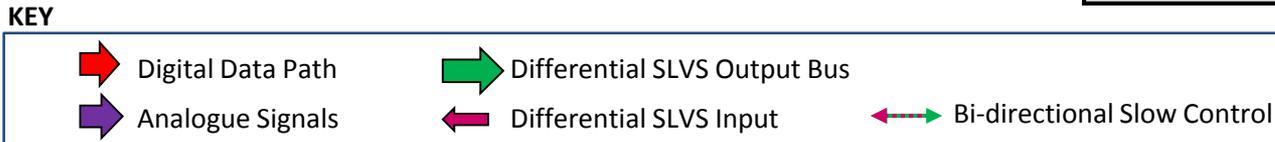
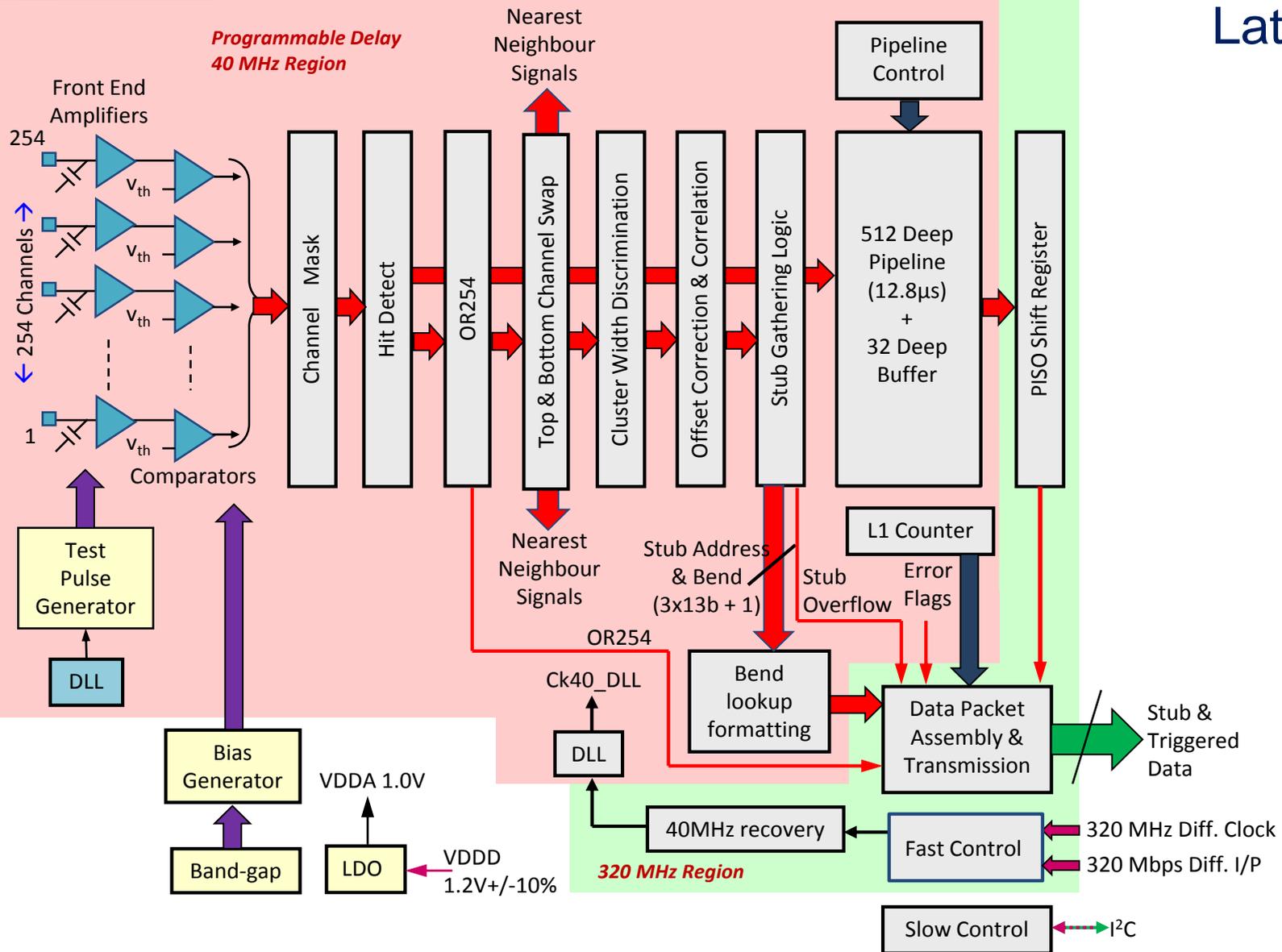
short term schedule on next page

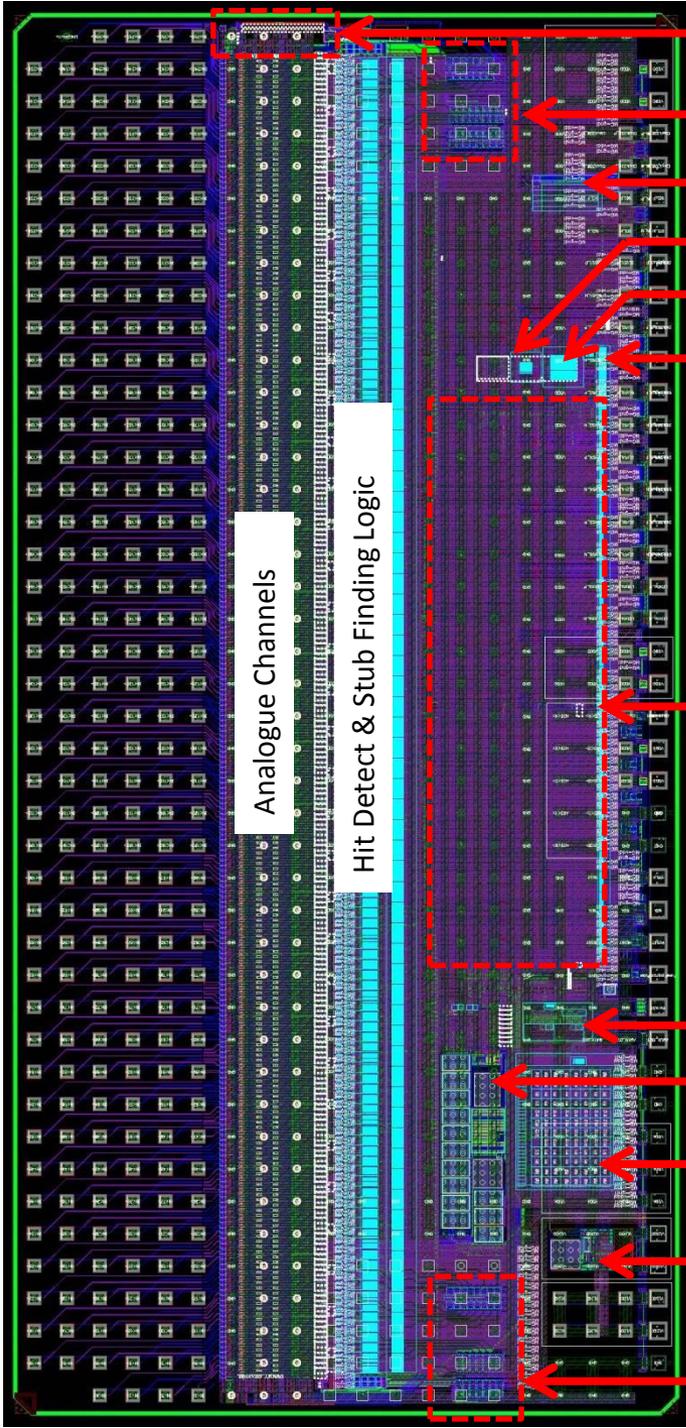
CBC3 test plan outline (continues to evolve)



extra

Latest Block Diagram





test pulse circuit

I/O to neighbour

DLL

bend LUT

data assembly

L1 counter & FIFO

Analogue Channels

Hit Detect & Stub Finding Logic

512 deep pipeline & O/P buffer

bandgap

I2C & biases

10b DAC for VCTH

LDO

I/O to neighbour

final layout picture for reference

20 columns, 43 rows
(1 more column than CBC2)

5.25 mm x 11 mm

pad allocations

pads as viewed on hybrid surface
(as if looking through chip)

right-most column for wire-bond / wafer probe

like CBC2 gives access to internal
bias currents and voltages

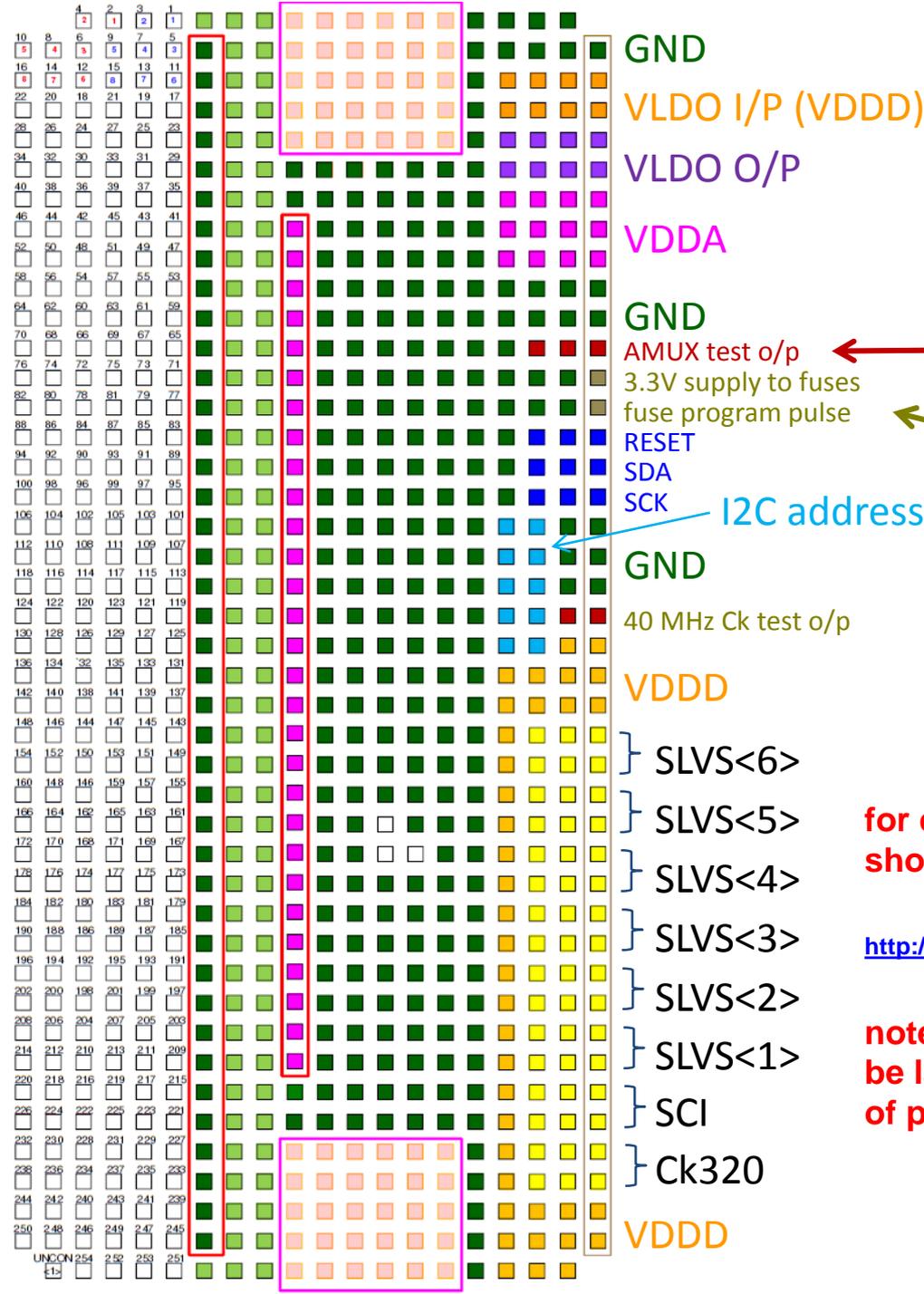
chip ID can be set by e-fuses (19 bits)
will be programmed at wafer probe time
every chip will have unique ID

CERN PMOS bandgap reference
also trimmed by e-fuses (6 bits)

for detailed picture, prepared by Lawrence Jones,
showing all pads labelled, download:

http://www.hep.ph.ic.ac.uk/~dmray/pictures/CBC3_PADS_Footprint1.png

note: downloadable picture shows pads as should
be laid out on hybrid surface (flipped version
of pads on chip)



CBC3 digital interfaces

output data: up to 3 stubs data transmitted to CIC/BX
6 SLVS diff pairs @ 320 Mbps

→ 25 ns

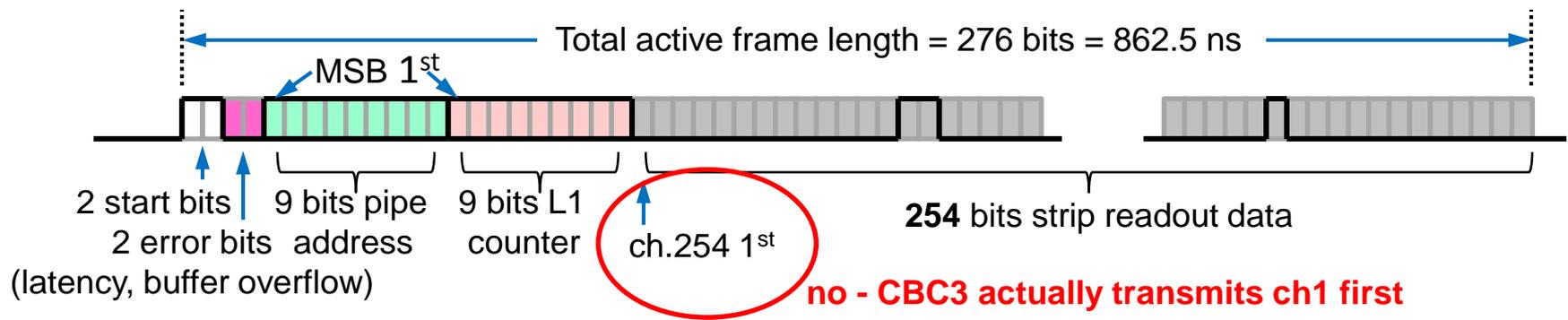
S1<7>	S2<7>	S3<7>	B2<3>	Sync	R
S1<6>	S2<6>	S3<6>	B2<2>	Error	R
S1<5>	S2<5>	S3<5>	B2<1>	OR254	R
S1<4>	S2<4>	S3<4>	B2<0>	SoF	R
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	R
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	R
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	R
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	R

R = L1 triggered readout data

time flow **top** to **bottom** (e.g. S1<7> output first)

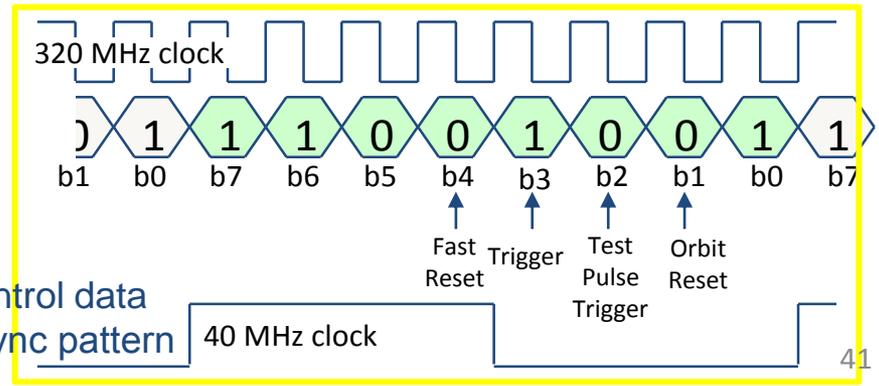
readout data

readout data frame length 950 nsec
=> up to 1 MHz L1 triggering capability



fast control

320 MHz clock
320 Mbps fast control line



40 MHz generated from fixed sync pattern in fast control data
normal command structure can't be confused with sync pattern