CBC3 progress

matters arising from last time
- I2C spec
- 40 MHz clock source

design progress

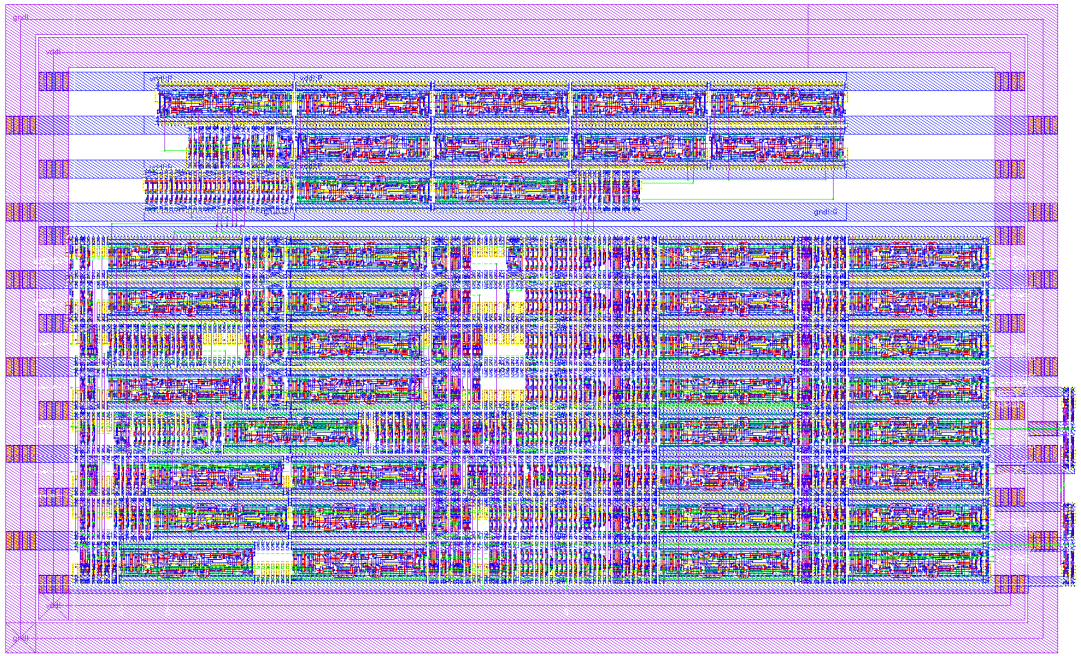
systems meeting, 26th April, 2016.

I2C modifications

CBC3 I2C complete, including

reset on start or repeated start conditions

reset if SDA stuck low for 9 clock cycles



CBC3 digital interfaces

output data: up to 3 stubs data transmitted to CIC/BX
- 5 diff pairs @ 320 Mbps
- 8 bit stub seed address (1/2 strip resolution)
- 4 bit bend info (location of cluster in window layer)

up to 1 MHz L1 triggering capability
- 1 diff pair @ 320 Mbps
- readout data frame < 1 usec

single 320 Mbps fast control line

NEW
- 40 MHz clock generated from fixed pattern in fast control data
- normal command structure can not be confused with sync pattern

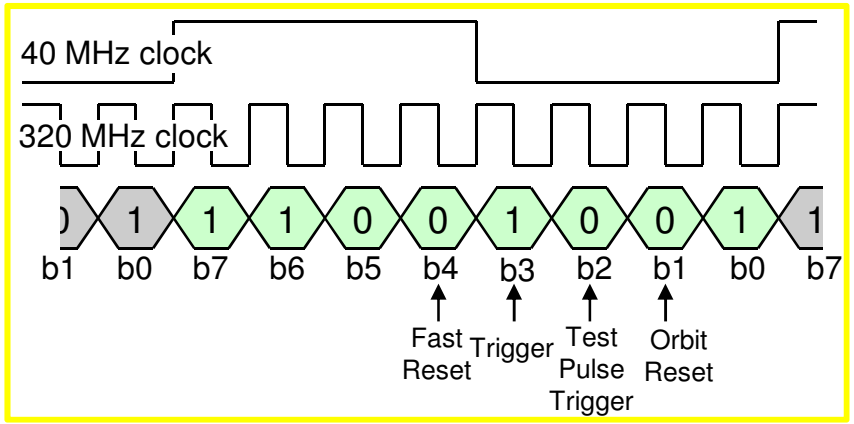
output data

25 ns

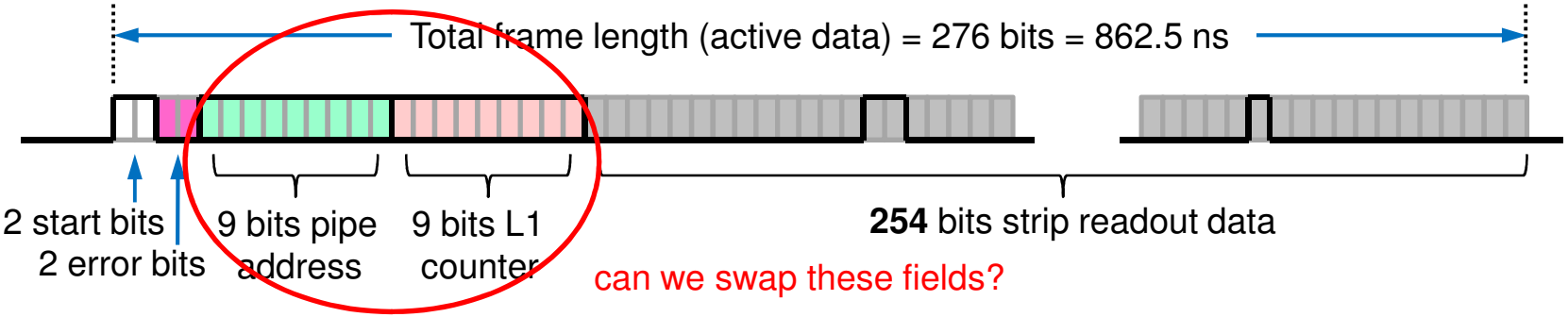
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	R
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	R
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	R
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	R
S1<4>	S2<4>	S3<4>	B2<0>	SoF	R
S1<5>	S2<5>	S3<5>	B2<1>	OR254	R
S1<6>	S2<6>	S3<6>	B2<2>	Error	R
S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	R

R = L1 triggered readout data
time flow top to bottom (e.g. S1<0> output first)

fast control

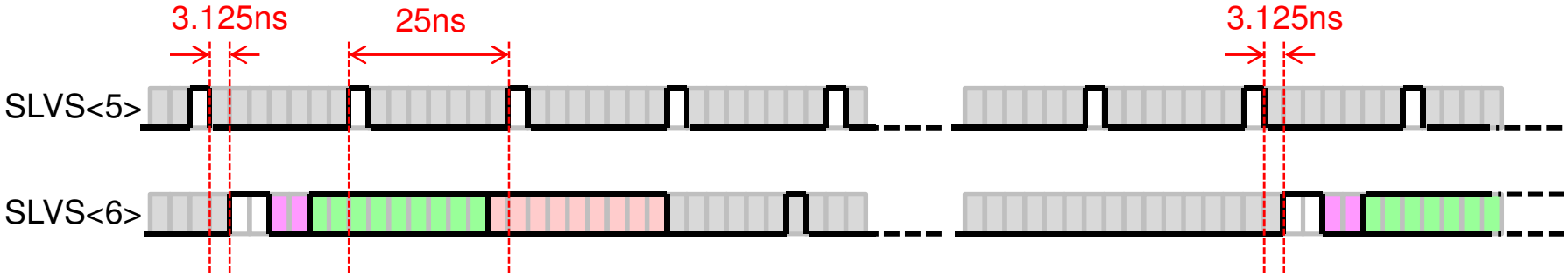


readout data frame



can we swap these fields?

output data frame timing



SLVS<5> contains sync pulse
SLVS<6> is triggered readout data

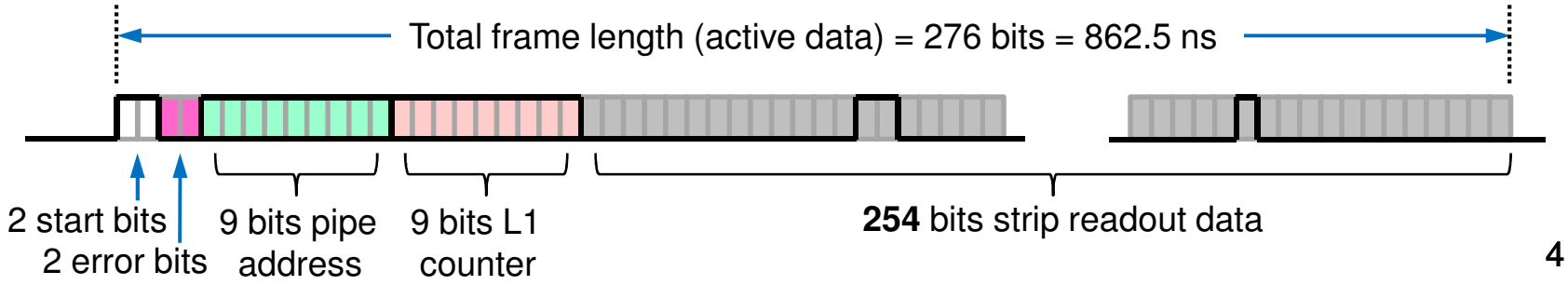
in current design output data frame header starts in 2nd bit of 25 nsec block
i.e. 3.125 nsec gap between sync pulse and 1st bit of header

overall output data frame length padded to exact multiple of 25 nsec

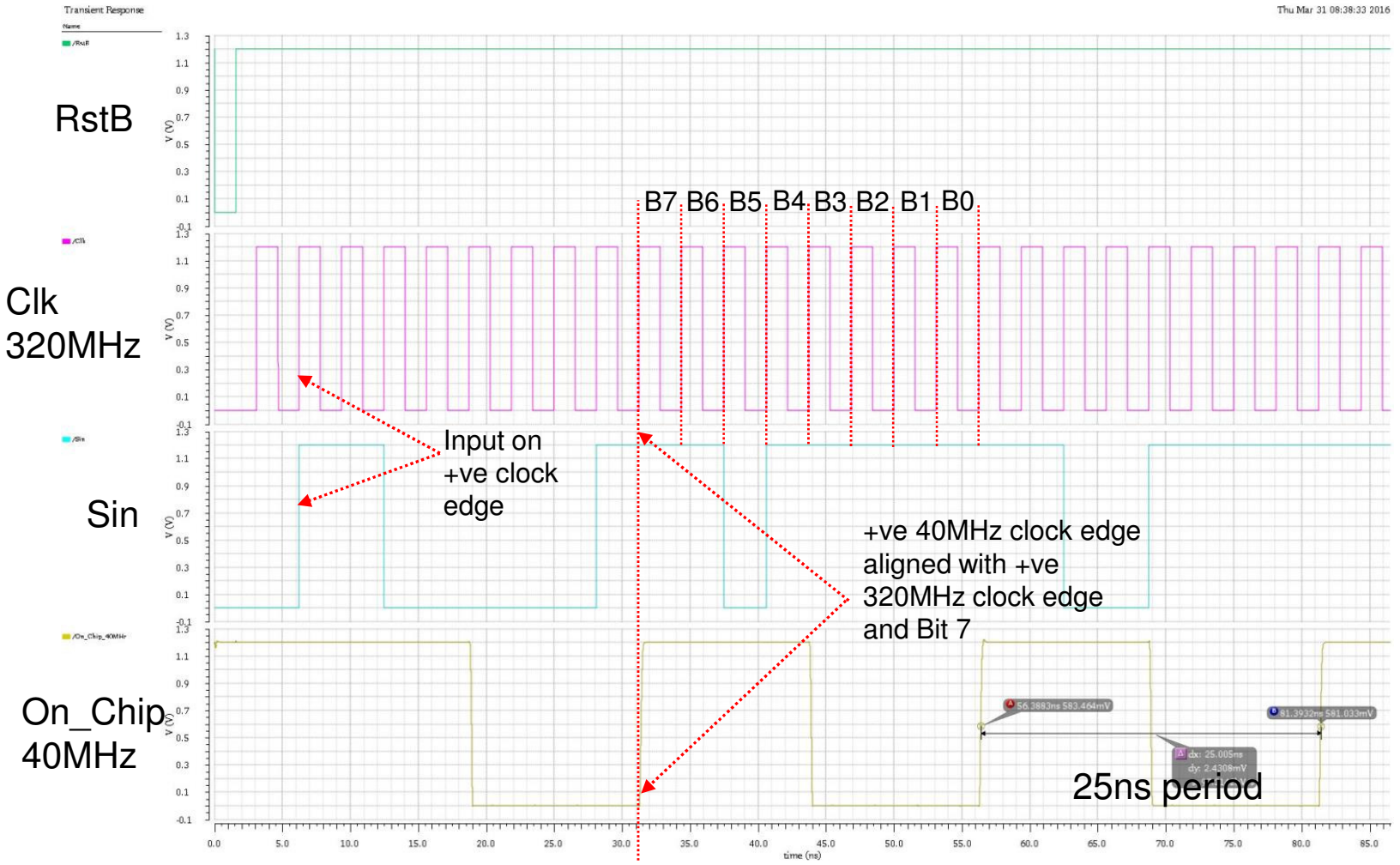
SLVS<1>	SLVS<2>	SLVS<3>	SLVS<4>	SLVS<5>	SLVS<6>
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	**R**
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	**R**
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	**R**
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	**R**
S1<4>	S2<4>	S3<4>	B2<0>	SoF	**R**
S1<5>	S2<5>	S3<5>	B2<1>	OR254	**R**
S1<6>	S2<6>	S3<6>	B2<2>	Error	**R**
S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	**R**

25 ns

readout data frame



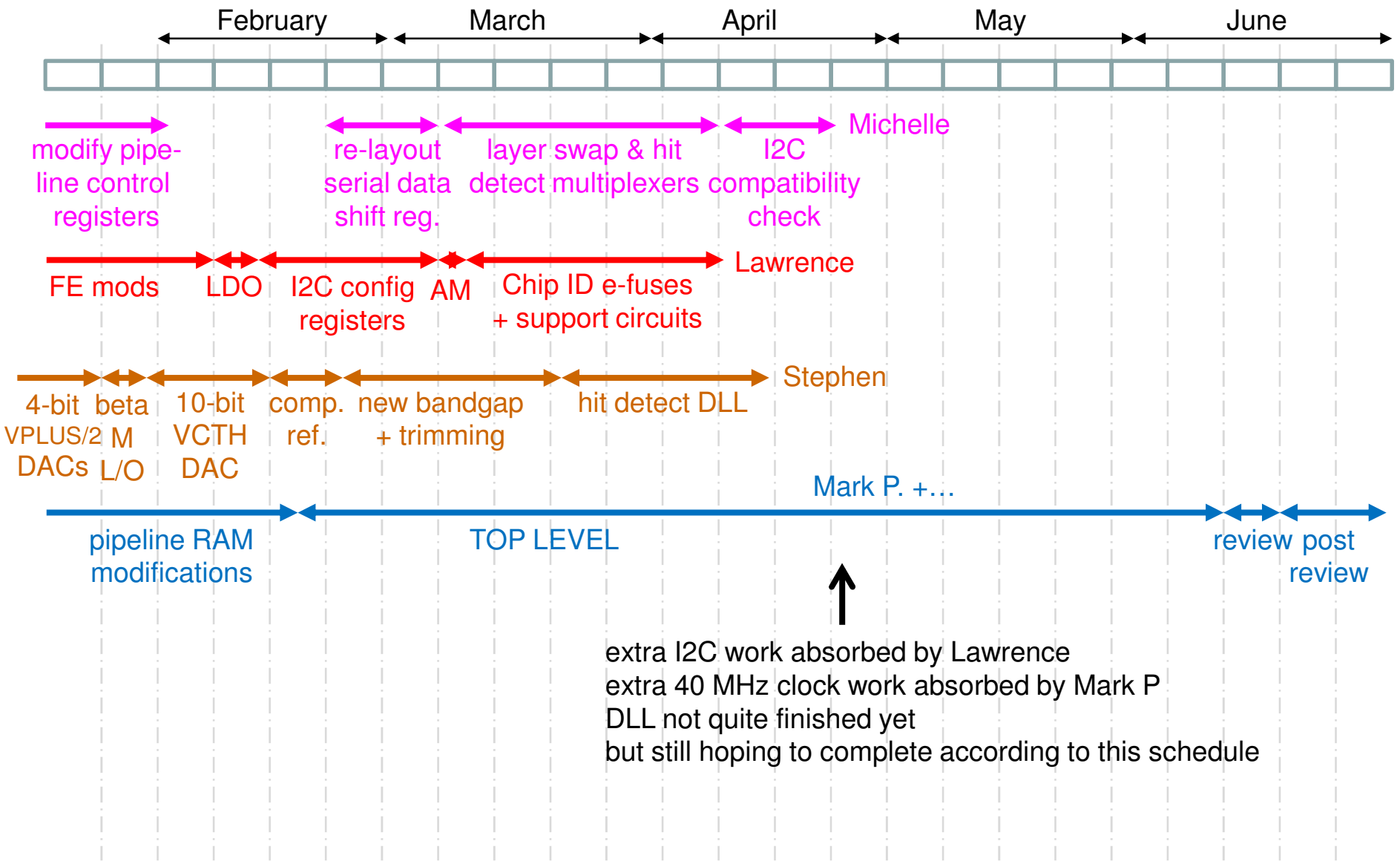
SCI timing detail



status: schematic only - layout to be done

plan to triplicate block, with majority vote on output

schedule


February
March
April
May
June
modify pipe-line control registers
re-layout serial data shift reg.
layer swap & hit detect multiplexers
I2C compatibility check
Michelle
FE mods
LDO
I2C config registers
AM
Chip ID e-fuses + support circuits
Lawrence
4-bit VPLUS/2 DACs
beta M L/O
10-bit VCTH DAC
comp. ref.
new bandgap + trimming
hit detect DLL
Stephen
Mark P. +…
pipeline RAM modifications
TOP LEVEL
review post review
extra I2C work absorbed by Lawrence
extra 40 MHz clock work absorbed by Mark P
DLL not quite finished yet
but still hoping to complete according to this schedule

I2C registers for fuses

Two types:

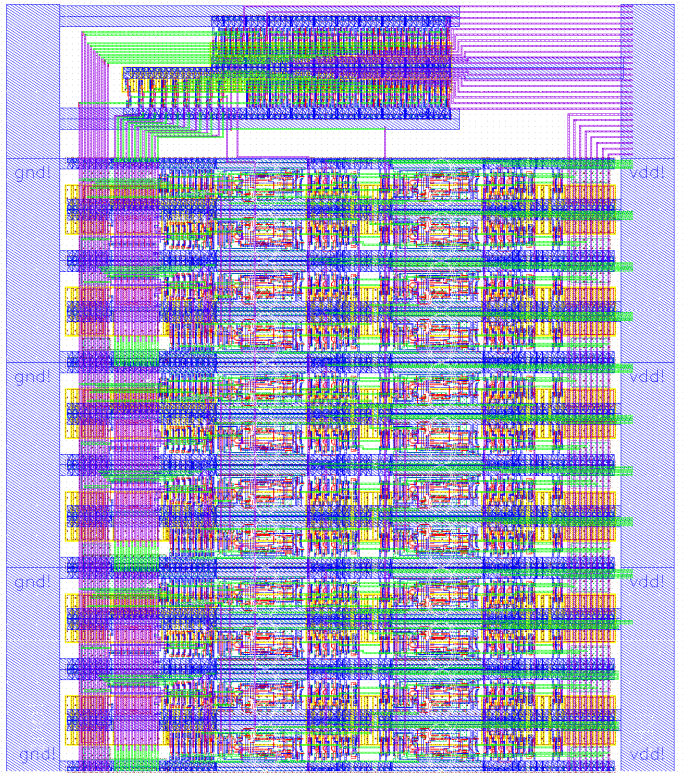
1) 19 bits version for chip ID
   - -Write fuse values to register
   - -Read fuse register back
   - -Blow fuses
   - -Read fuse settings back

   One control bit needed to set whether reading from register or fuses.

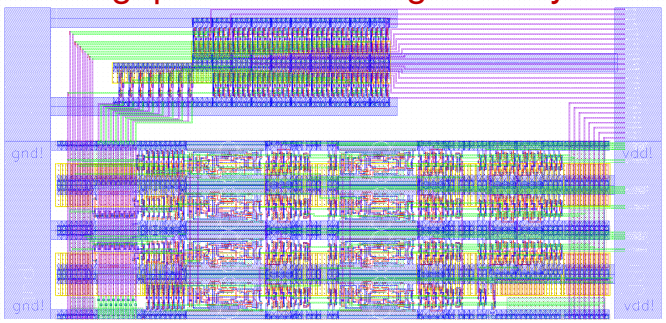
2) 6 bits version for Bandgap Trim
   - -Write fuse values to register
   - -Read fuse register back
   - -Blow fuses
   - -Read fuse settings back
   - -Override fuses

   Two control bits needed to select readback and to overide.

Chip ID Fuse Register Layout



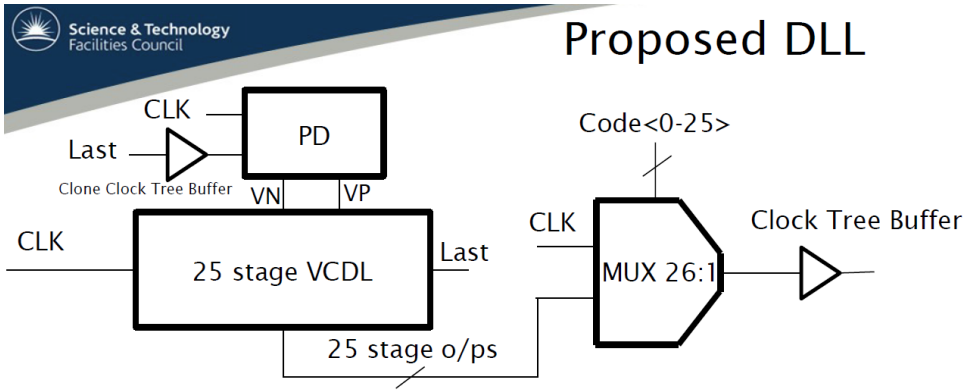
Bandgap Trim Fuse Register Layout



DLL for front end sampling

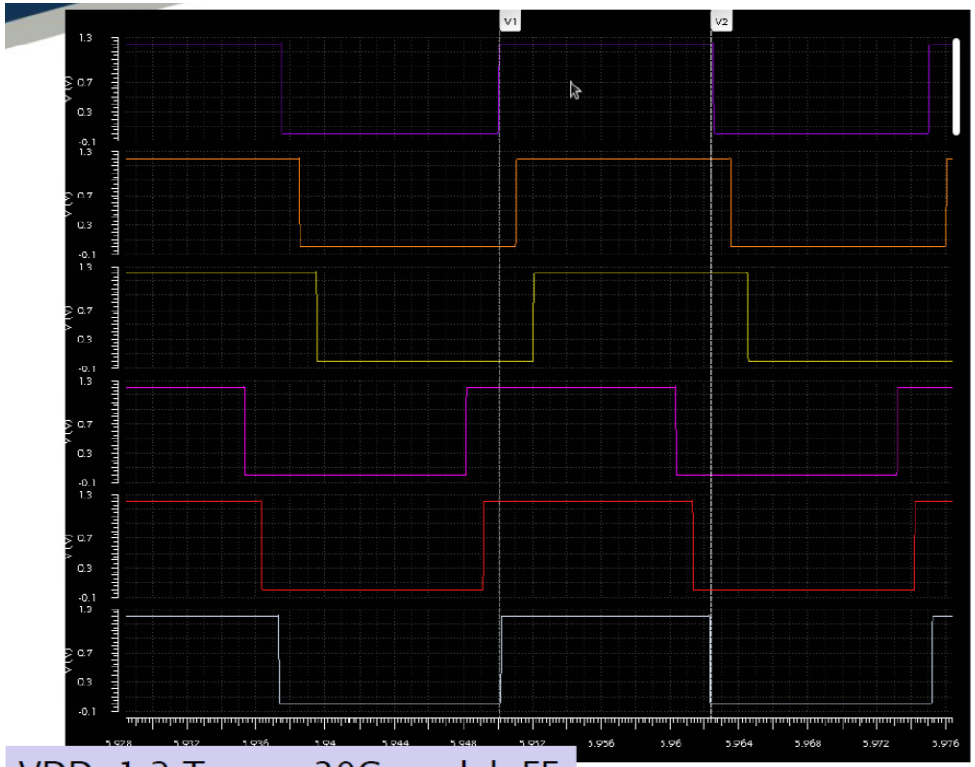
CBC2 DLL deviates slightly from 50:50 mark: space ratio (not an issue for test pulse)

will use improved version for CBC3



- Existing delay stages from CBC2
- Uses a new phase detection circuit
  - Two charge pumps
  - Muller C gate

- Fixed width delay pulses
- Synced to both edges of the clock
- Delay in steps of 1ns
- 25 step control with bypass option
- Code<0> = bypass
- Code<1-25> = <1-25>*1ns increments



VDD=1.2 Temp=-30C model=FF

i/p 40MHz

Code <1>
1ns delay

Code <2>
2ns delay

Code <23>
23ns delay

Code <24>
24ns delay

Code <25>
25ns delay

pre-layout simulation

pulse width 12.5 nsec +/- 150 psec
(all corners, -20, +30)

max period jitter (code <25>)
+/- 180 psec

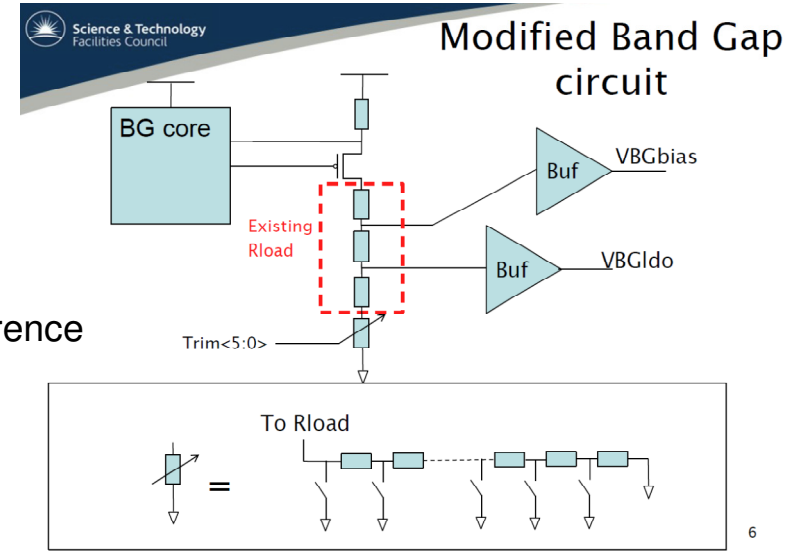
bandgap and trimming

using CERN PMOS based bandgap for radiation stability

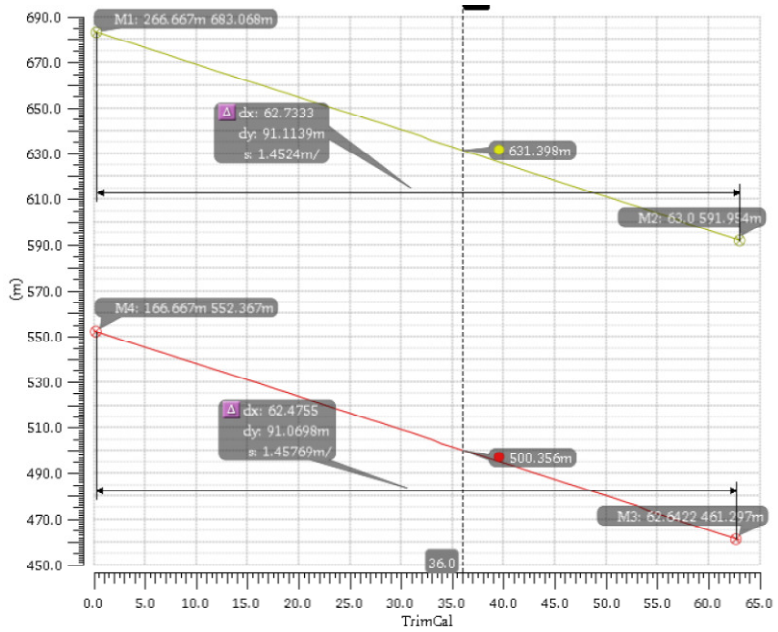
requires trimming for process variations

need 2 voltages, one for LDO and one for master current reference

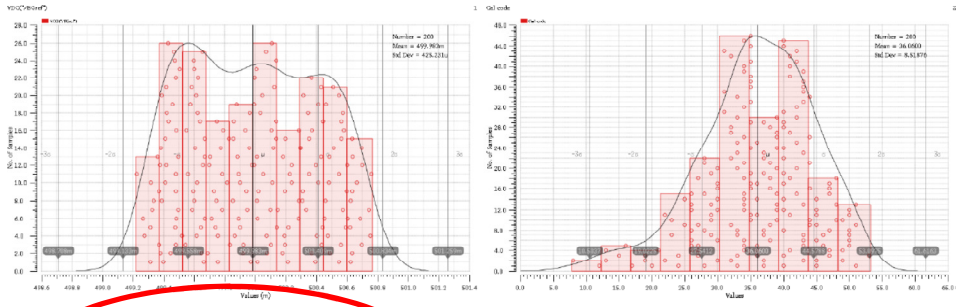
6-bit trim enough to cope with process with good accuracy



6bit trim range



Trimming of MC process variation

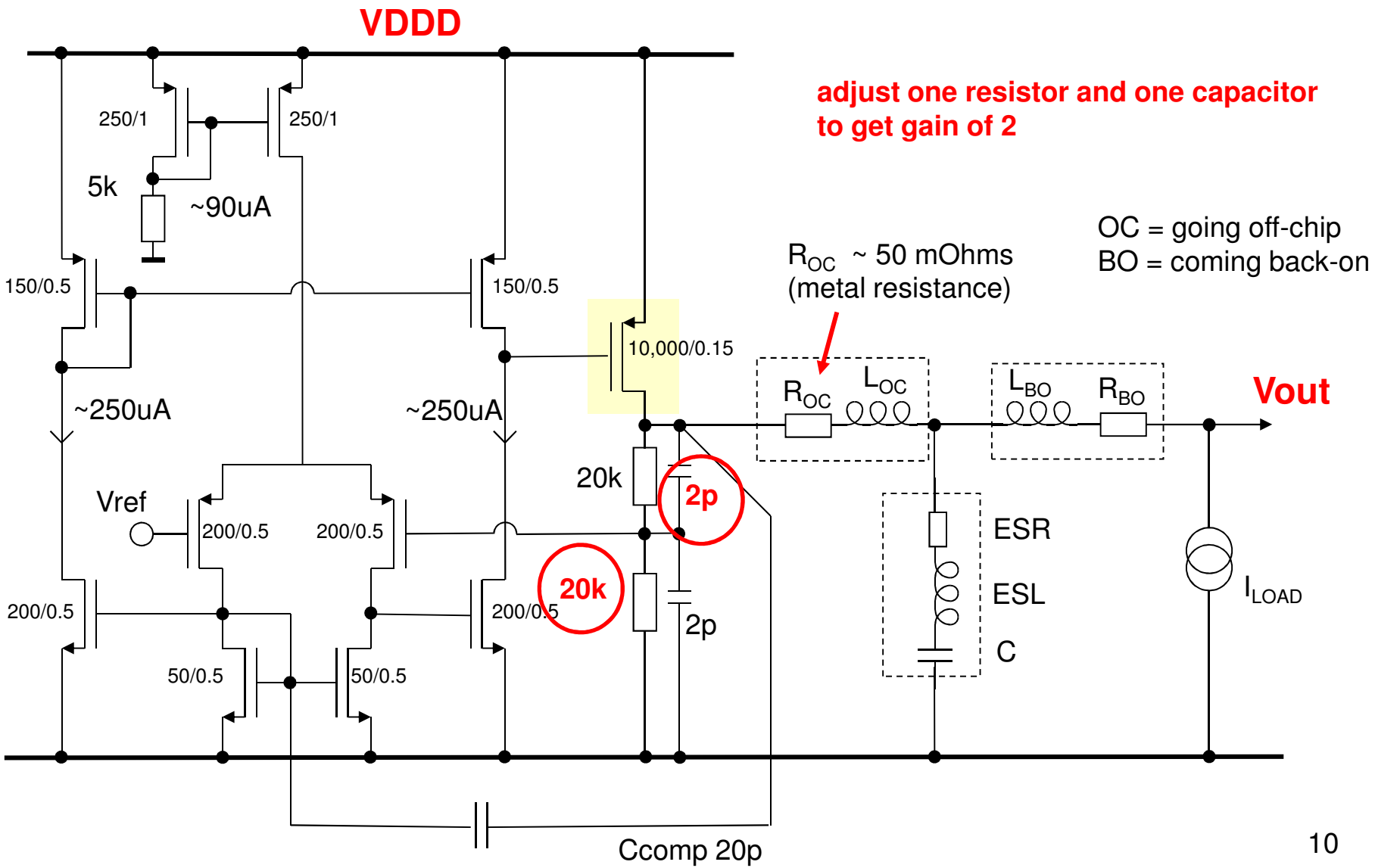


- VBGldo after trimming for process variation
  - Mean= 500mV
  - Range 499.2mV -> 500.8

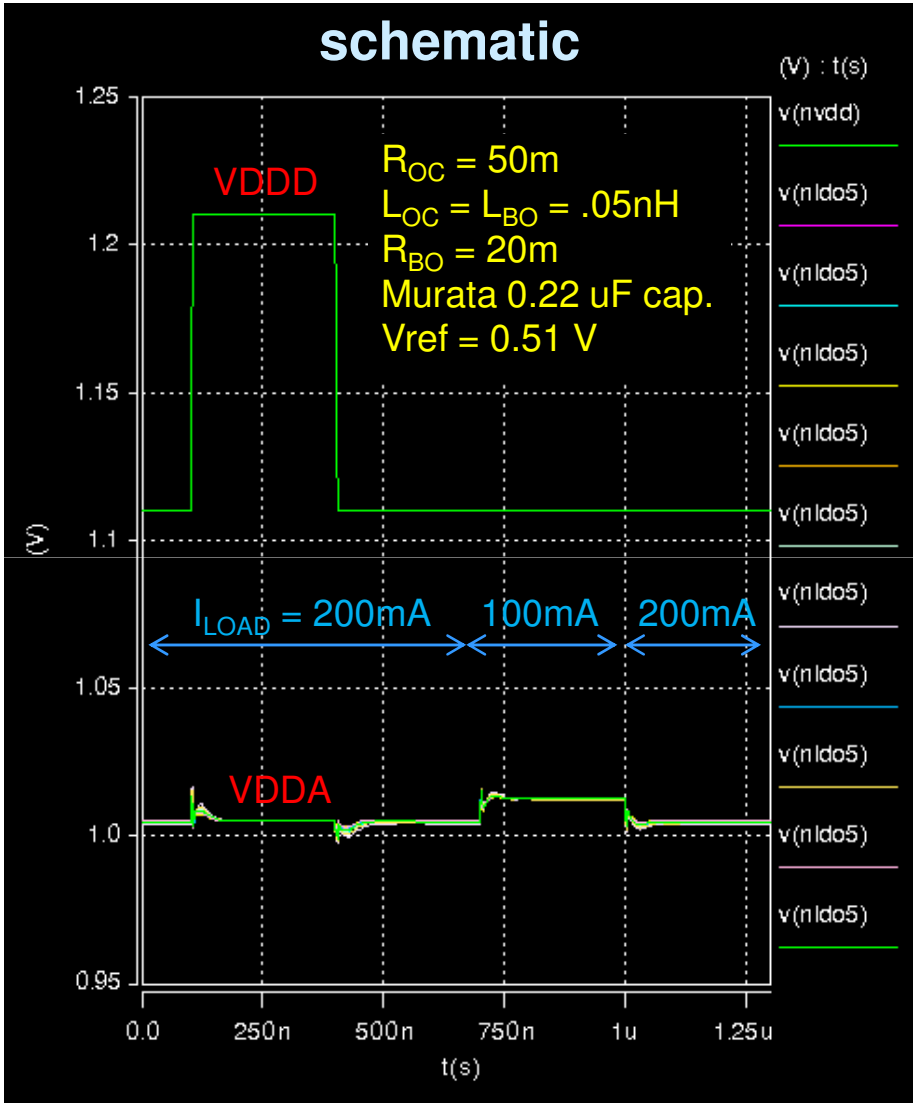
- Trim code used for process compensation
  - Mean= 36
  - Range 8 -> 51

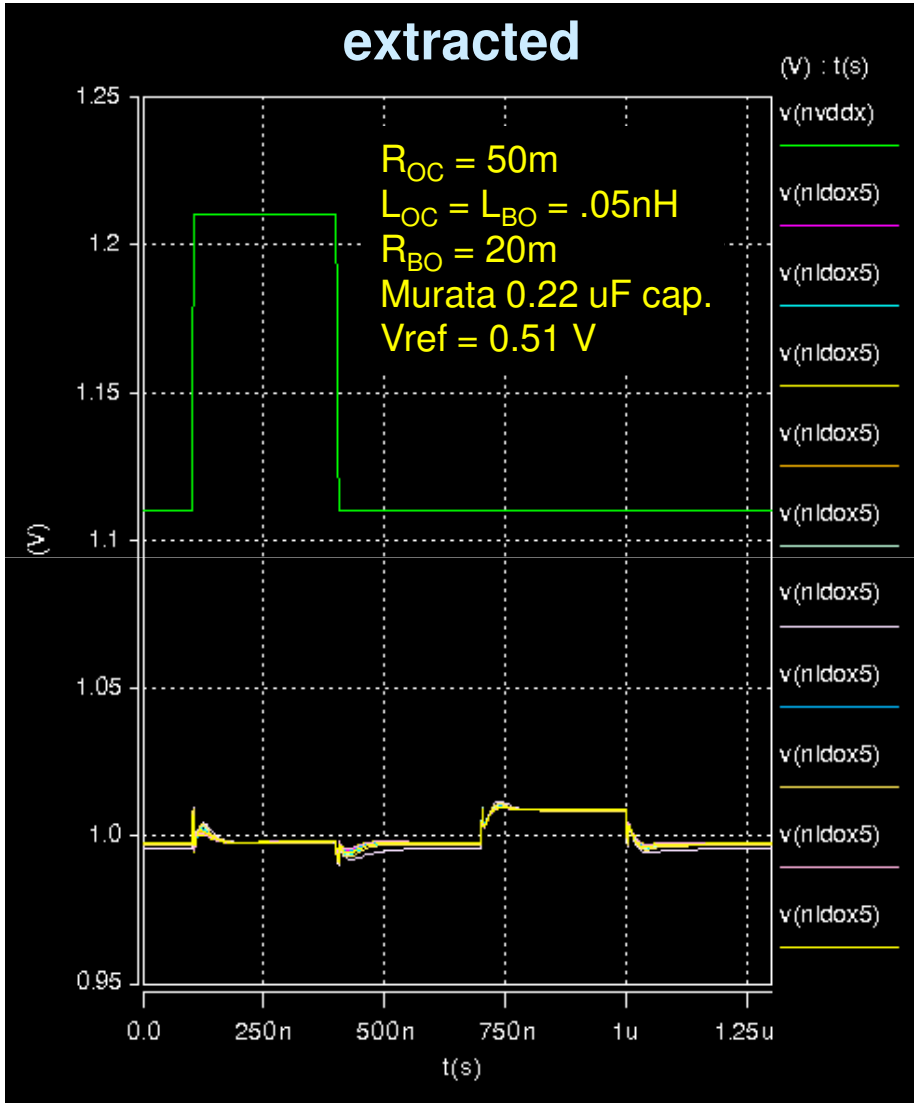
LDO

draws ~1200 µA from Vin



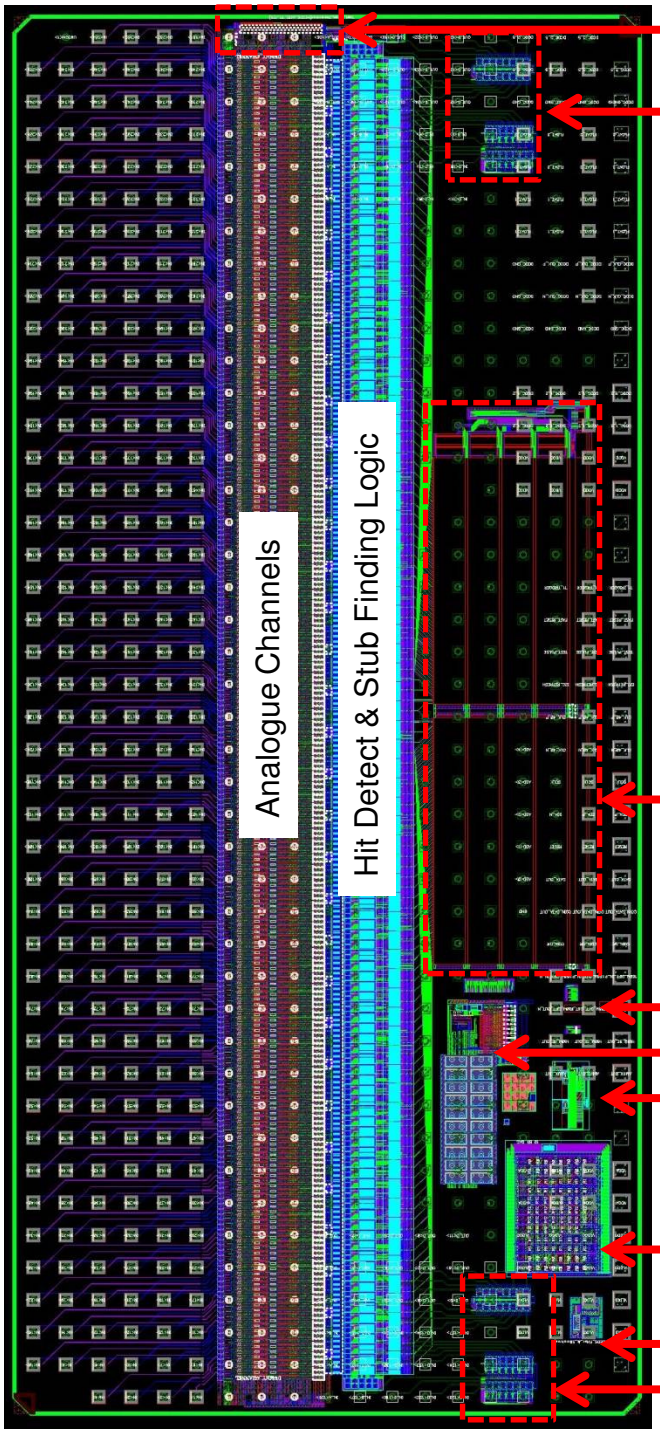
LDO schematic vs extracted: +40, -40, all corners





works ok down to VDDD = ~ 1.11

Top Level



test pulse circuit

I/O to neighbour

very congested in bottom right hand corner

all the blocks located there naturally want to be in close proximity

it is now clear that it will be necessary to increase width of chip by at least one column (250 um) (not yet implemented in this picture)

have agreed that vertical dimensions of chip can increase by 100 um at top and 100 um at bottom

512 deep pipeline & O/P buffer
(pipeline control logic now at top of chip)

efuses

I2C & biases

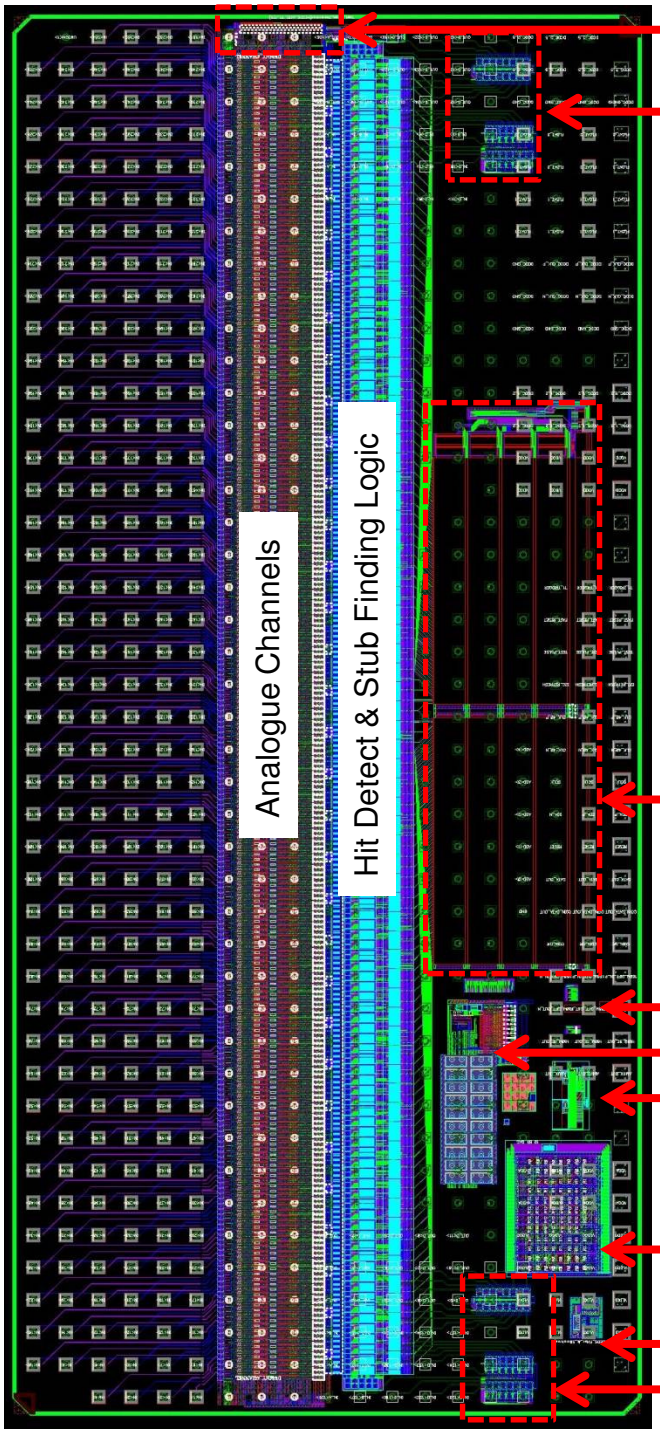
bandgap

10b DAC for VCTH

LDO

I/O to neighbour

Top Level



test pulse circuit

I/O to neighbour

note that pipeline and buffer ram have been flipped vertically so that control logic is at top of chip

helps with congestion in lower right hand corner

but one consequence is that channel order in triggered output data frame will be reversed compared with CBC2 - is that an issue?

512 deep pipeline & O/P buffer
(pipeline control logic now at top of chip)

efuses

I2C & biases

bandgap

10b DAC for VCTH

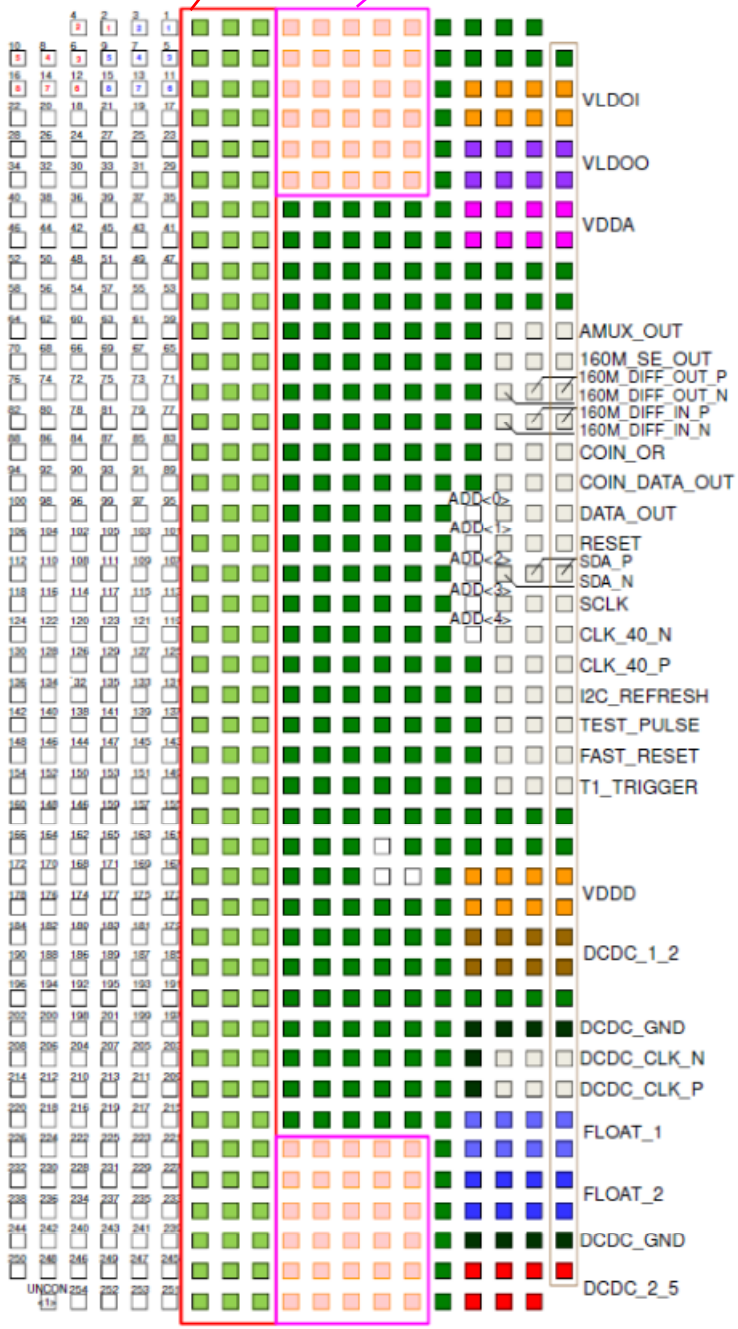
LDO

I/O to neighbour

CBC2

dummy pads on chip (no connection to chip ground)

interchip digital



pads as viewed through chip (i.e. pad pattern on hybrid)

CBC2: 43 rows, 19 cols
CBC3: 43 rows, 20 cols

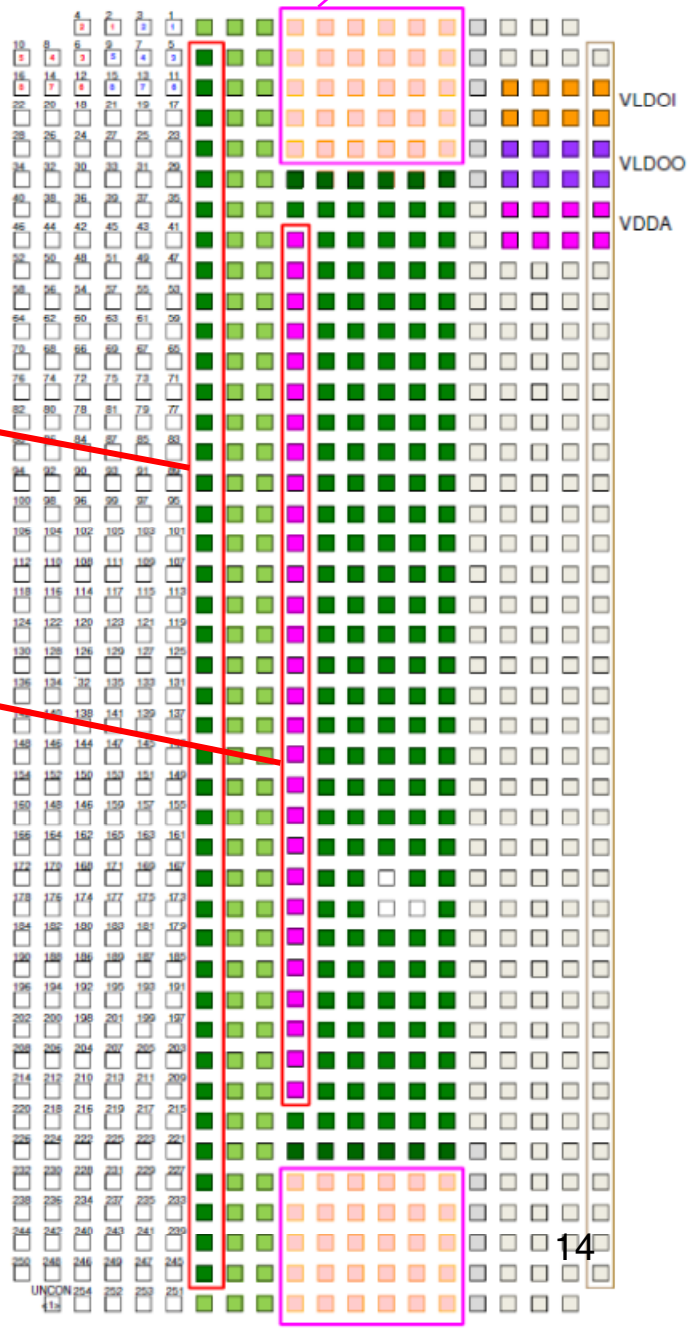
propose to replace these dummy pads (on CBC2) with GND pads on CBC3 connected internally to analogue front end

also propose to insert a column of pads to bring in VDDA close to analog front end

also note different orient-ation of interchip digital signals

CBC3

interchip digital



summary

I2C modifications incorporated into design and complete

Ck40 clock source changes incorporated into design - design not yet complete

can we swap pipe address and L1 counter fields in output data frame?

channel order in CBC3 triggered output data frame will be reversed cf. CBC2

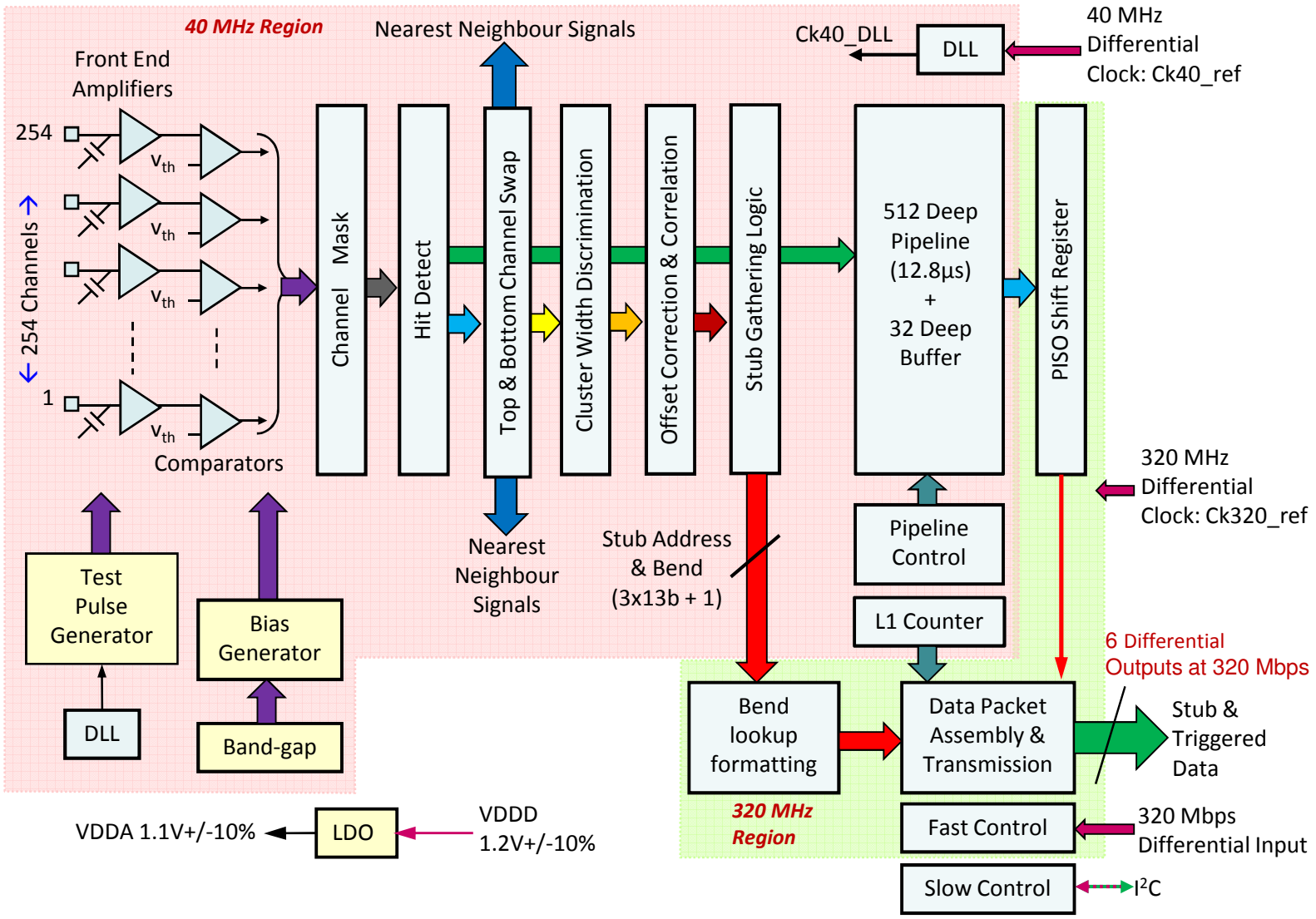
top level layout progress shows chip width has to grow by at least 1 column (250 um)

- will try to keep it to one column only

still hoping to be finished by end June

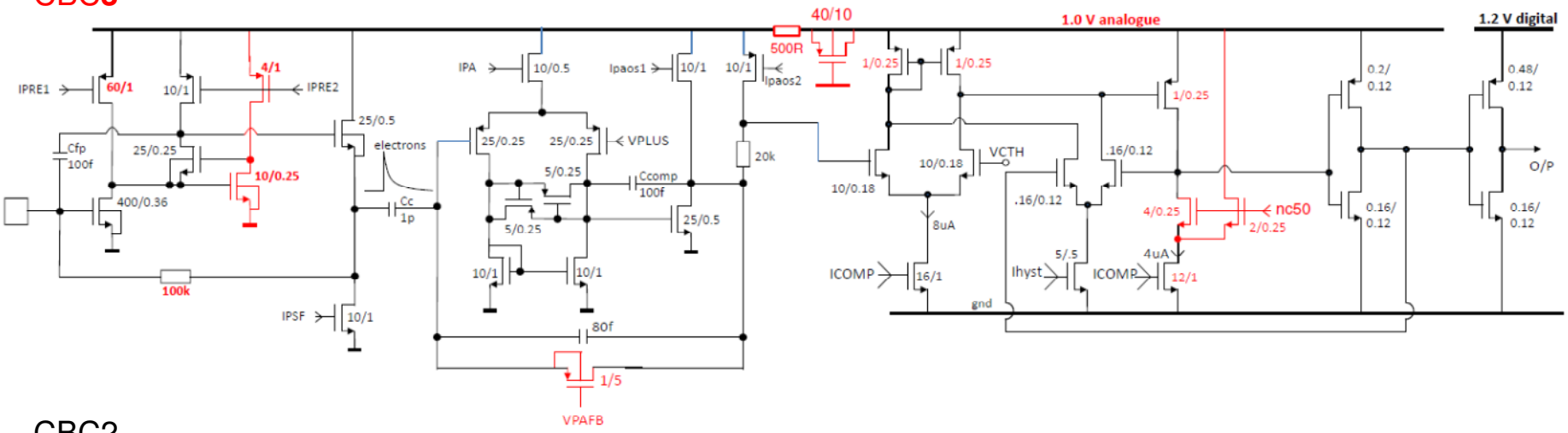
extra

for reference



front end design changes complete

CBC**3**



CBC2