CBC3 progress

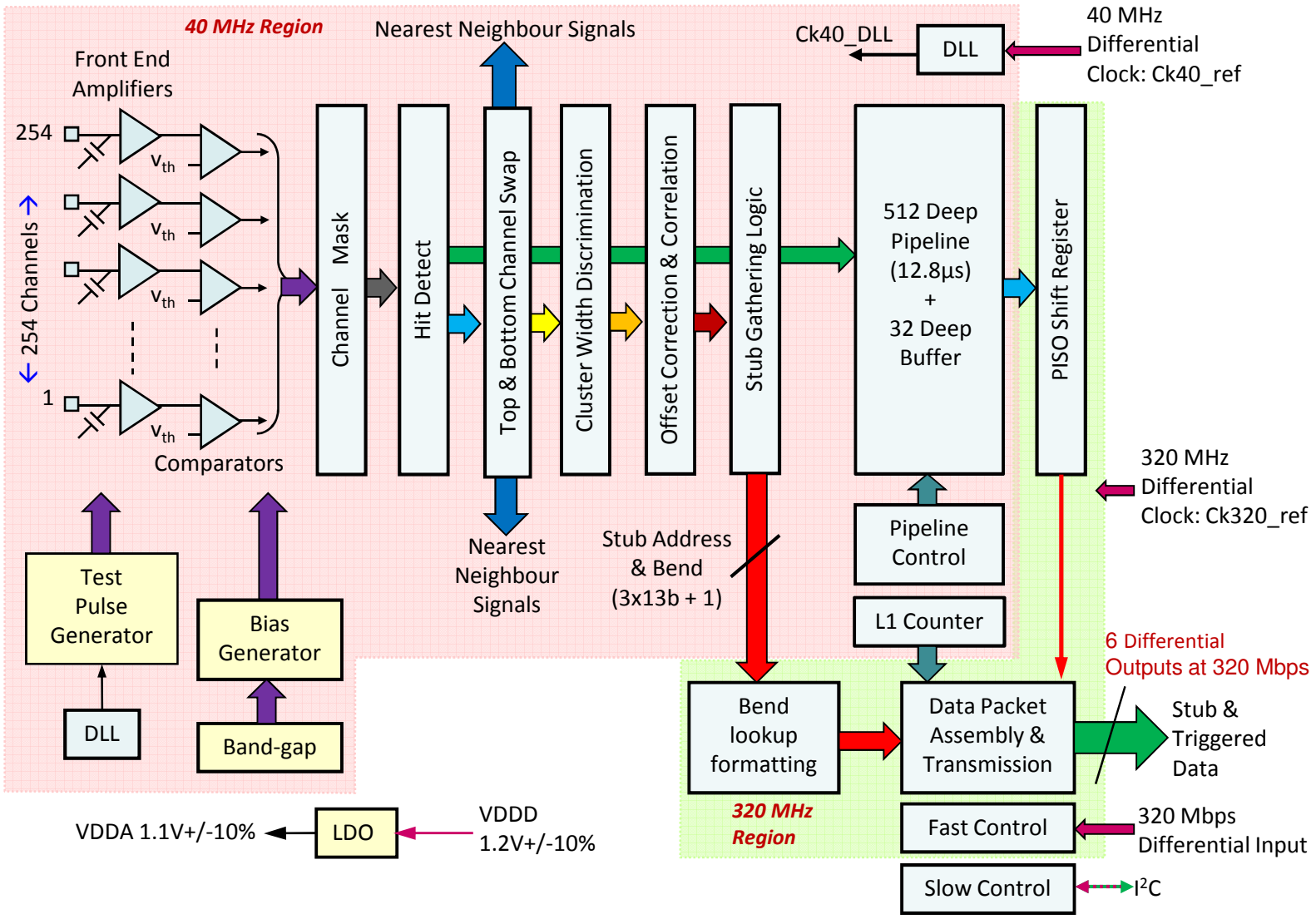
design progress
- VCTH DAC
- offset tuning modifications
- SLVS blocks

schedule

issues to raise

systems meeting, 19th January, 2016.

for reference

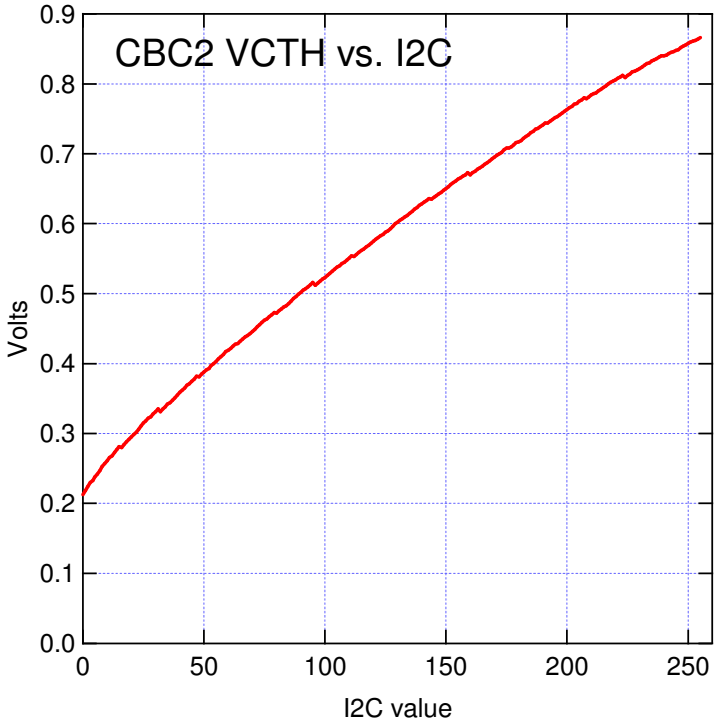


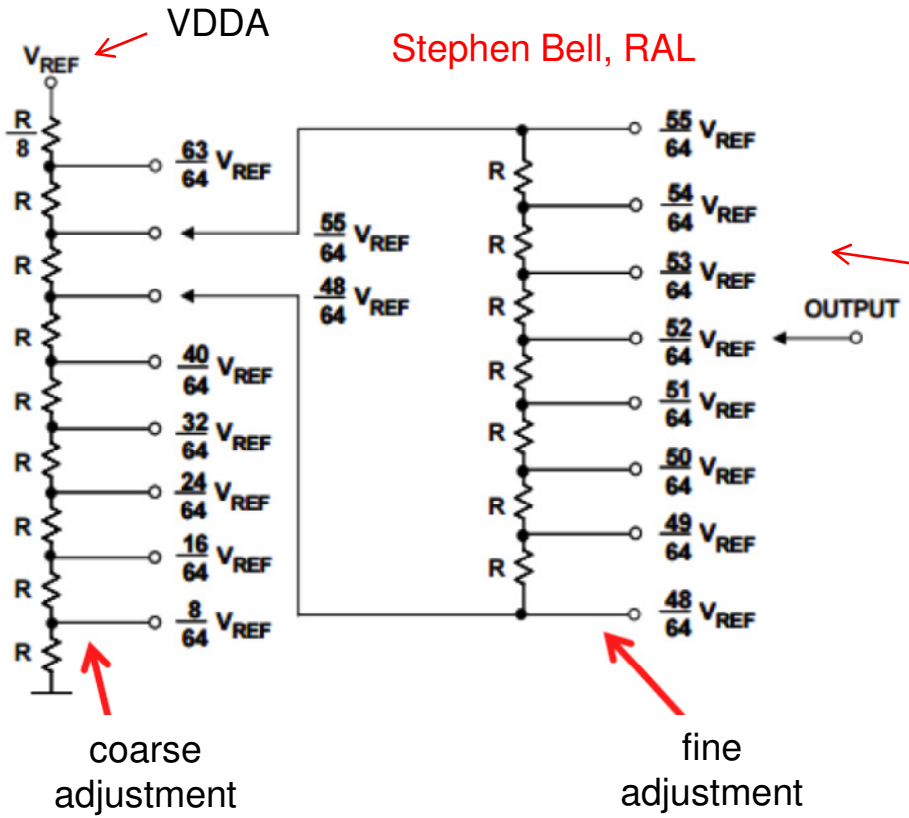
VCTH DAC

VCTH for CBC2 generated by mirroring adjustable current (8-bit res'n) into a resistor
not v. linear, and not monotonic

VCTH sweeps important diagnostic tool in binary system
used to measure efficiency, and noise

=> improve resolution and linearity for CBC3





VCTH in CBC3 to be implemented by segmented resistor ladder DAC architecture
~108 resistors -> 10-bit res'n
INL & DNL < 0.4 lsb
achieved for all simulation corners

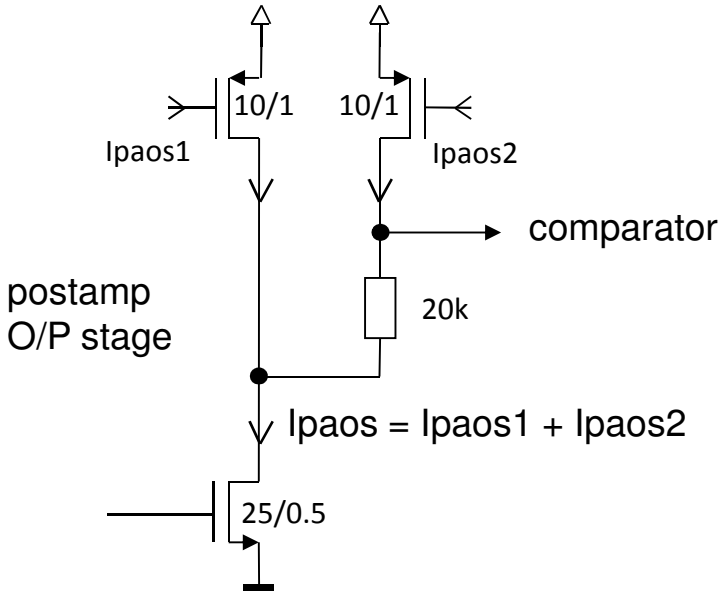
=> global threshold res'n ~ 140e

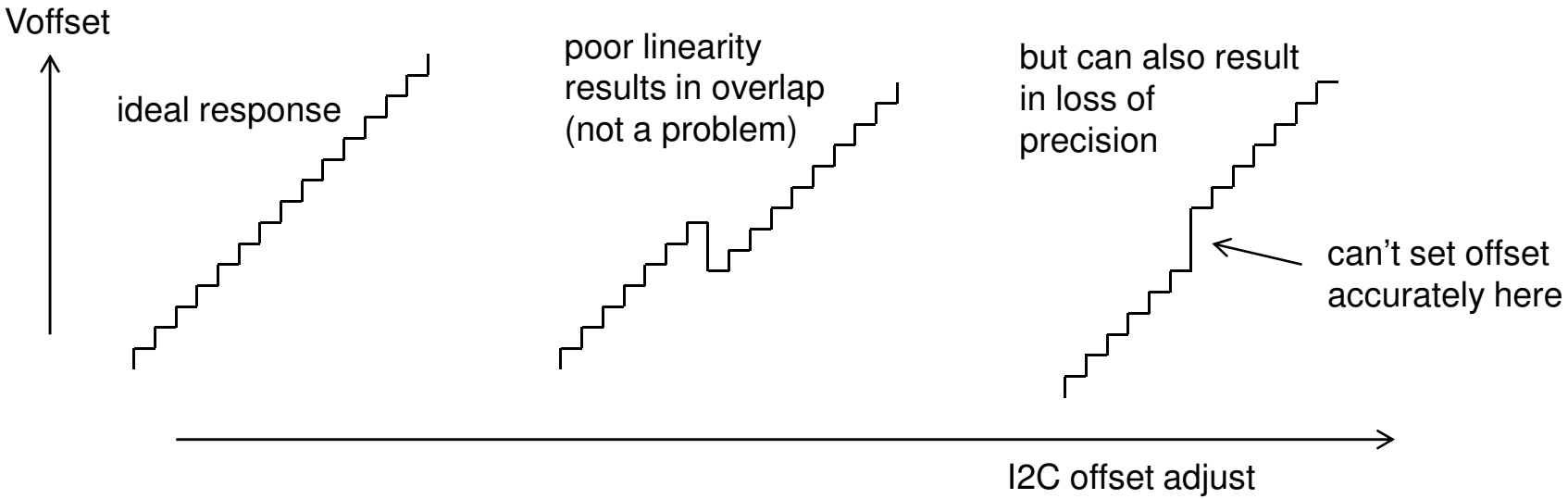
offsets tuning linearity

DC shift at postamp output (comp. I/P) produced by Ipaos2 current in 20k resistor

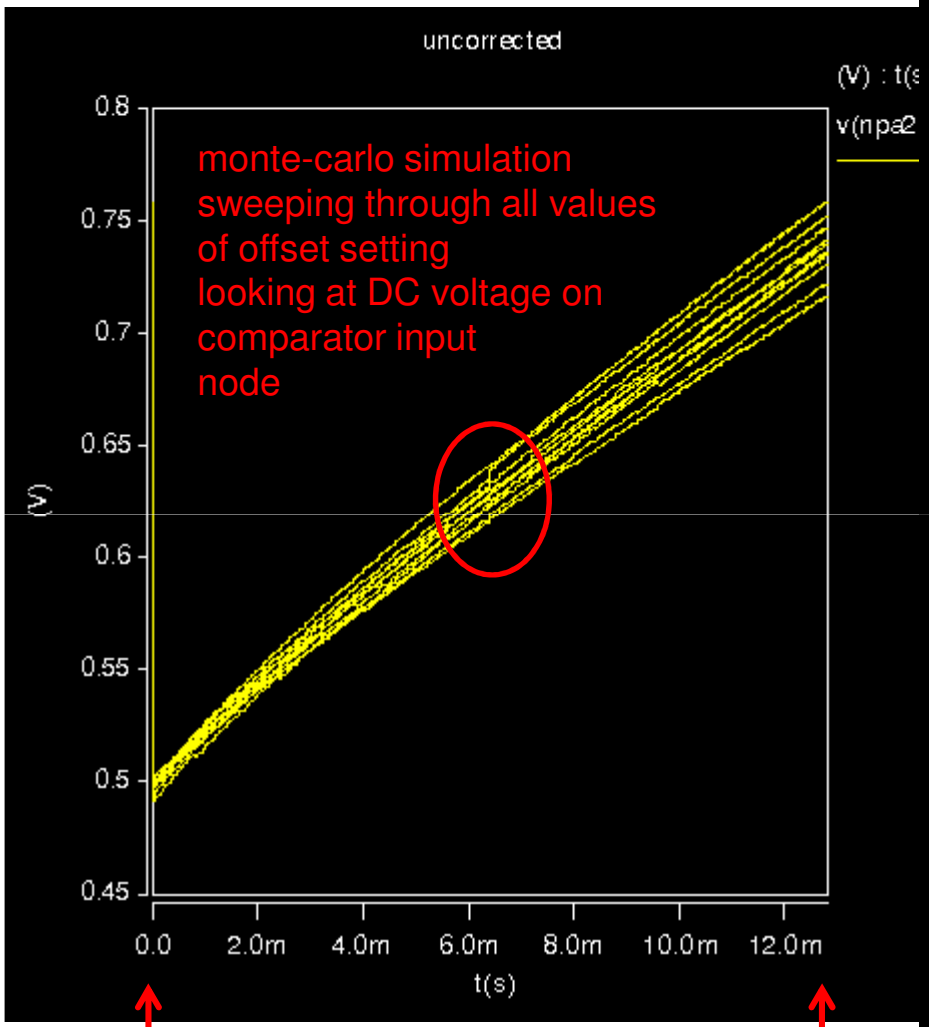
individual channel offsets adjust achieved by varying ratio of Ipaos1:Ipaos2 (total current Ipaos = constant)

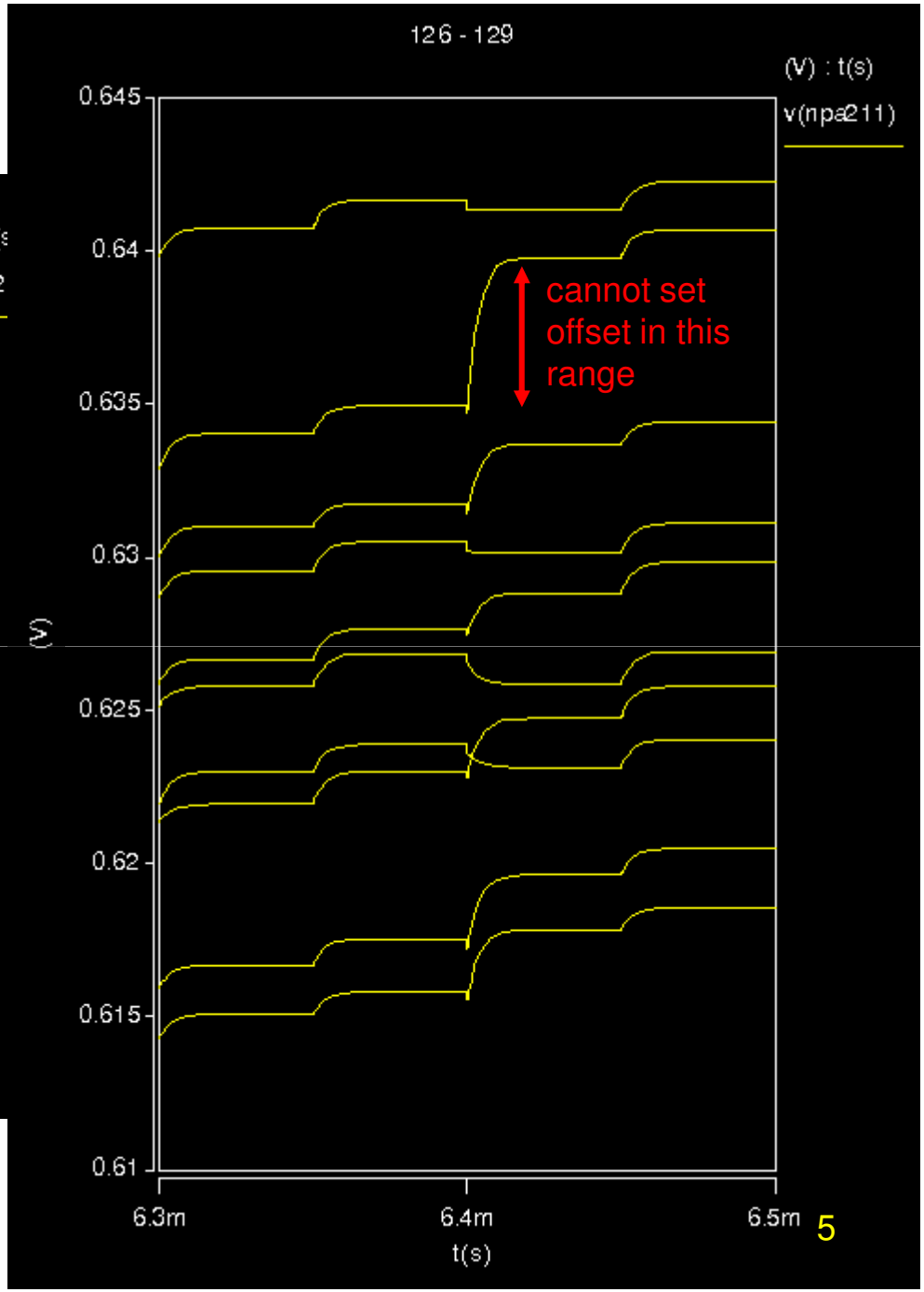
8-bit adjustment for nominal Ipaos = 10uA
gives 0.8mV /bit offset adjustment precision (~100e)
(for ideal DAC functionality)





CBC2 non-linearity simulated



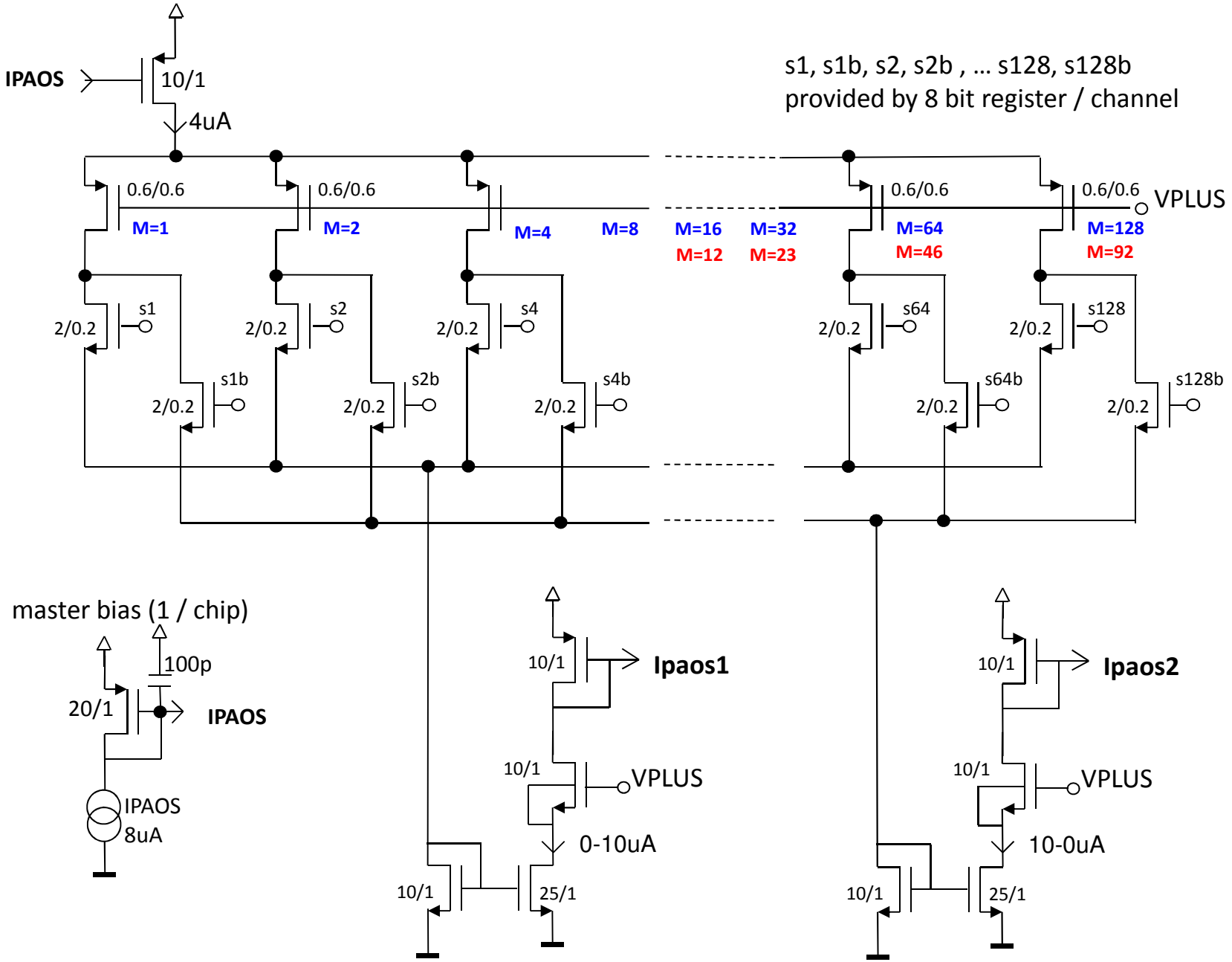


no current in
level shift resistor

maximum current in
level shift resistor

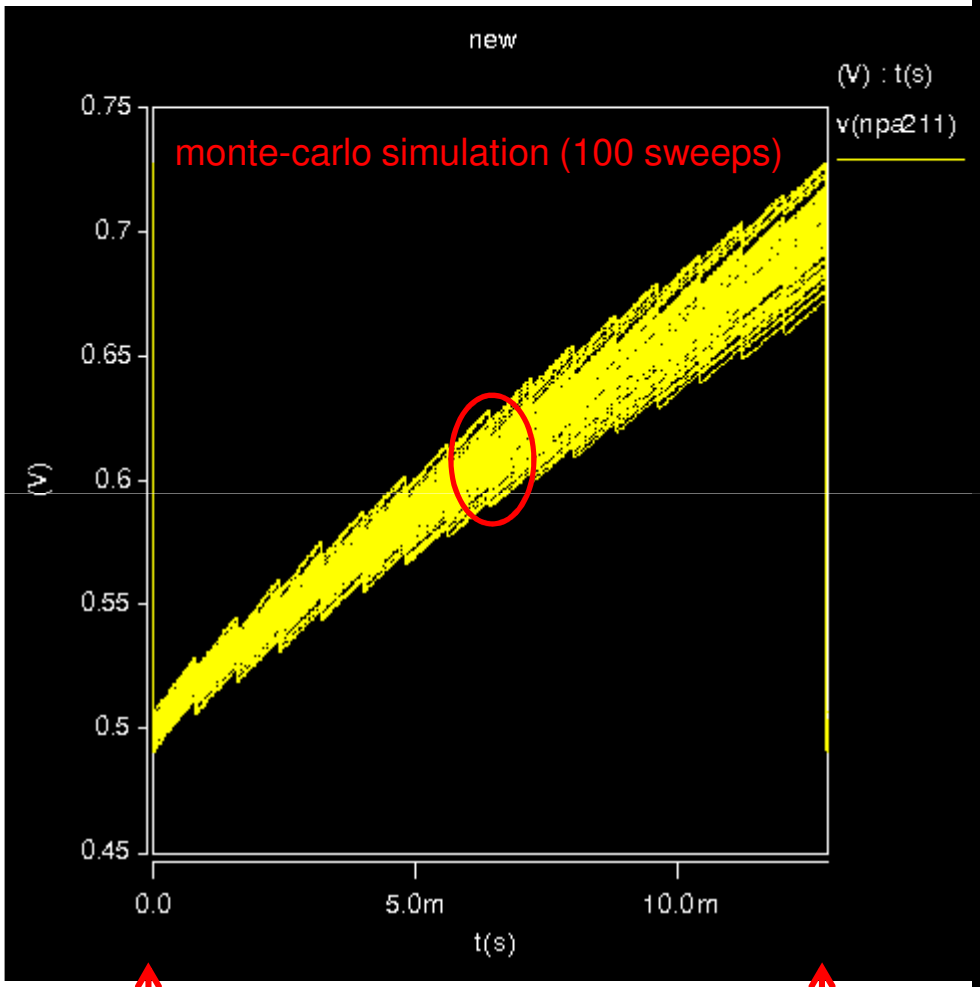
CBC2 -> CBC3 offset trim method

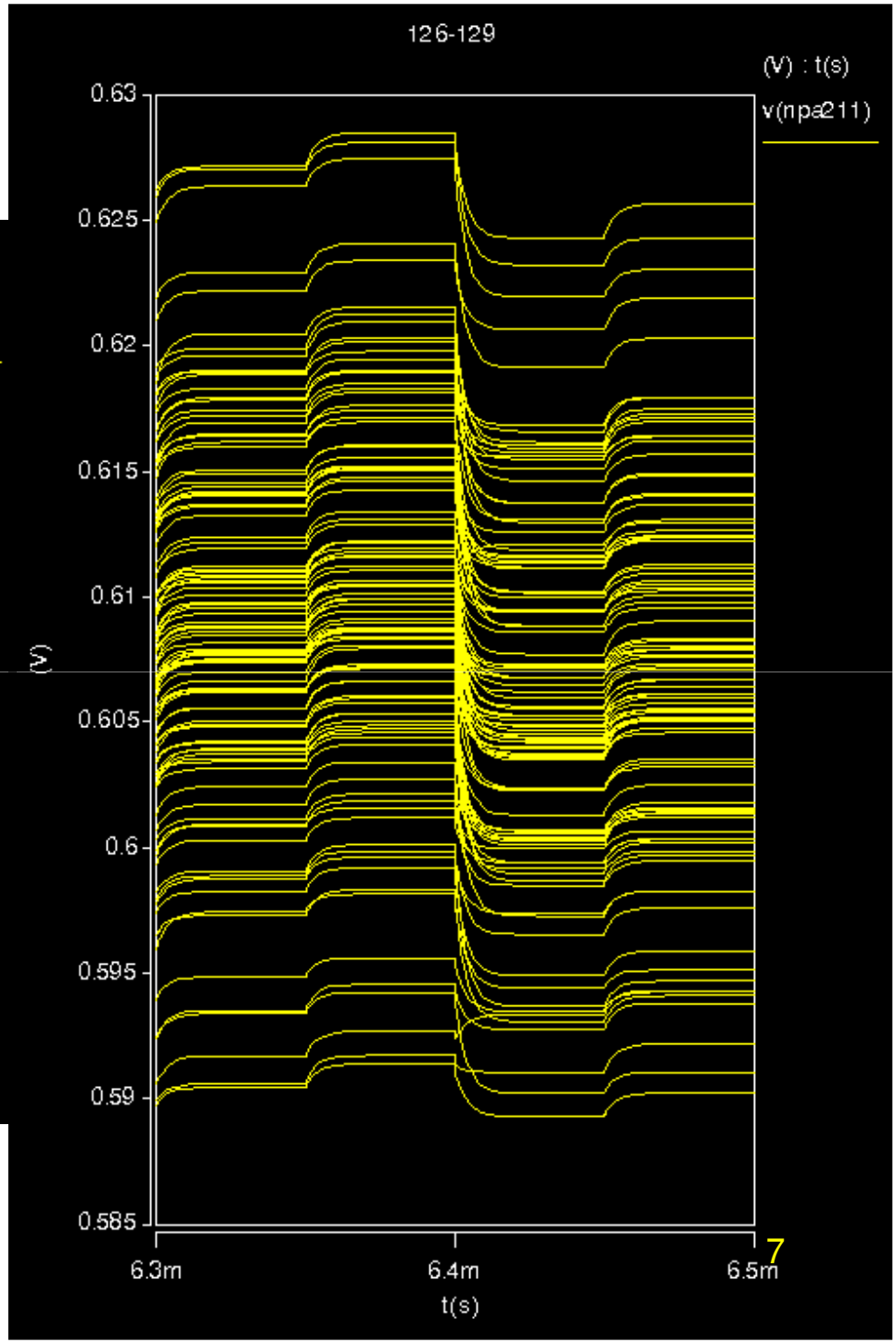
CBC2 values in blue
CBC3 values in red



non-linearity - but overlap

using CBC3 mirroring ratios



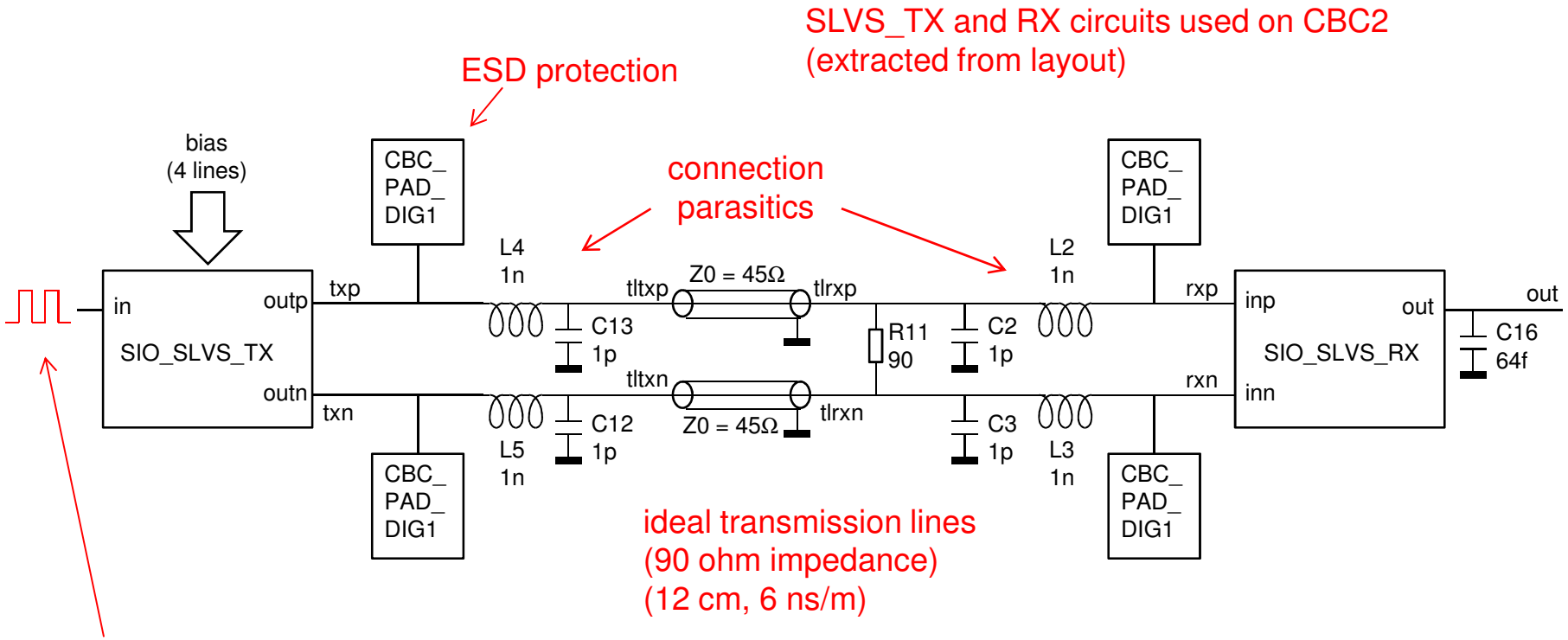


no current in
level shift resistor

maximum current in
level shift resistor

SLVS interfaces

SLVS used for 320 MHz clock and 320 Mbps fast control receiver, and 320 Mbps data out
TX and RX circuits provided by CERN (thanks)



SLVS simulation: T=+40

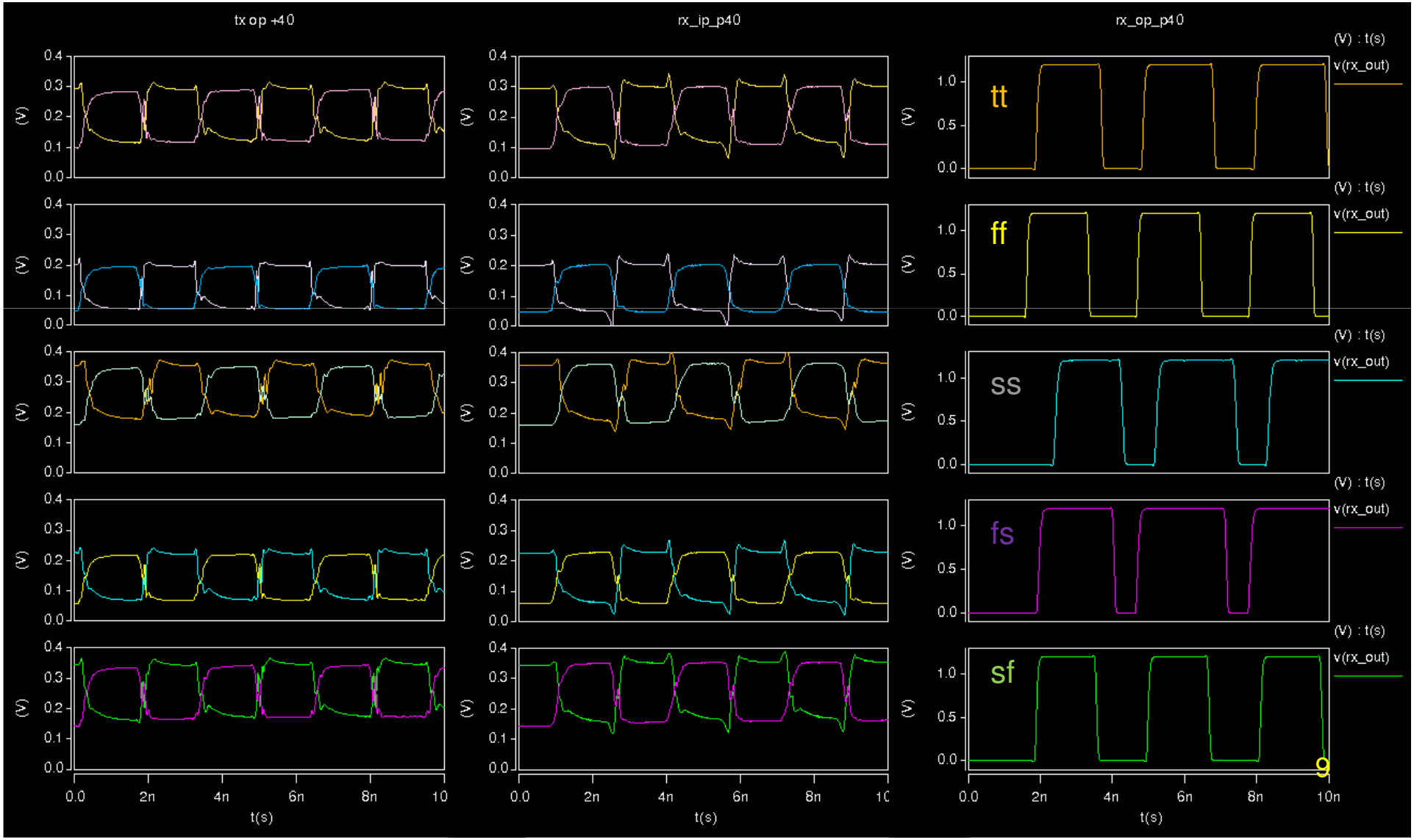
vdd = +1.2, T= +40, tx drive 1000

everything works - mark:space ratios at RX output not 50:50

at TX output

at RX input

at RX output



SLVS simulation: T=-40

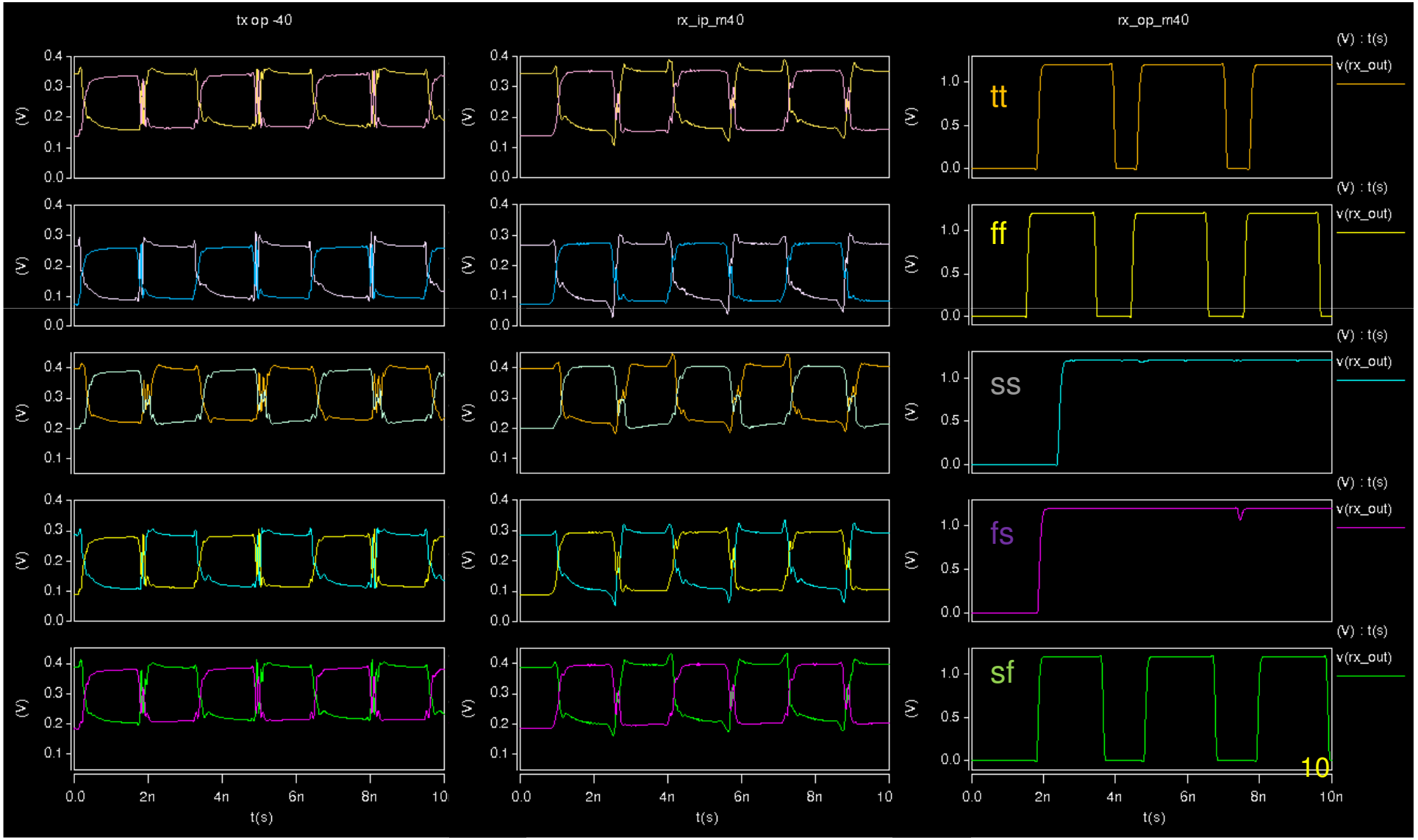
vdd = +1.2, T= -40, tx drive 1000

RX fails to recover clock for slow P corners

at TX output

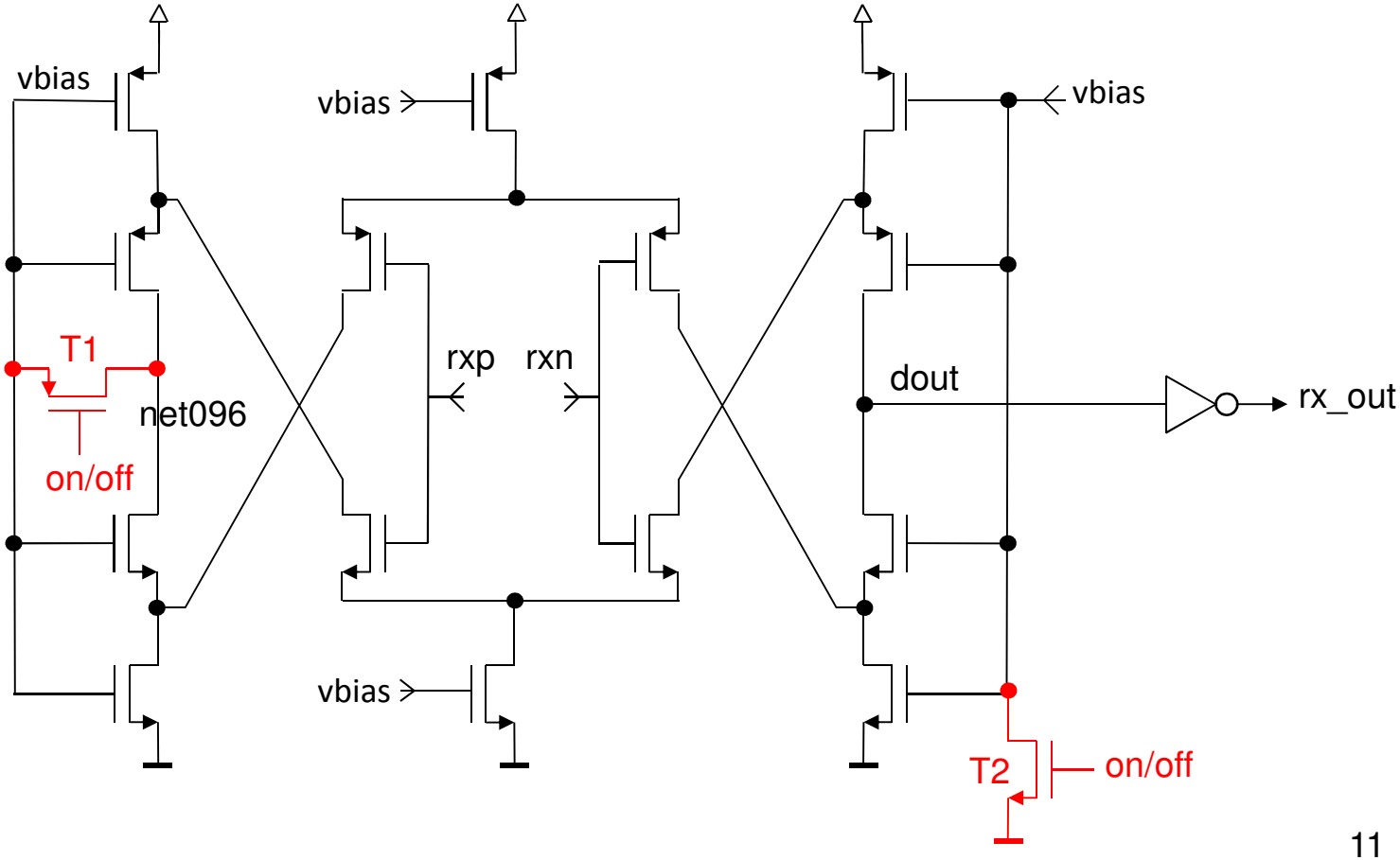
at RX input

at RX output



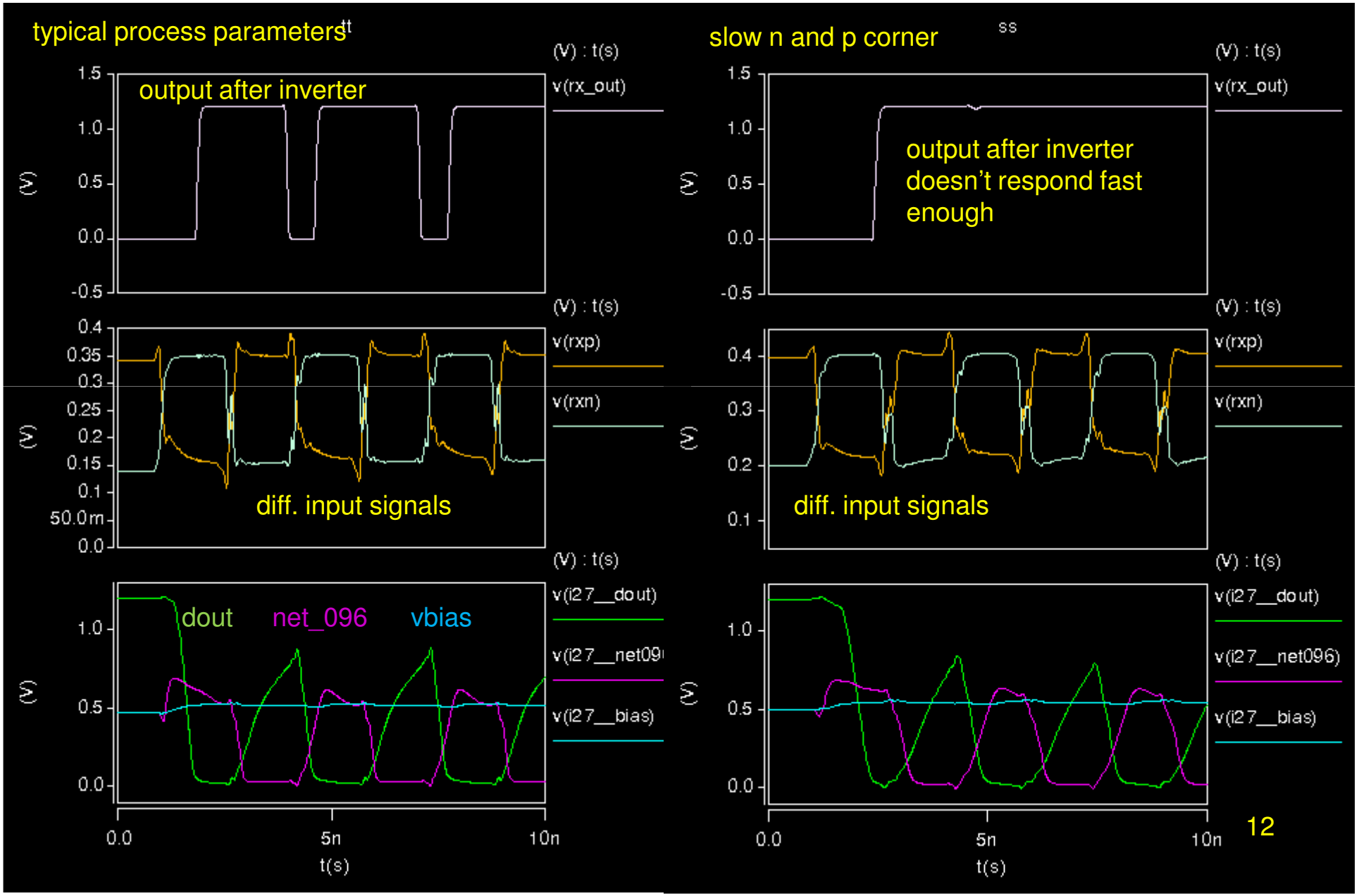
SLVS RX circuit details

2 transistors used to disable by disconnecting net096 from vbias, and shorting vbias to gnd
for normal operation net096 is connected to vbias by T1 andT2 is off
to switch off T1 is switched off and T2 is switched on to connect vbias to gnd



SLVS simulation: T=-40

net096 not closely coupled to vbias when swings negative
dout has stronger pull-down behaviour than pull-up

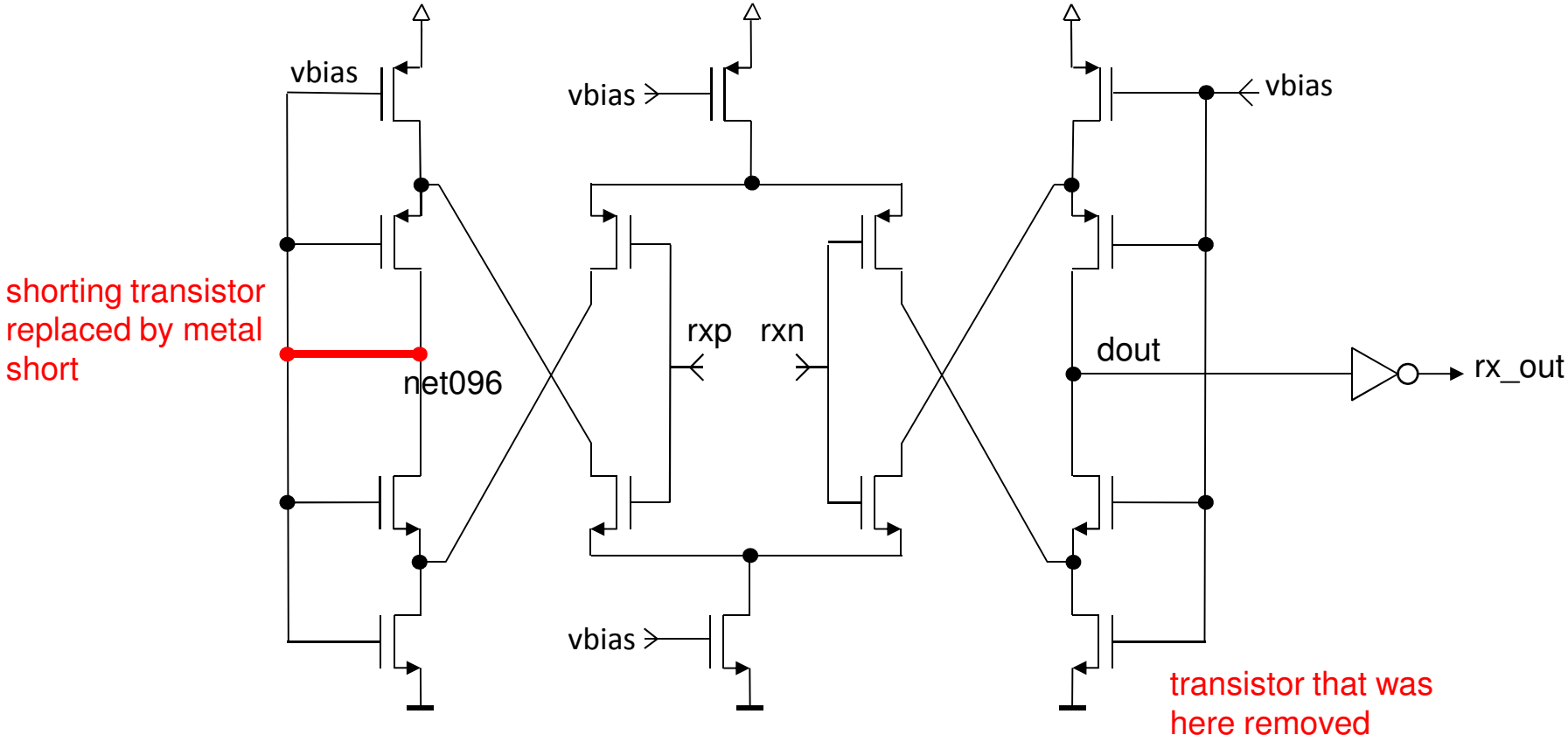


SLVS RX circuit details

can it be improved?

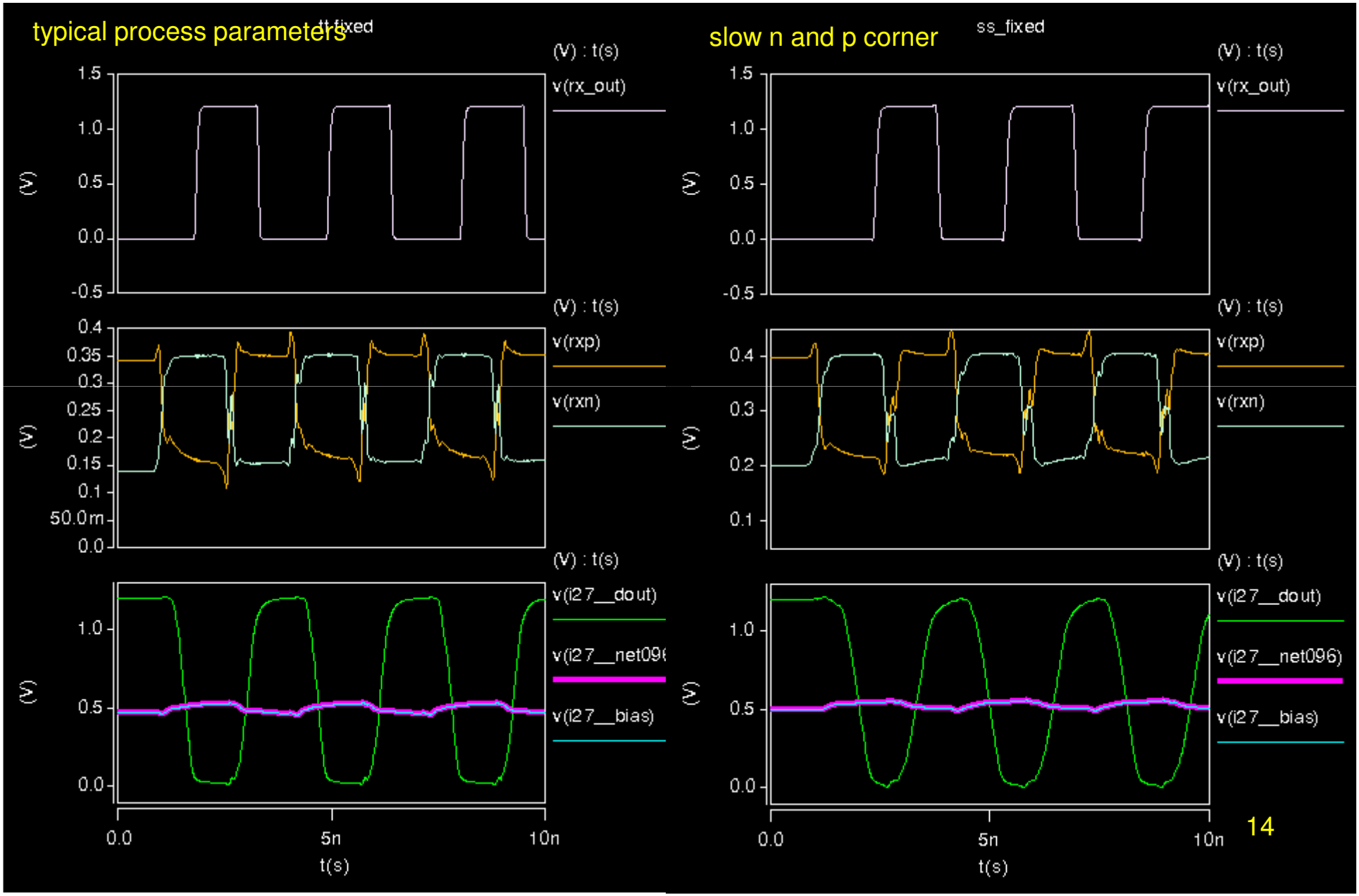
try removing disabling transistors and replacing one connecting vbias to net096 by a short

(this is the published version of the circuit - but obviously removes disabling functionality)



SLVS RX simulation: T=-40

net096 now same as vbias and circuit behaves much better

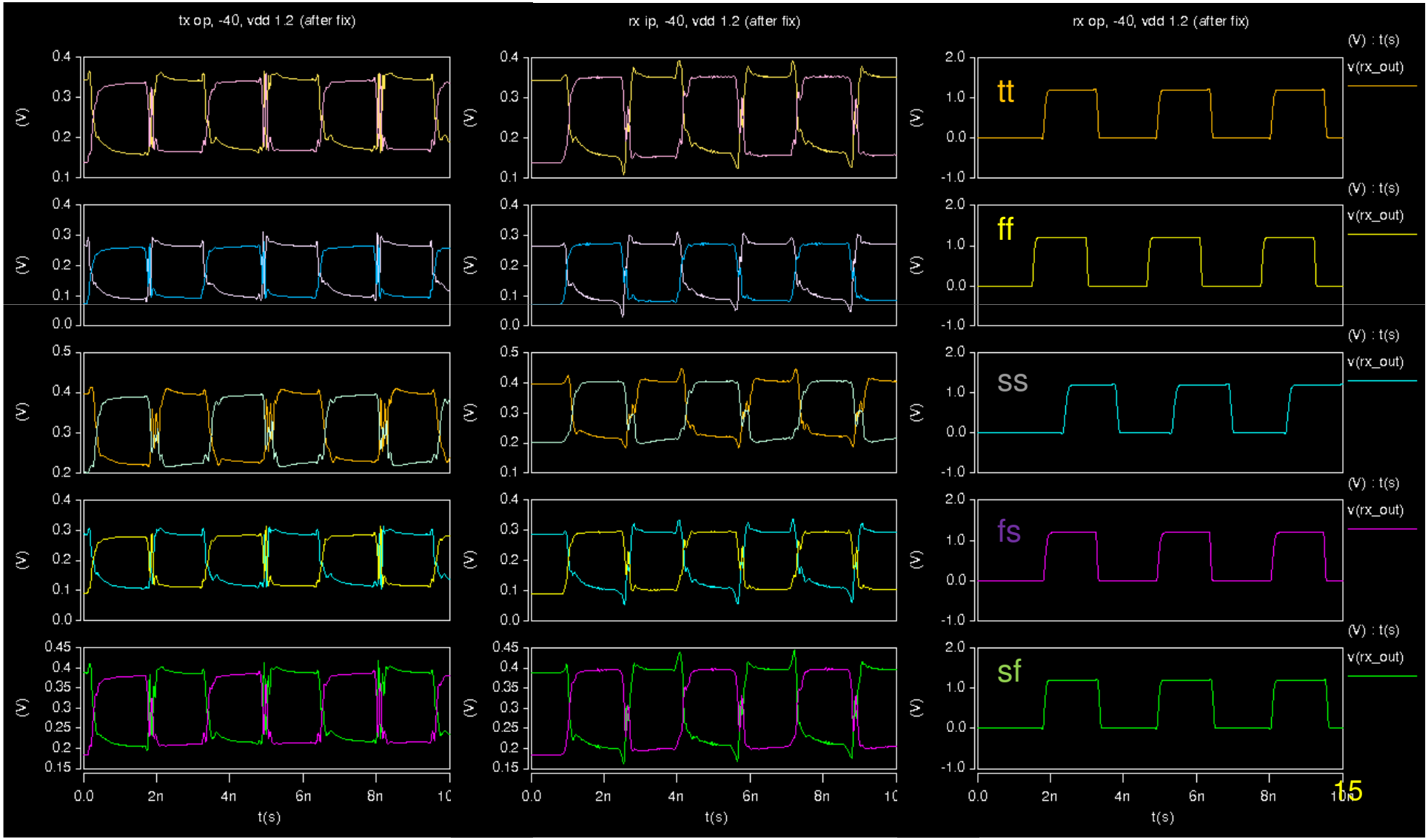


SLVS simulation: T=-40

vdd = +1.2, T= -40, tx drive 1000

RX circuit successfully recovers 320 MHz clock for all simulation conditions
(process corners, -40, +40, VDD 1.1 to 1.3V - results after layout modified and extracted)

at TX output | at RX input | at RX output



schedule

as mentioned last time, have suffered from staff loss at RAL

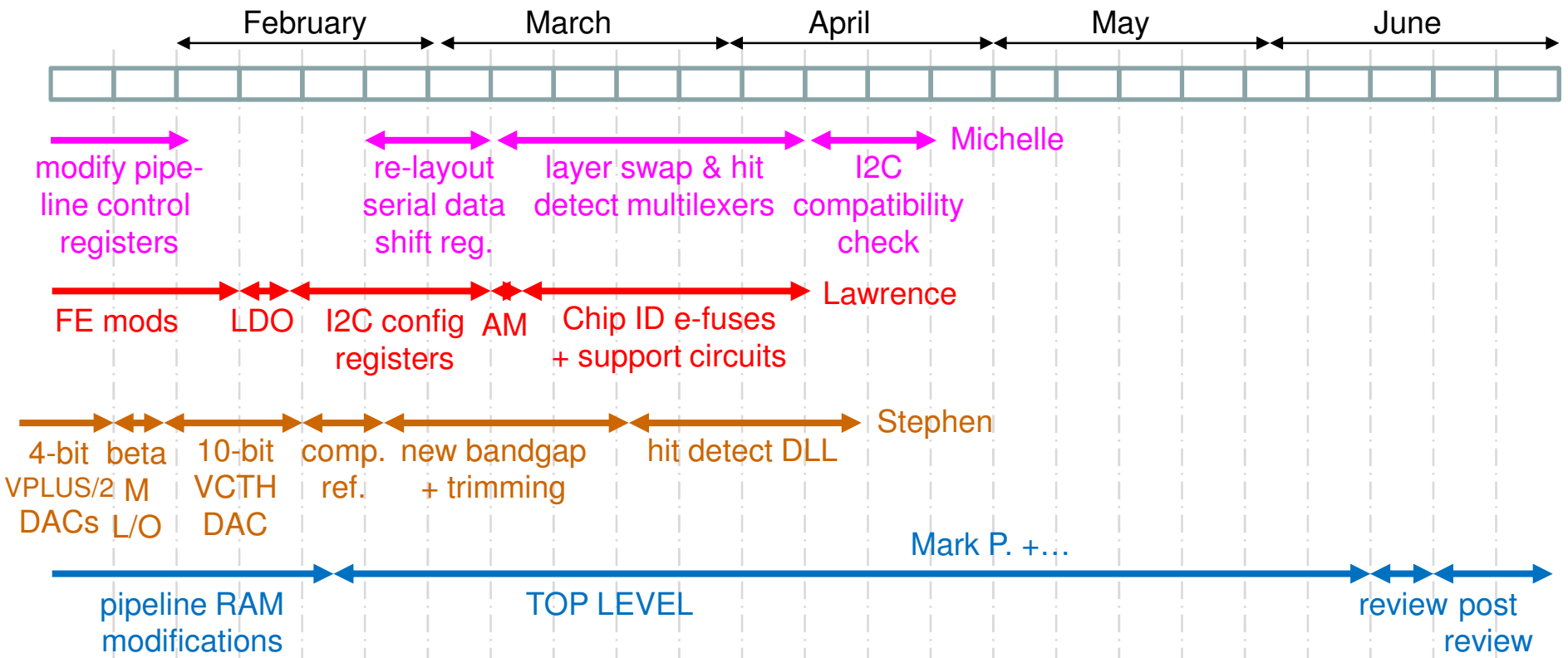
Lawrence Jones and Stephen Bell now allocated to CBC3

a few previouly unforeseen additions to the design now incorporated

new bandgap+trimming, e-fuses, FE mods a bit more extensive than expected,..

project schedule to completion has now been revised (Mark Prydderch)

schedule



all design blocks complete by ~mid April
but TOP level work takes till June
(assembly of complete chip, connecting up, checking,..)
can probably provide information needed for reticle assembly earlier

questions to raise

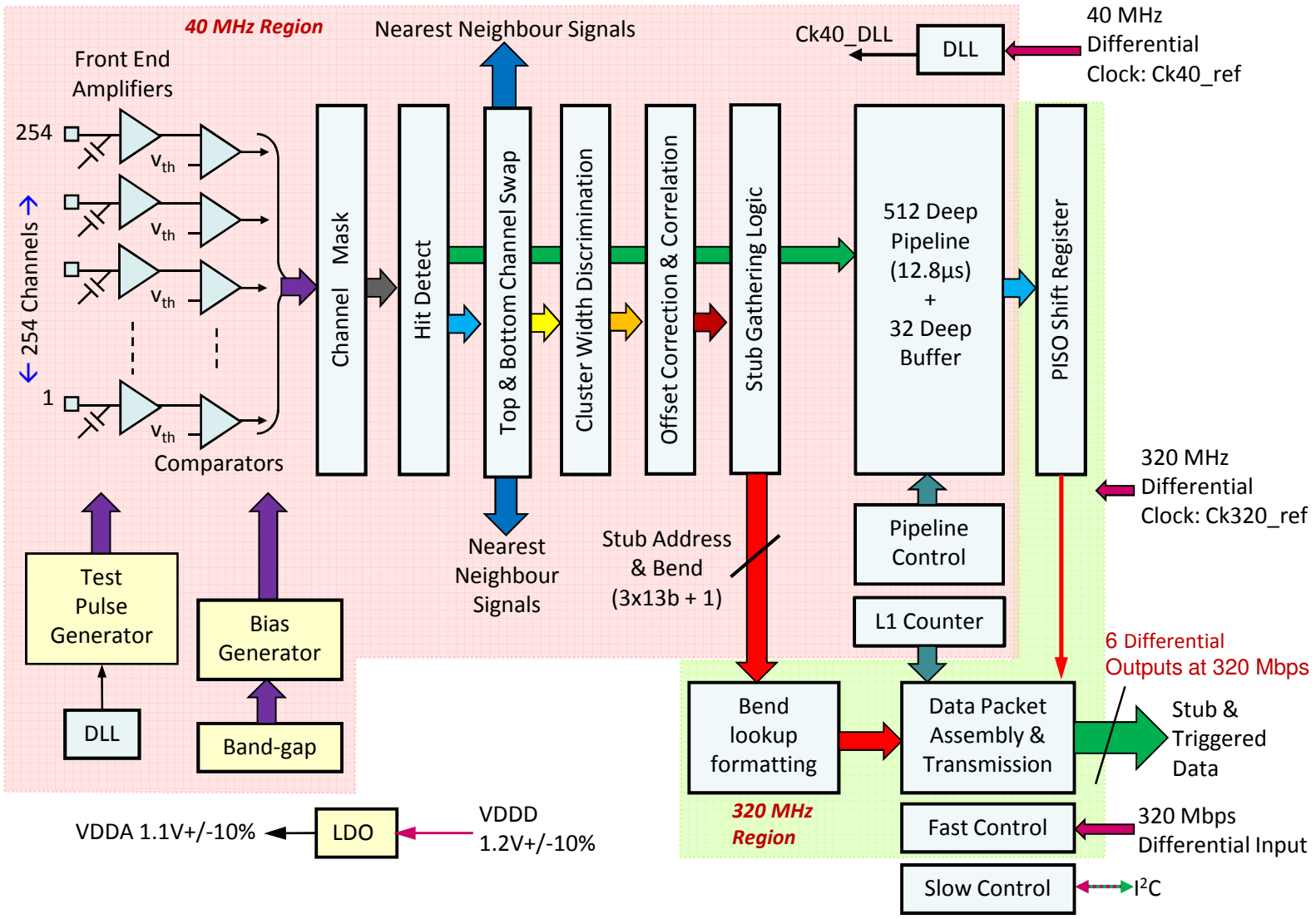
will CBC3 delay jeopardize joint submission with GBT-SCA?

would like to have a clear picture of:

- wafer sharing details
  - likely area ratio of CBC:GBT-SCA?
    - (what are cost implications for UK budget?)
- bump-bond technology
  - who will do it?
  - factors affecting pad design?
    - passivation opening, shape, ..

extra

for reference



CBC3 digital interfaces

reminder of main changes/new features

stub gathering logic, address and bend transmission
- 8 bit stub seed address (1/2 strip resolution)
- 4 bit bend info (location of cluster in window layer)

up to 3 stubs data transmitted to CIC /BX
- 6 diff pairs @ 320 Mbps

pipeline cell modifications and length increase (12.8usec)

single 320 Mbps fast control line

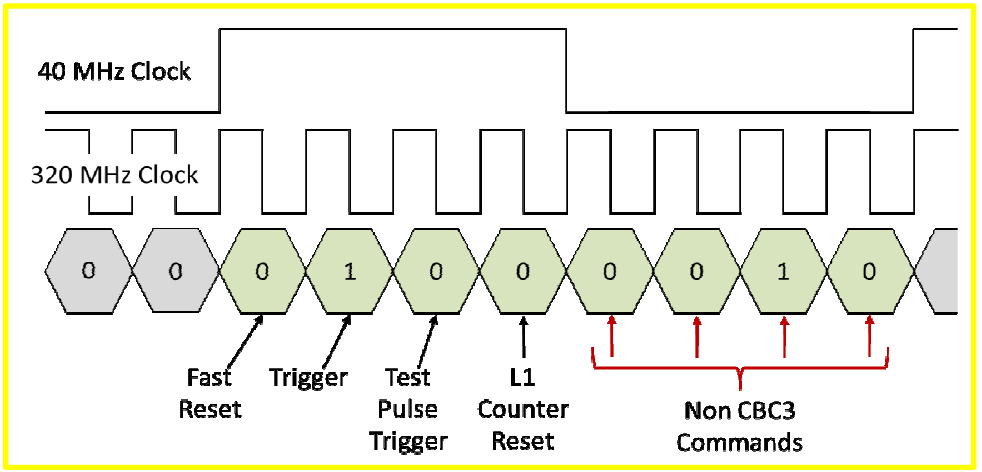
up to 1 MHz L1 triggering capability
- readout data frame < 1 usec

output data

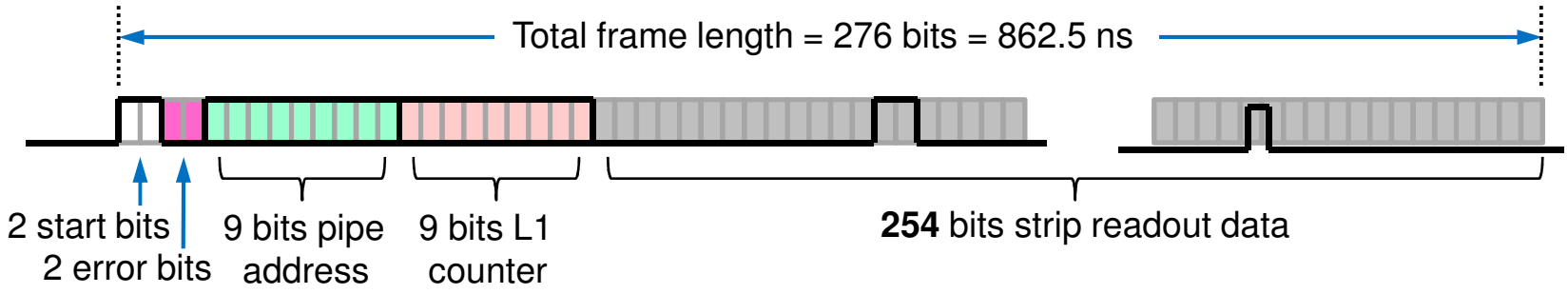
25 ns

S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B2	SoF	**R**
S1	S2	S3	B2	OR254	**R**
S1	S2	S3	B2	Error	**R**
S1	S2	S3	B2	**Sync**	**R**

(R = L1 triggered readout data)

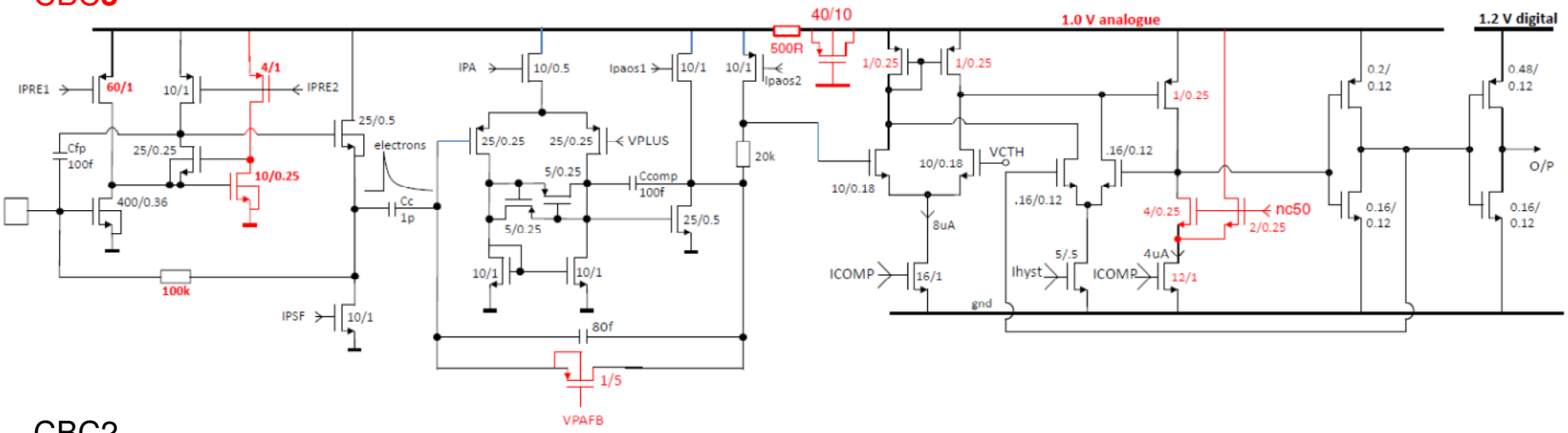


Readout data frame



front end design changes complete

CBC**3**



CBC2