CBC3 progress

issues raised last time

- changes to test pulse wiring to allow easy detection of shorted channels
  - turns out to be unnecessary (next slide)

- some changes proposed to output data fields and order
  - outcome of subsequent discussions:
    - pipe address and L1 data fields remain as they were
    - L1 triggered data channel order reversed

- further CIC/CBC3 discrepancies found since (spec. document)
  - have been resolved & will present “final” spec. today

CBC3 progress and status

systems meeting, 7th June, 2016.

test pulse wiring

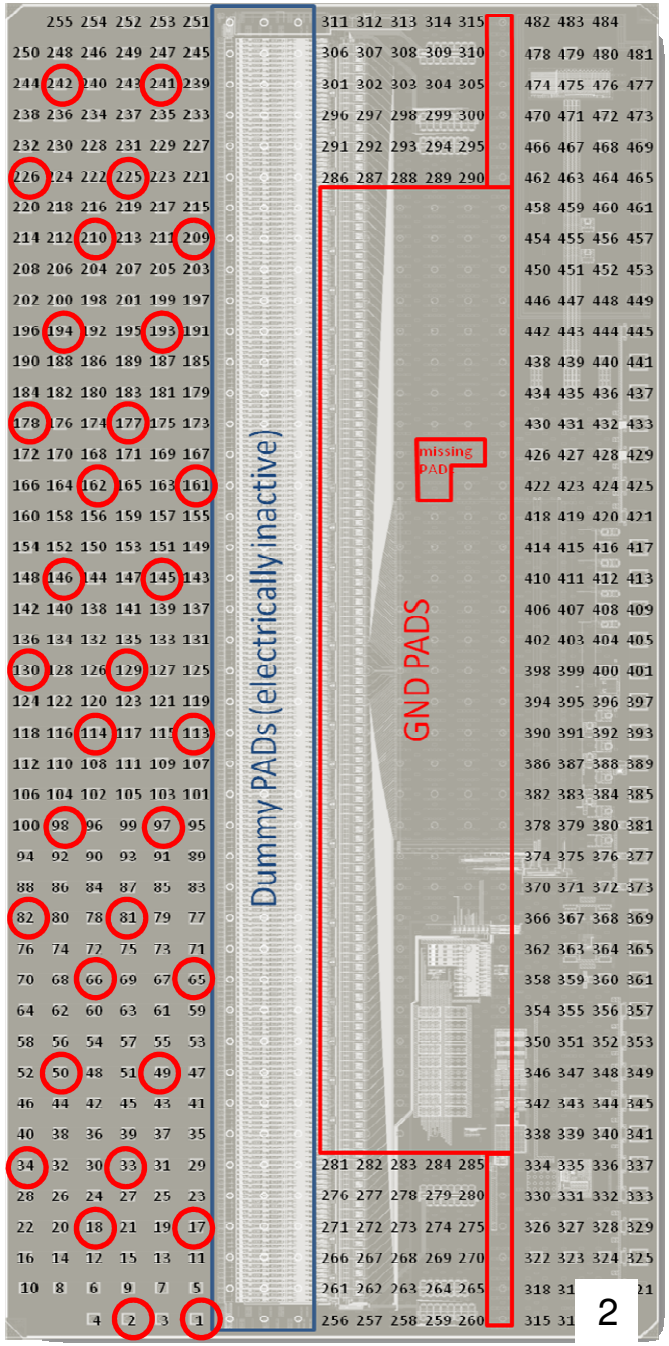
concern that test pulse grouping would not allow easy detection of neighbouring channel shorts

e.g. test group 1 involves channels 1,2,17,18,33,34,…

but actually turns out that channels 1 & 2, 17 & 18, … are not neighbouring in layout

other test groups follow same pattern

so turns out that this is not an issue



output data

until recently CBC3 spec. document stated:

*"The direction of time flow is **top** to **bottom**, i.e. Stub1<0> is output first"*

Francois spotted inconsistency between this and CIC spec., where CIC is expecting opposite time flow direction

25 ns

SLVS<1>	SLVS<2>	SLVS<3>	SLVS<4>	SLVS<5>	SLVS<6>
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	**R**
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	**R**
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	**R**
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	**R**
S1<4>	S2<4>	S3<4>	B2<0>	SoF	**R**
S1<5>	S2<5>	S3<5>	B2<1>	OR254	**R**
S1<6>	S2<6>	S3<6>	B2<2>	Error	**R**
S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	**R**

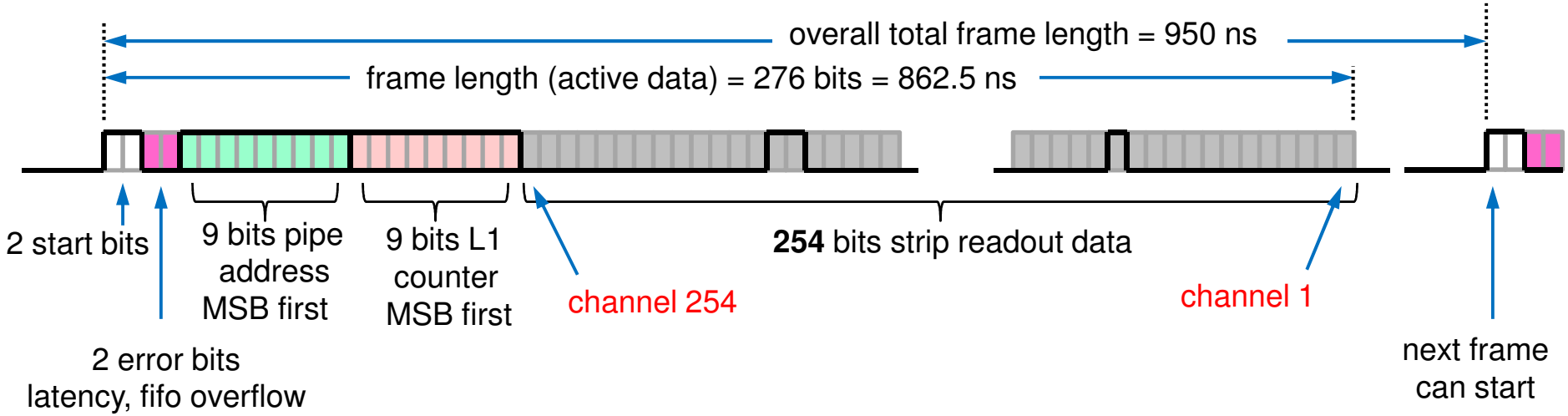
This has now been fixed in design (fortunately not difficult to do)

CBC3 spec. document has been updated (now version 1.3) to read

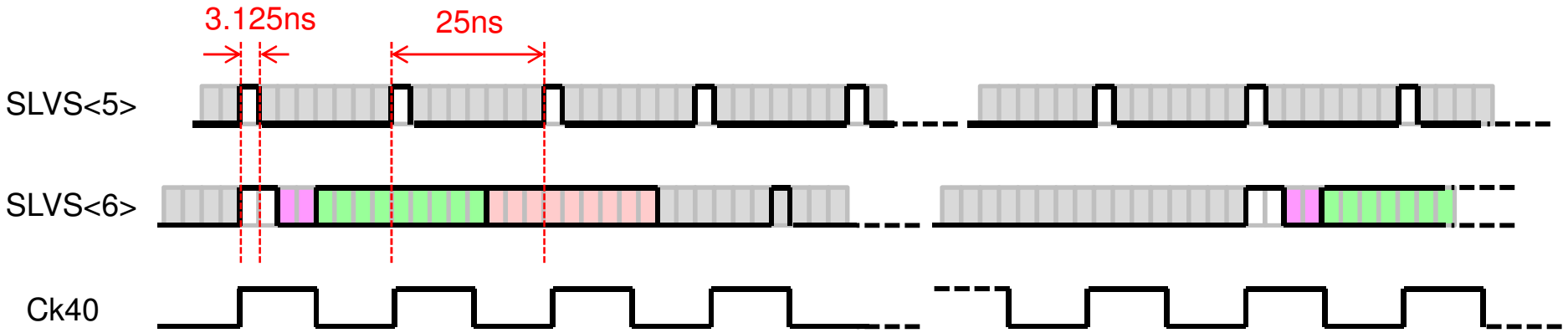
*"The direction of time flow is **bottom** to **top**, i.e. Stub1<7> is output first"*

http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Technical_Spec_V1p3.docx

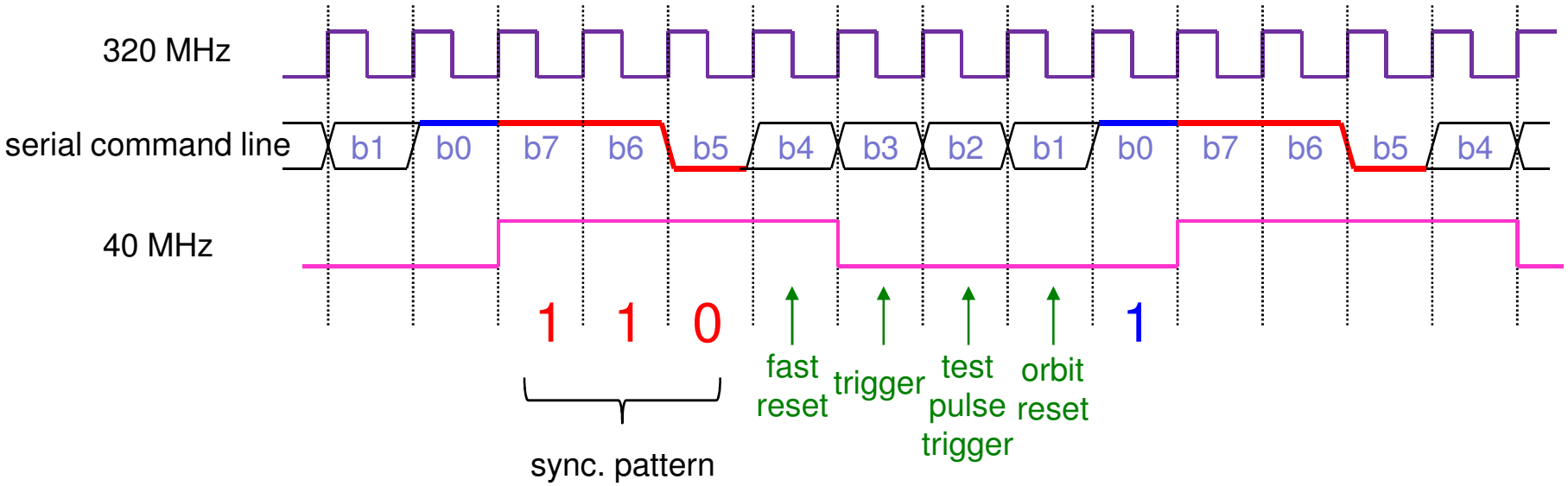
triggered output data



output data frame phase w.r.t. SLVS<5> (& Ck40)



fast control input (serial command interface)



FOR COMPLETENESS
NOTHING "NEW" HERE

40 MHz derived from sync pattern in serial command stream

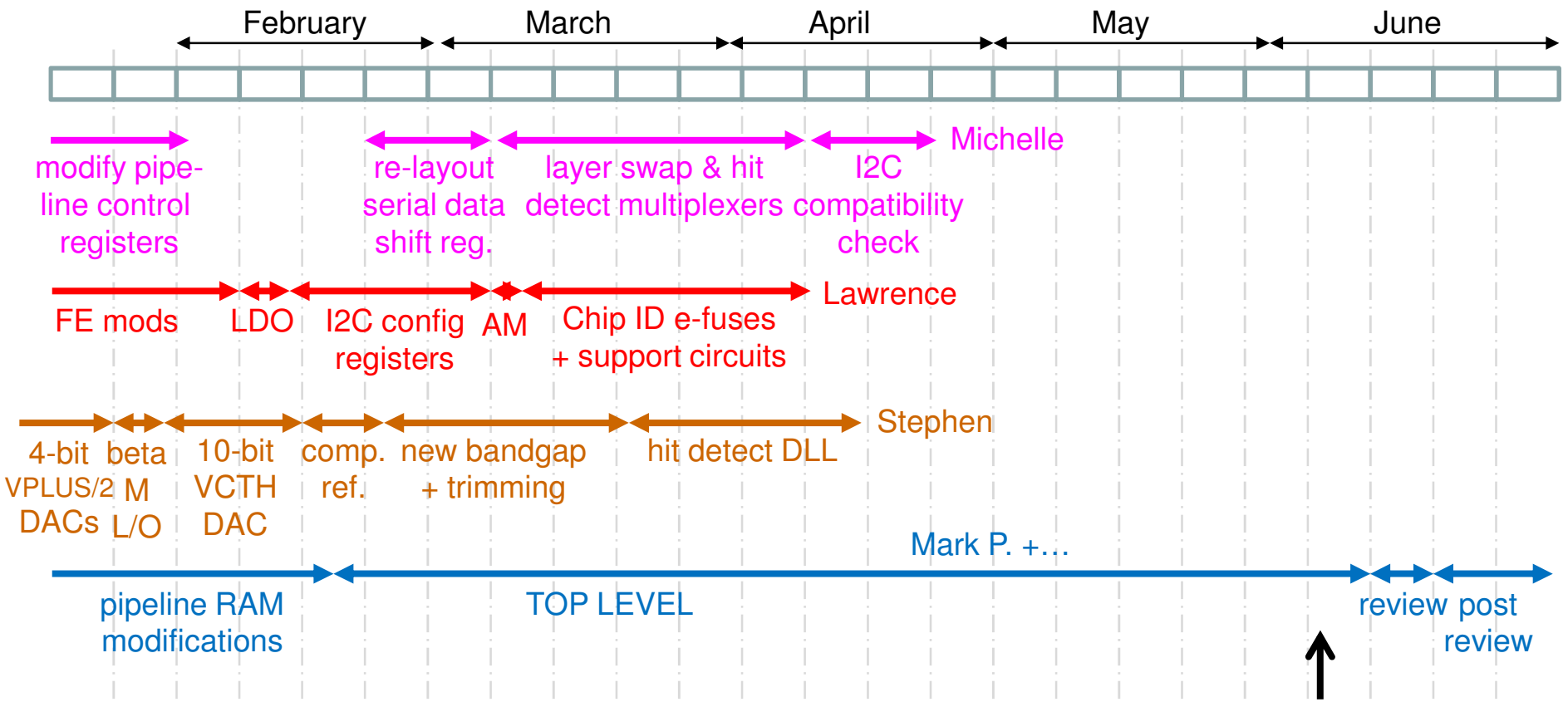
normal command structure cannot be confused with '110' sync. pattern

would never send fast reset at same time as trigger

would never send trigger at same time as test pulse trigger

final '1' ensures test pulse trigger coincident with orbit reset does not produce '110'

schedule



almost there

no last minute surprises expected

individual design blocks have been subject to ongoing review process during regular meetings

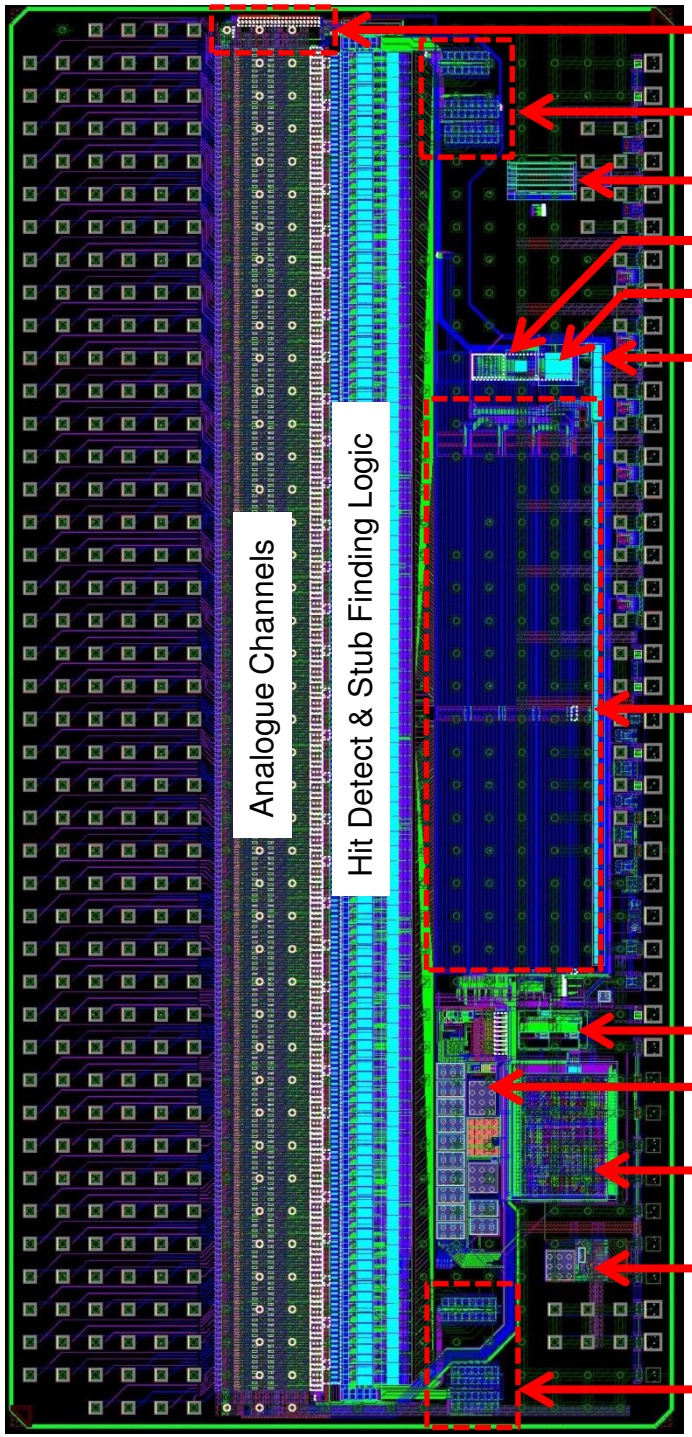
things left to do

- **Serial Command Interface:** Triplicate Layout, simulate & integrate in top level ← In progress
- **Solve** ss corner issue with the L1 Data Register ← In progress, poss. solution being evaluated
- **DLL:** Balance capacitive loads to lock in all corners, simulate & integrate in top level
- Finish routing signals (clocks)
- **Simulate** extracted netlist of SCI, DLL, reduced pipeline, L1 Data Register, L1 Counter, L1 FIFO, Bend LUT, Stub Data Assembly and SLVS pads all as one
- **Simulate** extracted netlist of the Bias & I2C block ← In progress
- **Add** extra I2C register to top of chip. ← In progress
- **DRC & LVS** Top Level without fill patterns or power routing
- **Add** power routing ← In progress
- **DRC & LVS** with power routing
- **Add** fill patterns
- **DRC & LVS** with fill patterns
- **Stream** out to GDS, stream back in & DRC & LVS again
- Review
- Revise
- Submit
- Fix any DRC issues CERN find.

Top Level

20 columns, 43 rows
(1 more column than CBC2)

all circuit blocks now present
in this picture



test pulse circuit

I/O to neighbour

DLL

bend LUT

data assembly

L1 counter & FIFO

512 deep pipeline & O/P buffer
(pipeline control logic now at top of chip)

bandgap

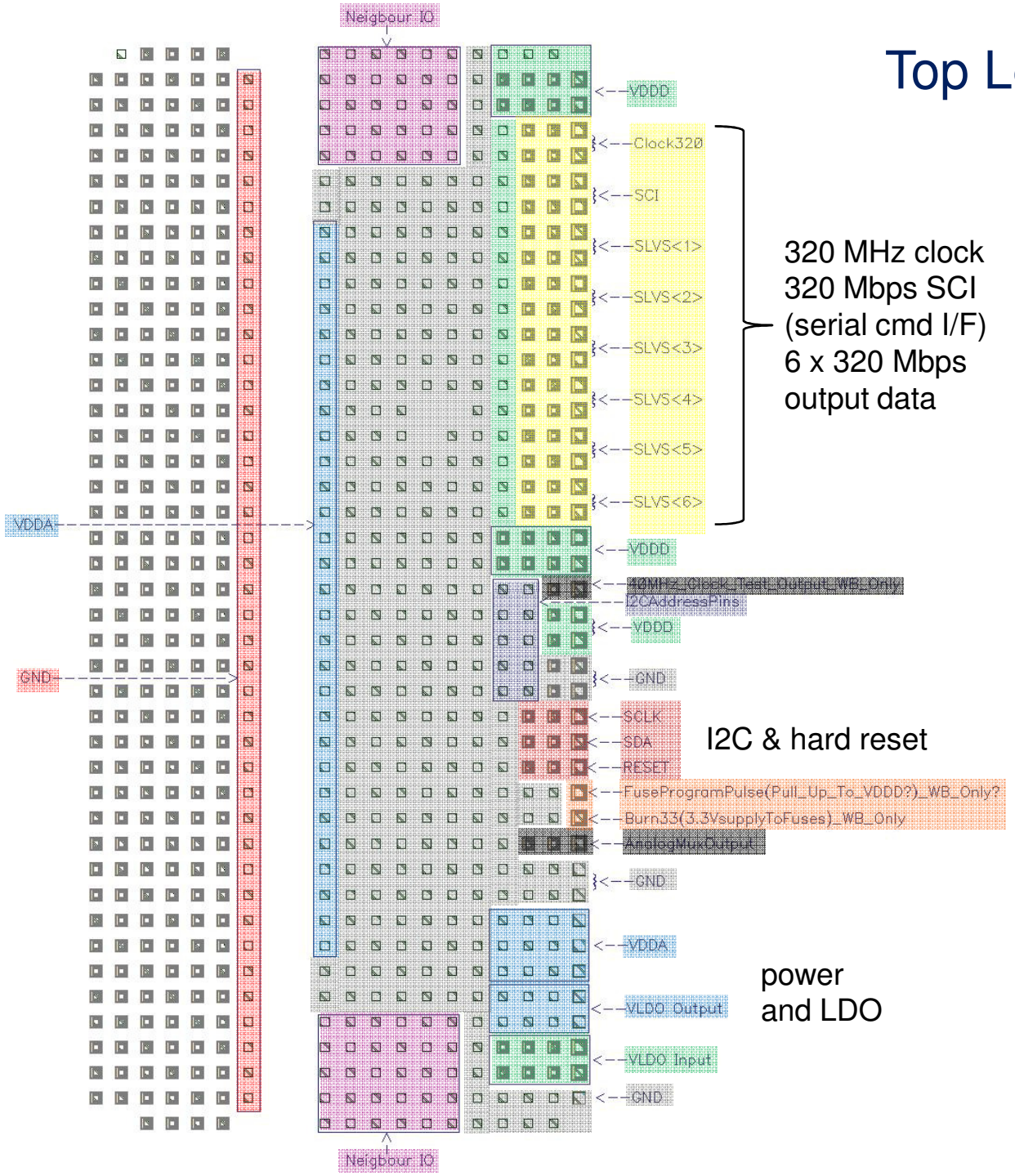
I2C & biases

10b DAC for VCTH

LDO

I/O to neighbour

Top Level - pad allocations



320 MHz clock
320 Mbps SCI
(serial cmd I/F)
6 x 320 Mbps
output data

I2C & hard reset

e-fuse
programming

power
and LDO

pads as viewed on chip surface
43 rows, 20 columns

(may not yet be completely final)
(but probably is)

extra power provision (GND
and VDDA) to front end

tracking to neighbour IO pads
now only 5 pads deep into chip

(6 cols of 5 rows instead of
5 cols of 6 rows)

hard reset

length not specified up to now

comes (I think) from LP-GBT parallel bus

any restrictions on length?

DLL needs worst case ~400 nsec

summary

final interface specs presented today

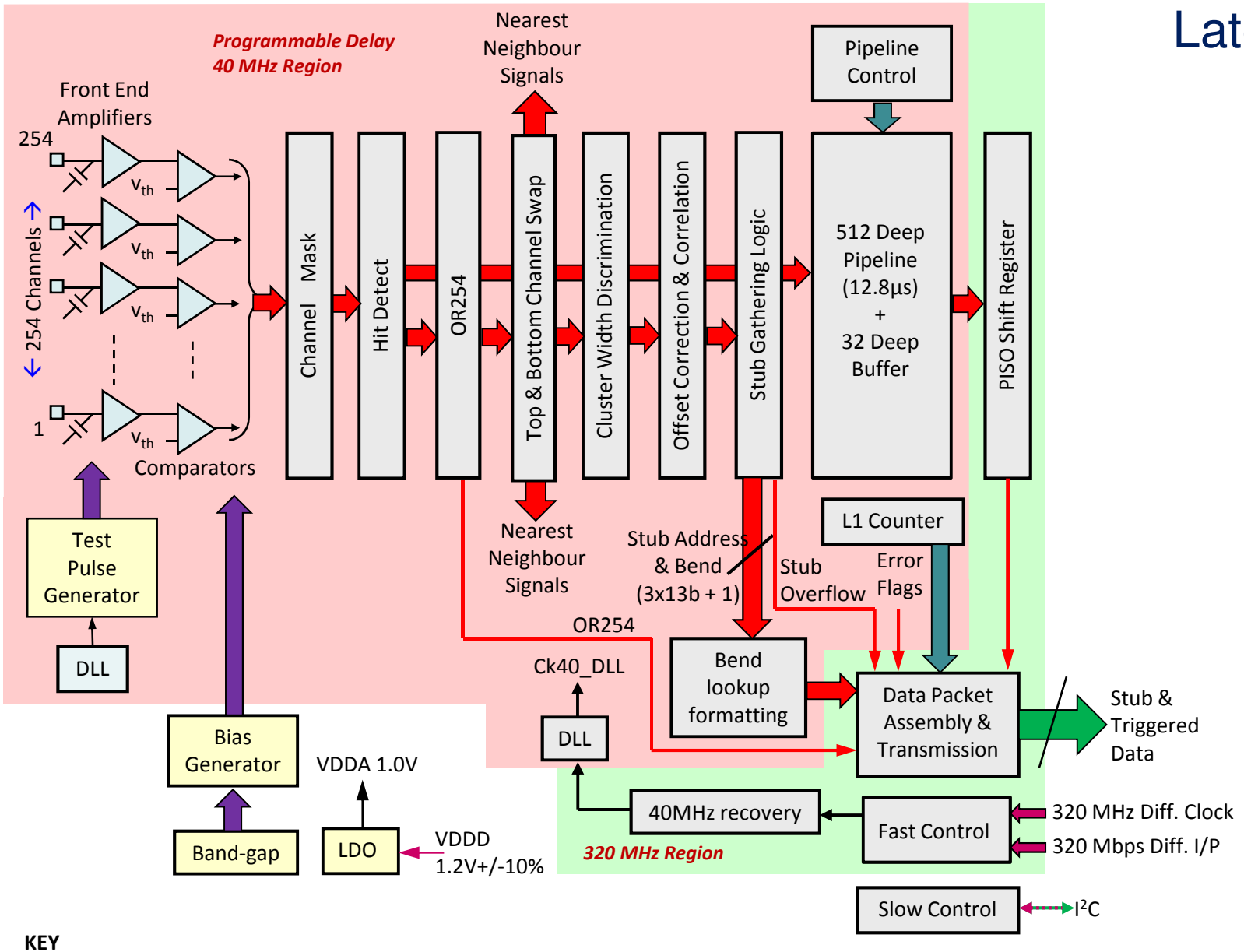
- some discrepancies fixed in design and spec document

http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Technical_Spec_V1p3.docx

still on track for completion at end of this month

extra

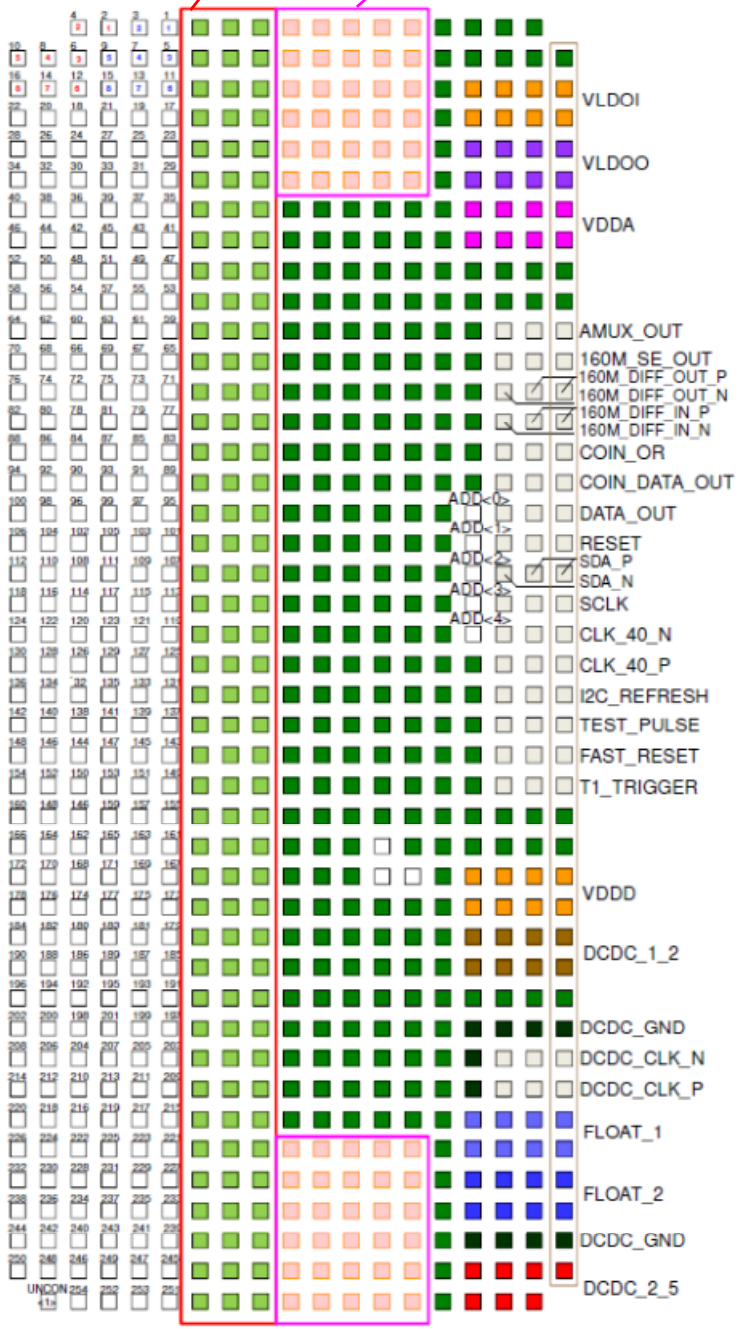
Latest Block Diagram



CBC2

dummy pads on chip (no connection to chip ground)

interchip digital



pads as viewed through chip (i.e. pad pattern on hybrid)

CBC2: 43 rows, 19 cols
CBC3: 43 rows, 20 cols

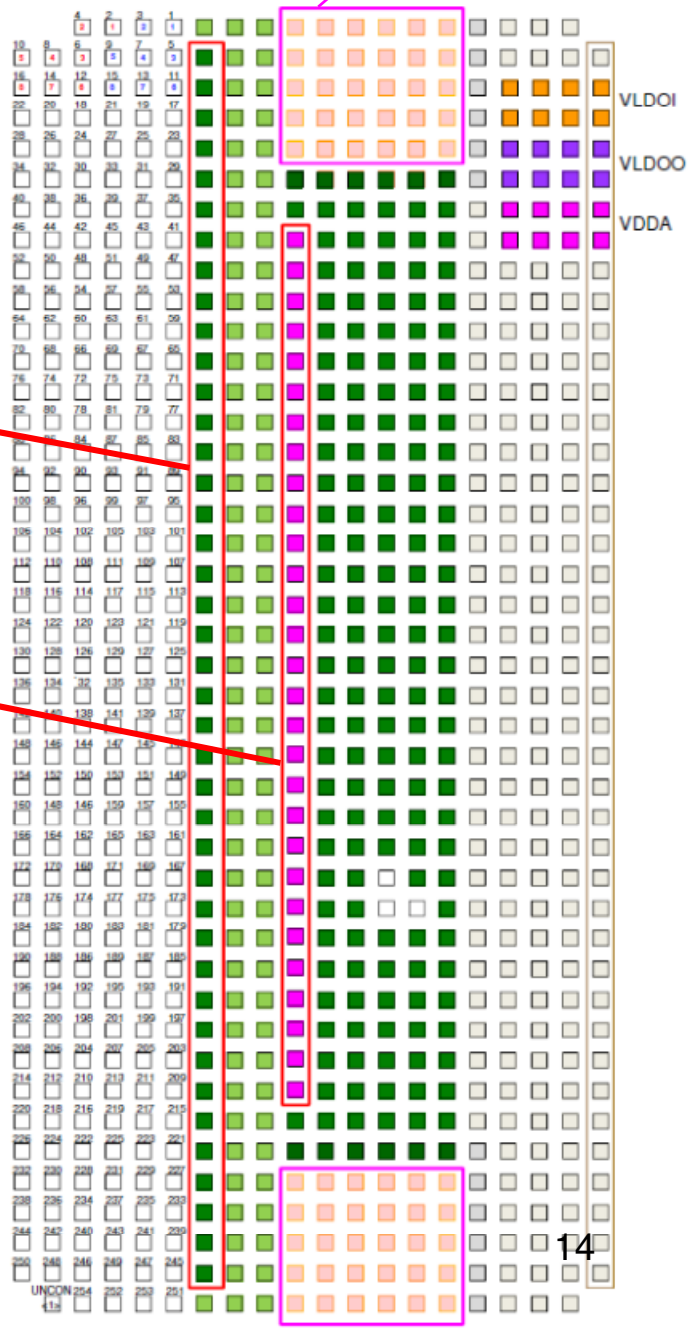
propose to replace these dummy pads (on CBC2) with GND pads on CBC3 connected internally to analogue front end

also propose to insert a column of pads to bring in VDDA close to analog front end

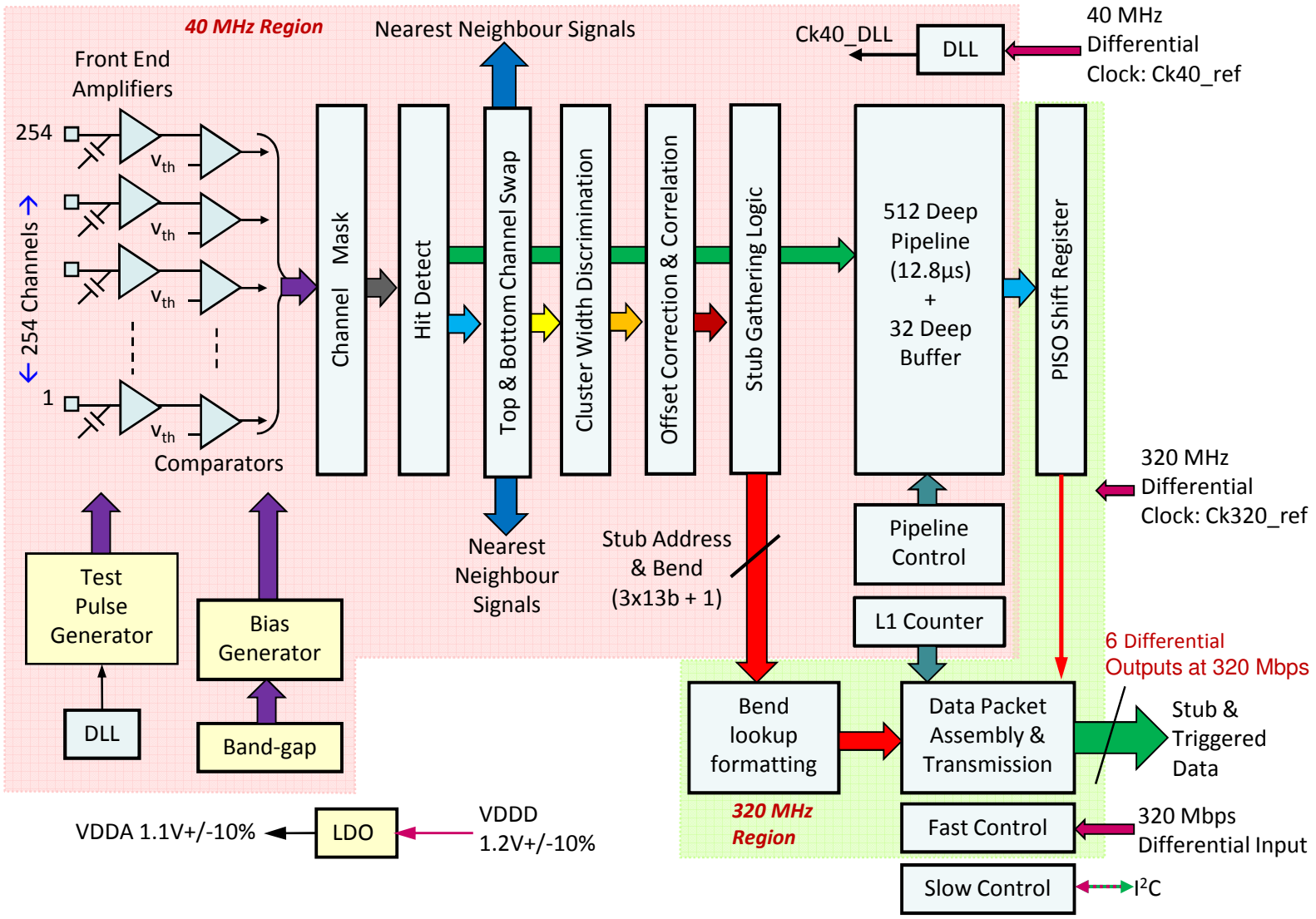
also note different orient-ation of interchip digital signals

CBC3

interchip digital

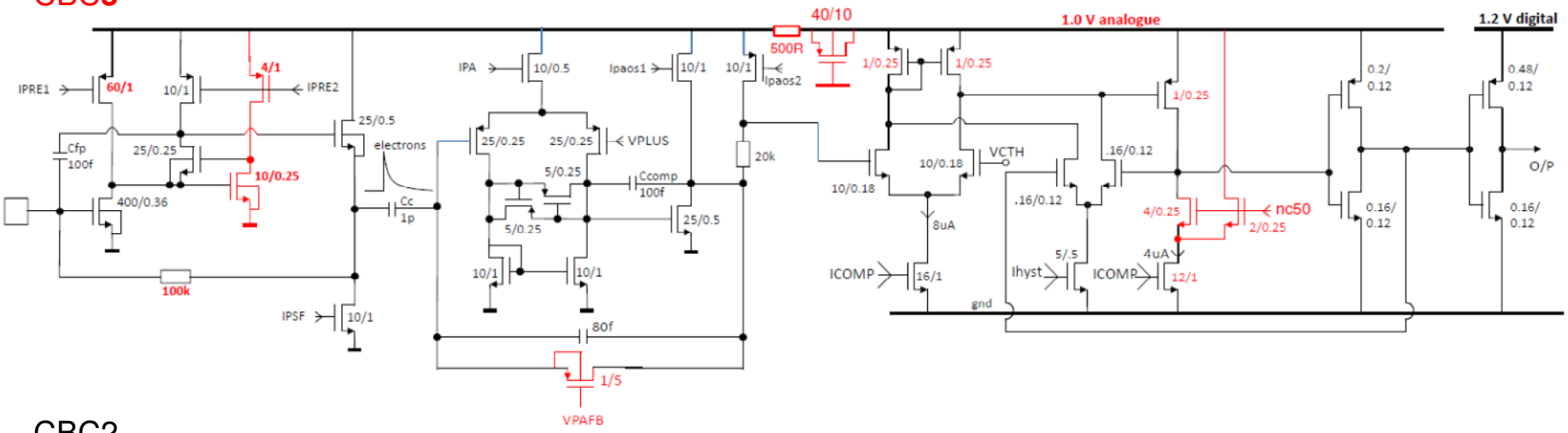


for reference (old block diagram)



front end design changes complete

CBC**3**



CBC2