CBC3 progress

matters arising from last time
- I2C spec
- 40 MHz clock source

design progress
- front end
- bias circuits
- top level

systems meeting, 2nd March, 2016.

Extracts from Kostas' I2C document

Data transfer protocol

- I2C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address, even if these START conditions are not positioned according to the proper format. **CBC currently doesn't comply**

Bus clear

- Where SCL is stuck LOW, reset the bus using the HW reset signal. **YES**
- If device does not have HW reset input, cycle power to the device (POR). **YES**
- If SDA is stuck LOW, the master should send nine clock pulses. The device holding the bus should release it within those nine clocks. If not, then use the HW reset or cycle power to clear the bus.

NO **YES**

Reserved addresses

- The I2C specification has reserved two sets of eight addresses, 1111XXX and 0000XXX. These addresses are used for special purposes.

no clash (CBC address b10xxxxx)

General call address

- The general call address comprises an address equal to 0000 000 followed by R/W = 0 and is reserved to implement special operations. The general call addresses every device connected to the I2C-bus at the same time.

Software reset

- Following a General Call, (0000 0000), sending 0000 0110 (06h) as the second byte causes a software reset. This feature is optional.
- On receiving this 2-byte sequence, all devices designed to respond to the
- general call address reset and take in the programmable part of their address.

CBC does not implement this

Device ID

3 bytes for CBC (19 bits - 10 for wafer ID, 9 for chip ID on wafer)

- Each device must have hardcoded on silicon a unique 2-byte device identifier, implemented with pre-programed laser fuses or electrically programmable fuses.
- The Device ID is read only and should be mapped in two consecutive addressed device internal registers.

scrapping the 40 MHz reference clock

proposal to derive from 320 MHz using sync bit in fast control data stream

doable - details of 40 MHz phase definition need to be specified

some kind of start-up protocol?

e.g. operating period with sync pulse only?

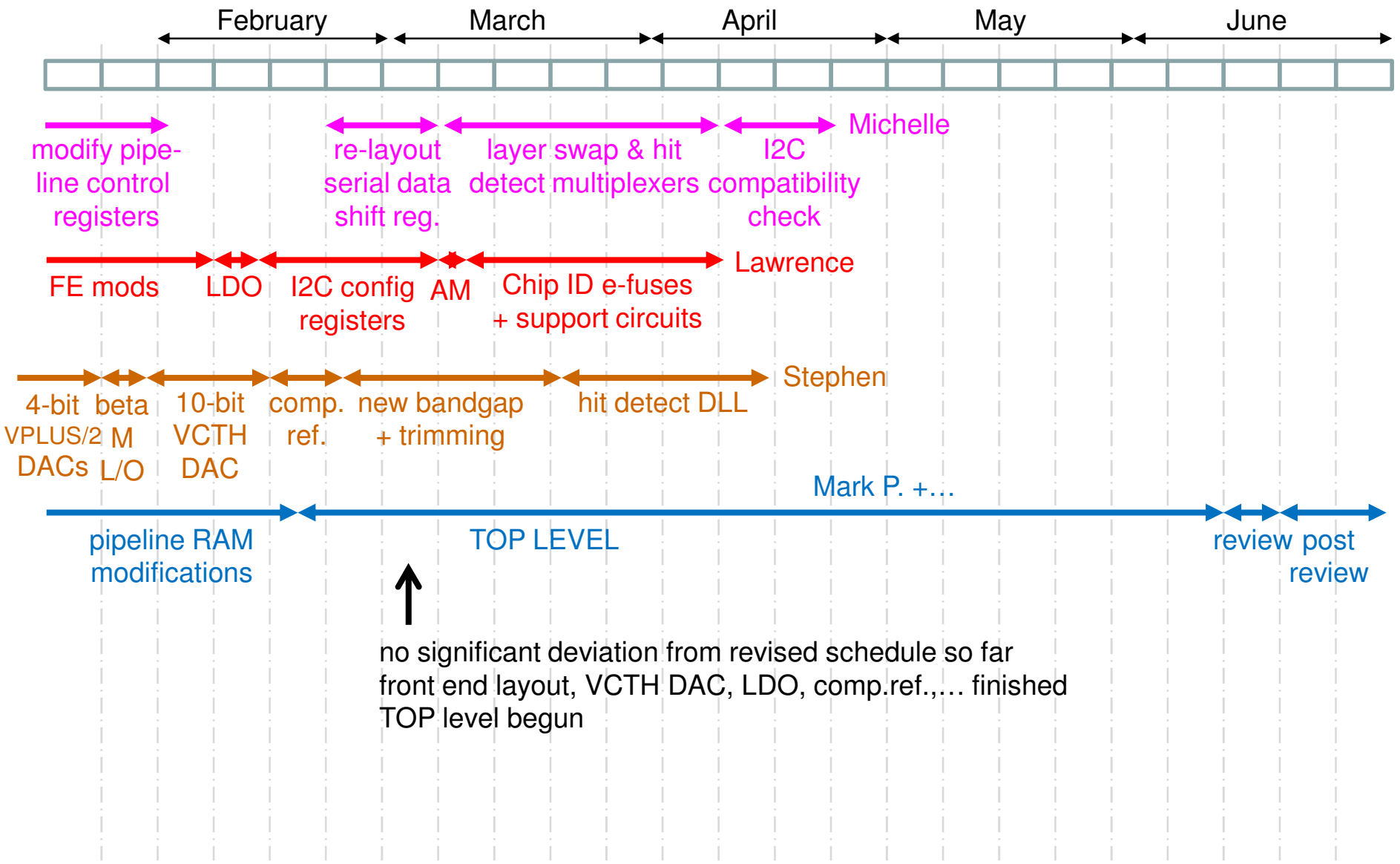
may have some design issues for low frequency (40 MHz) testing for CBC3

if adopted for CBC then will inevitably add something to schedule

specification, design, simulation, implementation, re-simulation,…

hard to be specific, but might stretch to a few weeks

schedule


February
March
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modify pipe-line control registers
re-layout serial data shift reg.
layer swap & hit detect multiplexers
I2C compatibility check
Michelle
FE mods
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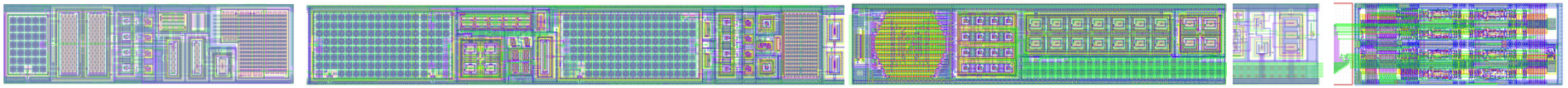
Chip ID e-fuses + support circuits
Lawrence
4-bit VPLUS/2 DACs
beta M L/O
10-bit VCTH DAC
comp. ref.
new bandgap + trimming
hit detect DLL
Stephen
Mark P. +…
pipeline RAM modifications
TOP LEVEL
review post review
no significant deviation from revised schedule so far
front end layout, VCTH DAC, LDO, comp.ref.,… finished
TOP level begun

front end layout modifications complete

CBC2



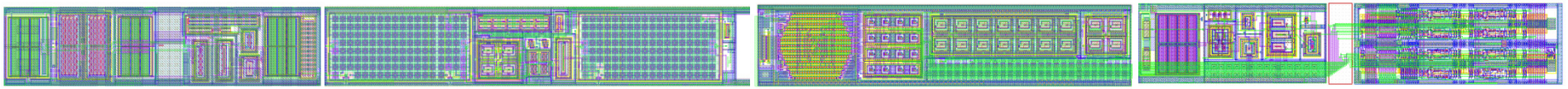
preamp
~same

postamp
shrunk

offset adjust

comparator
larger

CBC3



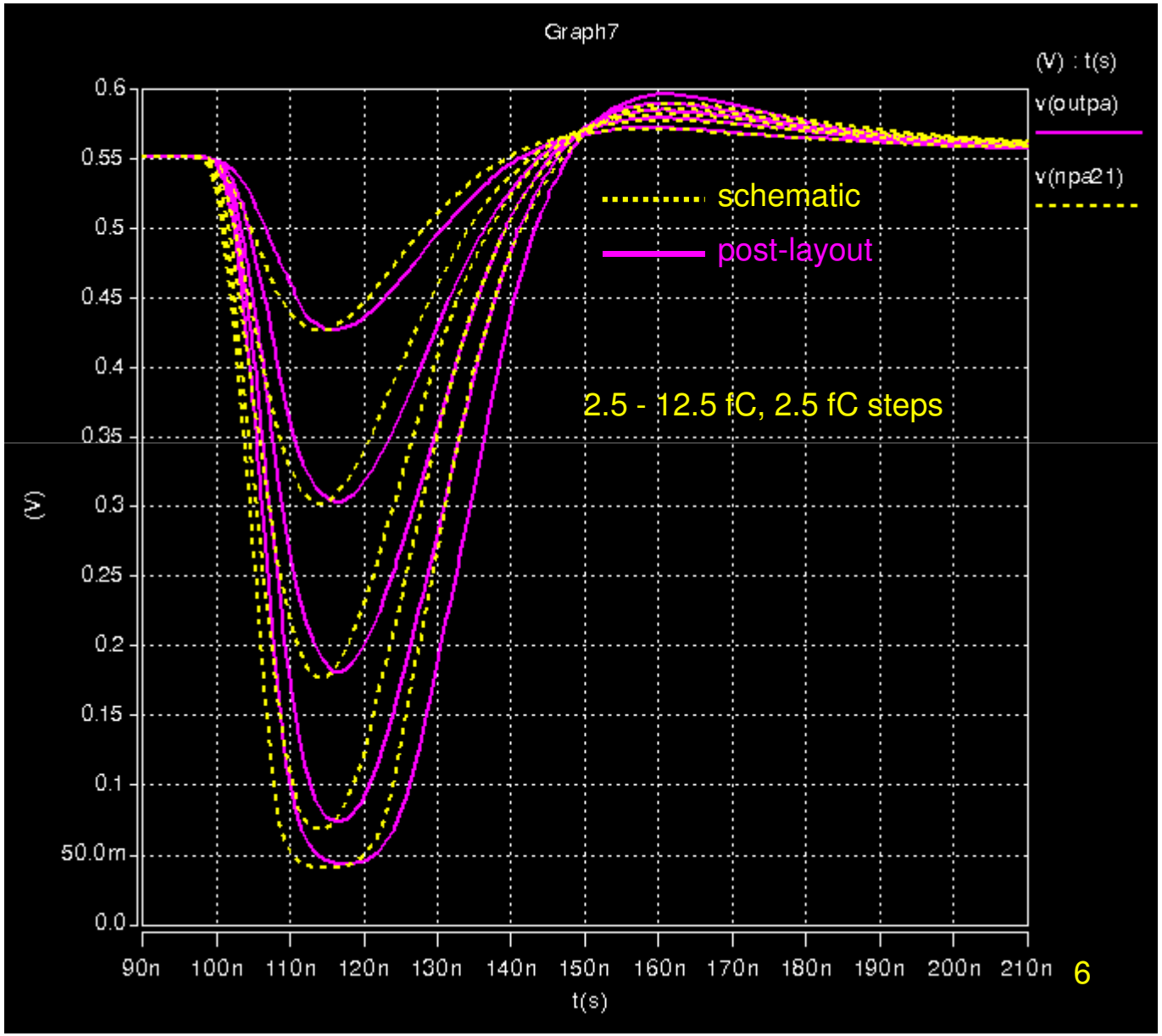
overall channel length the same

extracted front end simulations: postamp O/P

extracted postamp response slower but gain and overall pulse width ~same

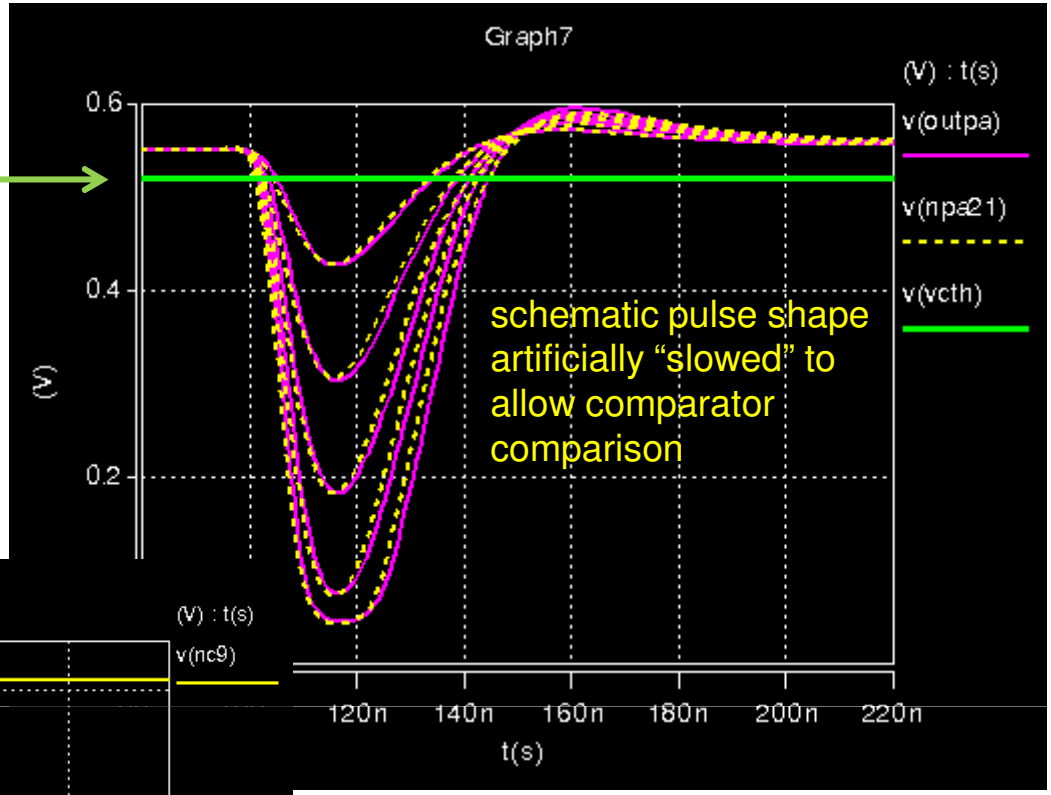
typical params, T=0

=> no concerns

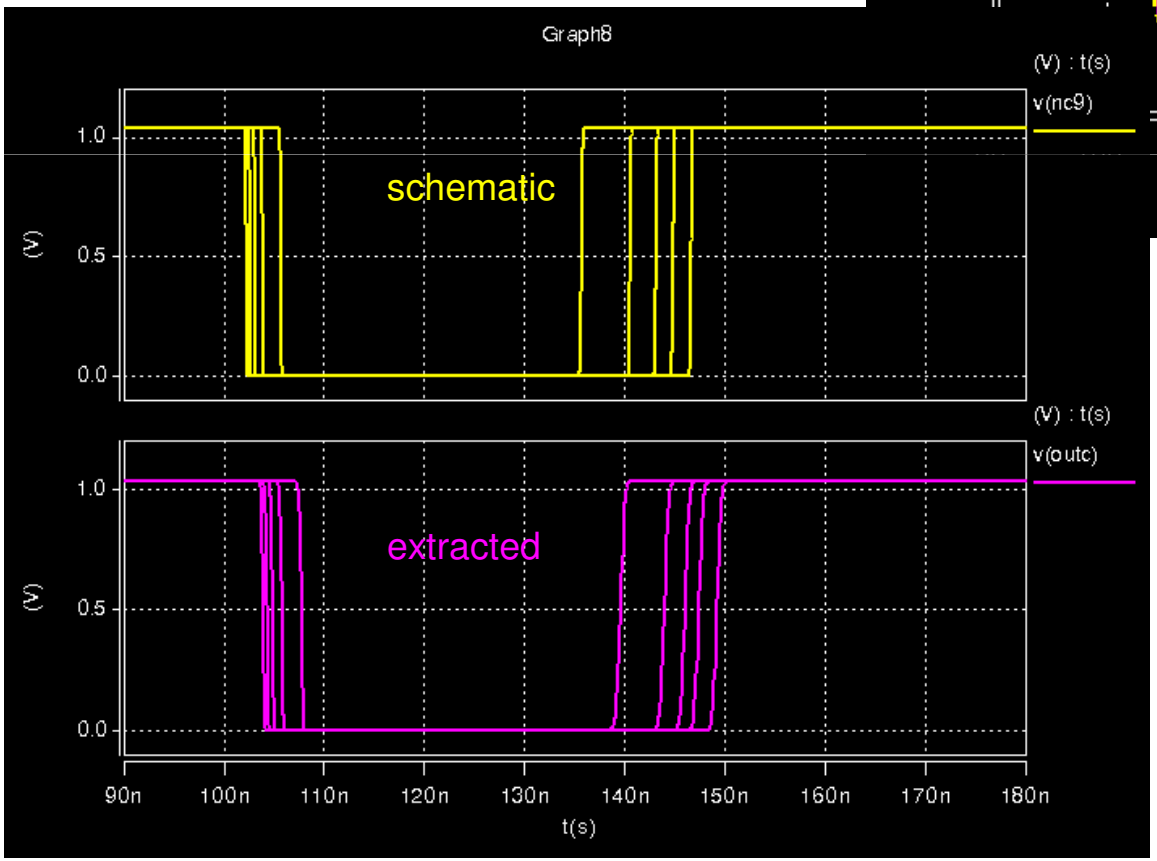


comparator output

for this threshold



get this response



note: minimum hysteresis selected

comparator output pulse width <50ns

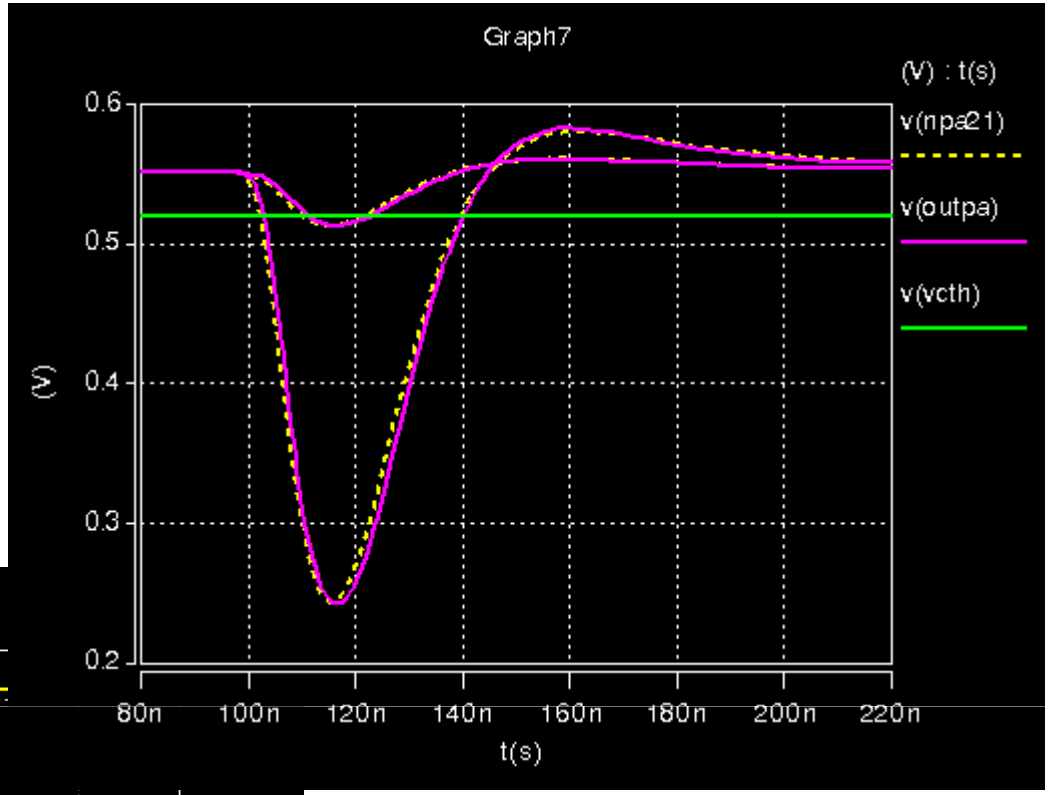
comparator timewalk

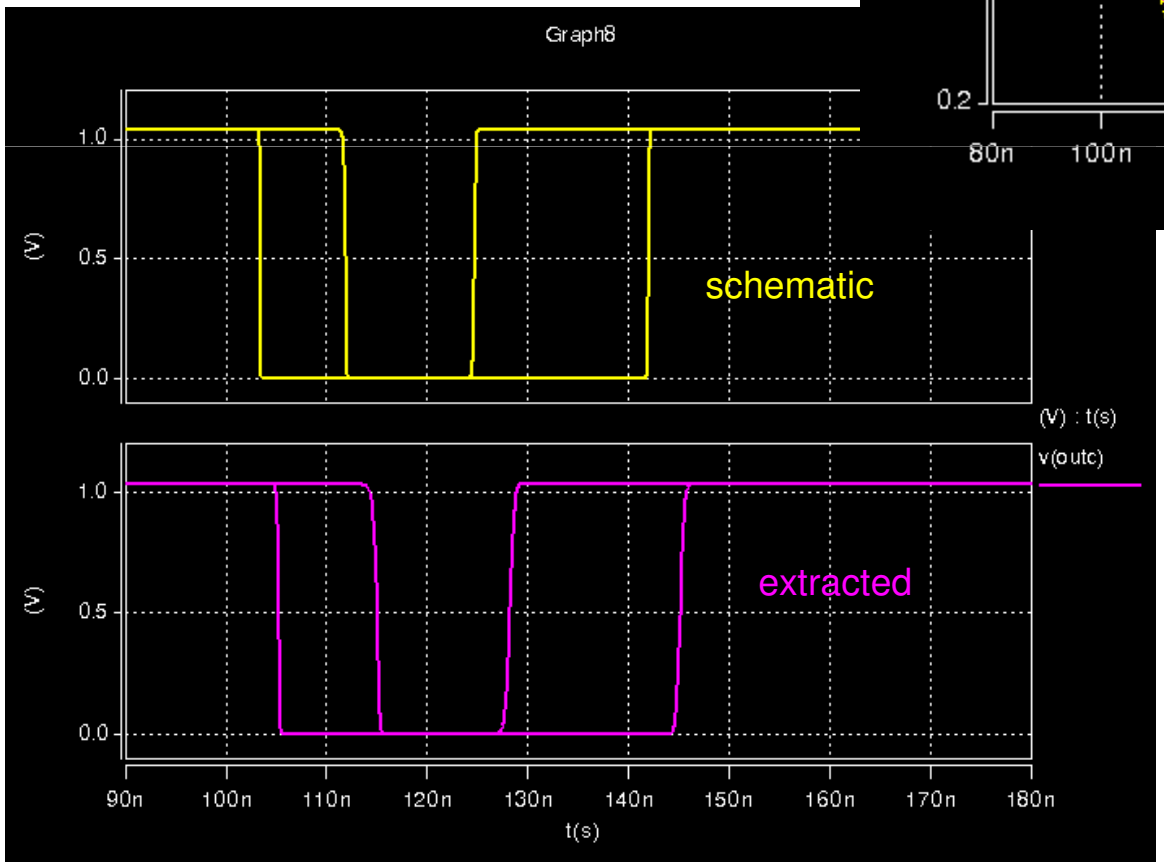
have modified existing spec.

<16ns for 1.25 -> 10 fC (thresh. @ 1fC)

to allow for thinner sensors (200um cf. 300um)

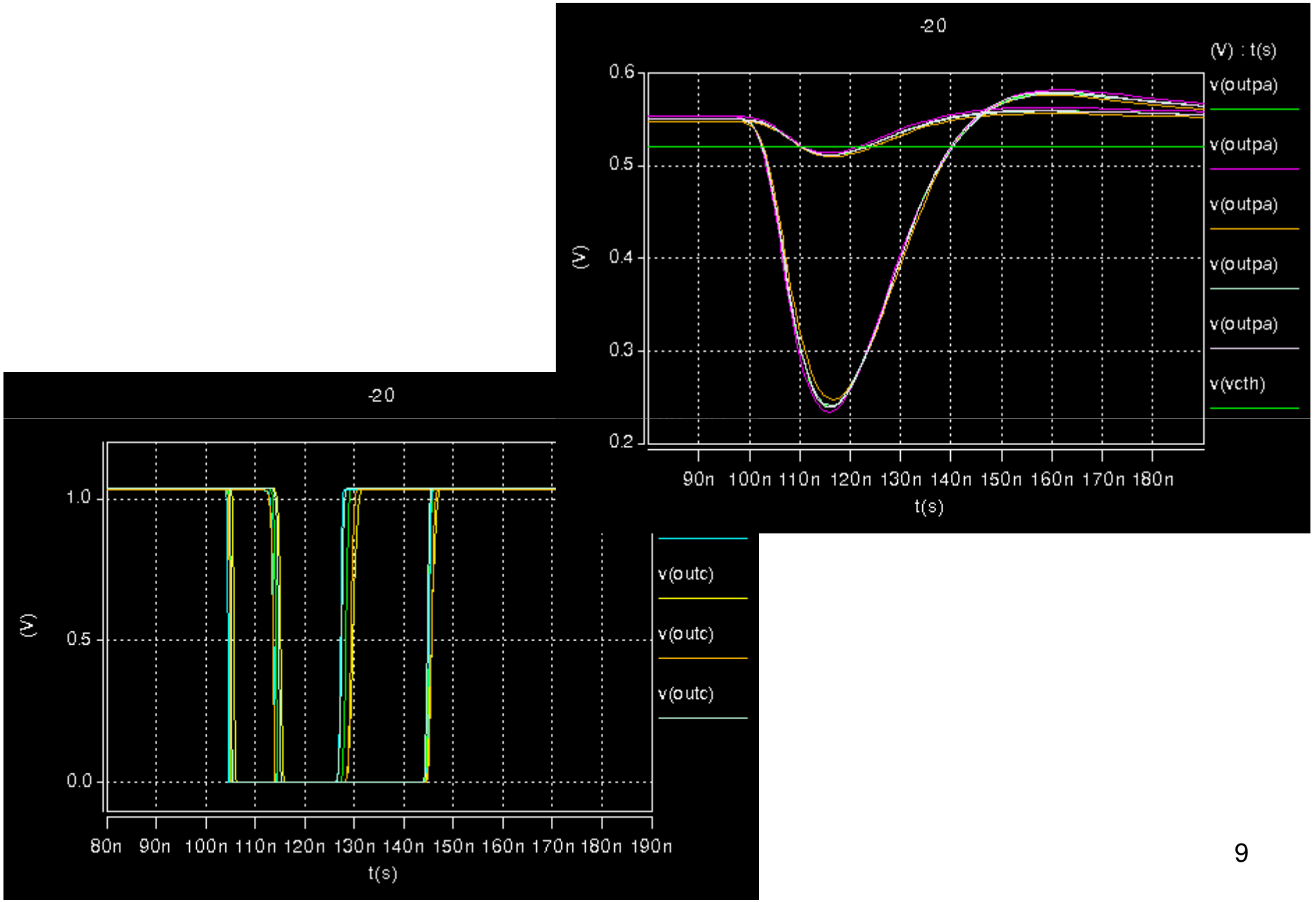
gives <16ns for 0.78 -> 6.25fC (thresh. @ 0.625)



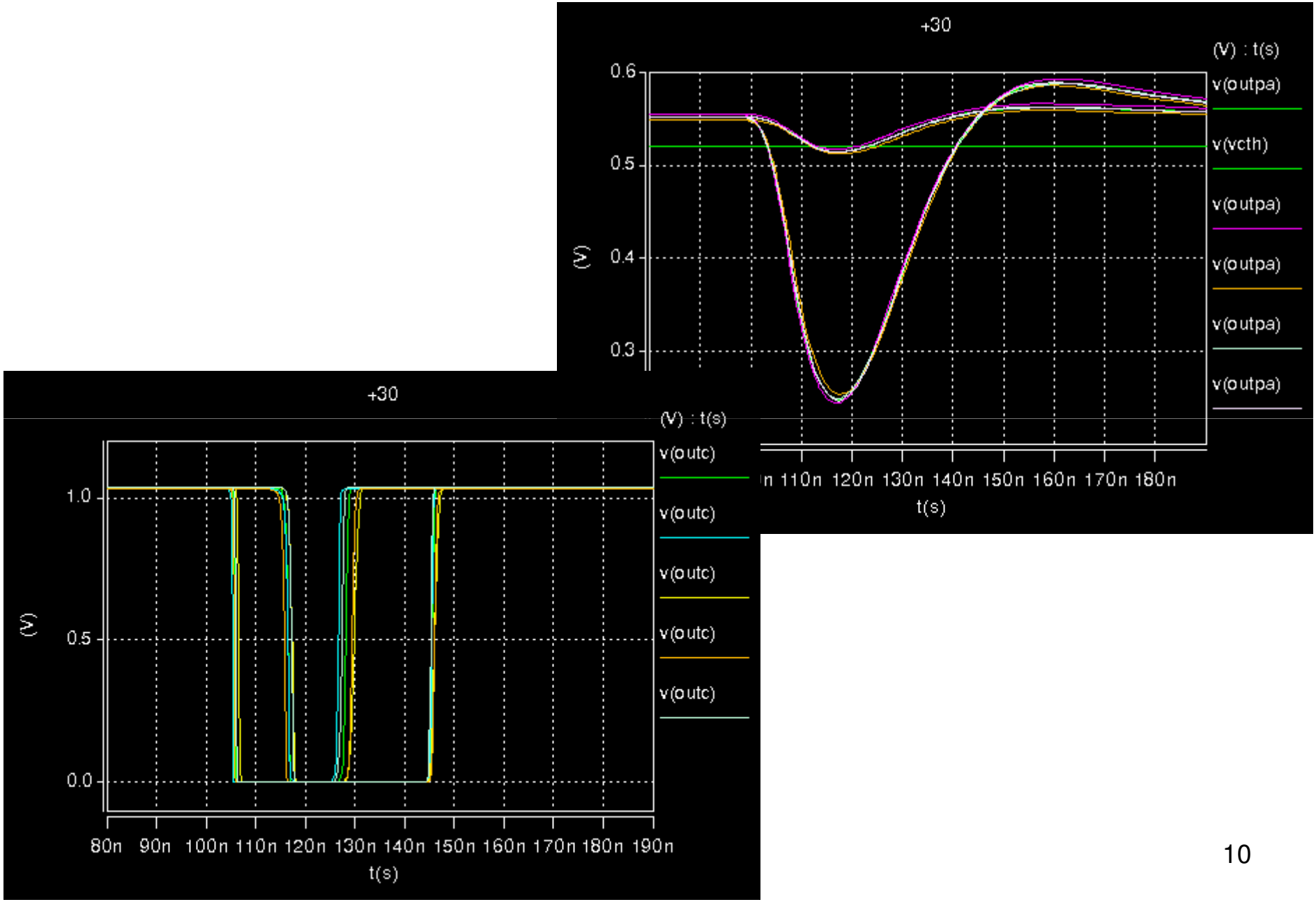


timewalk ~ 10 nsec

comparator timewalk vs process (-20)

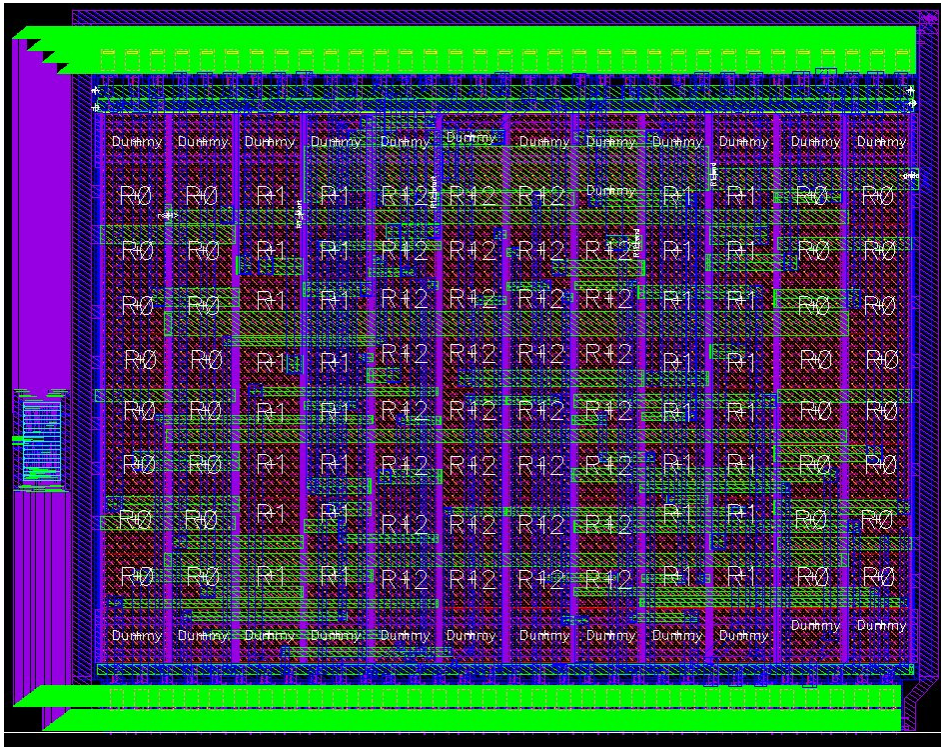


comparator timewalk vs process (+30)



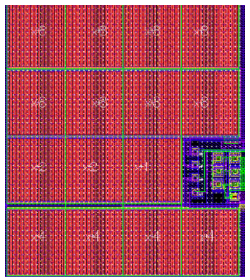
other design blocks

10-bit VCTH DAC

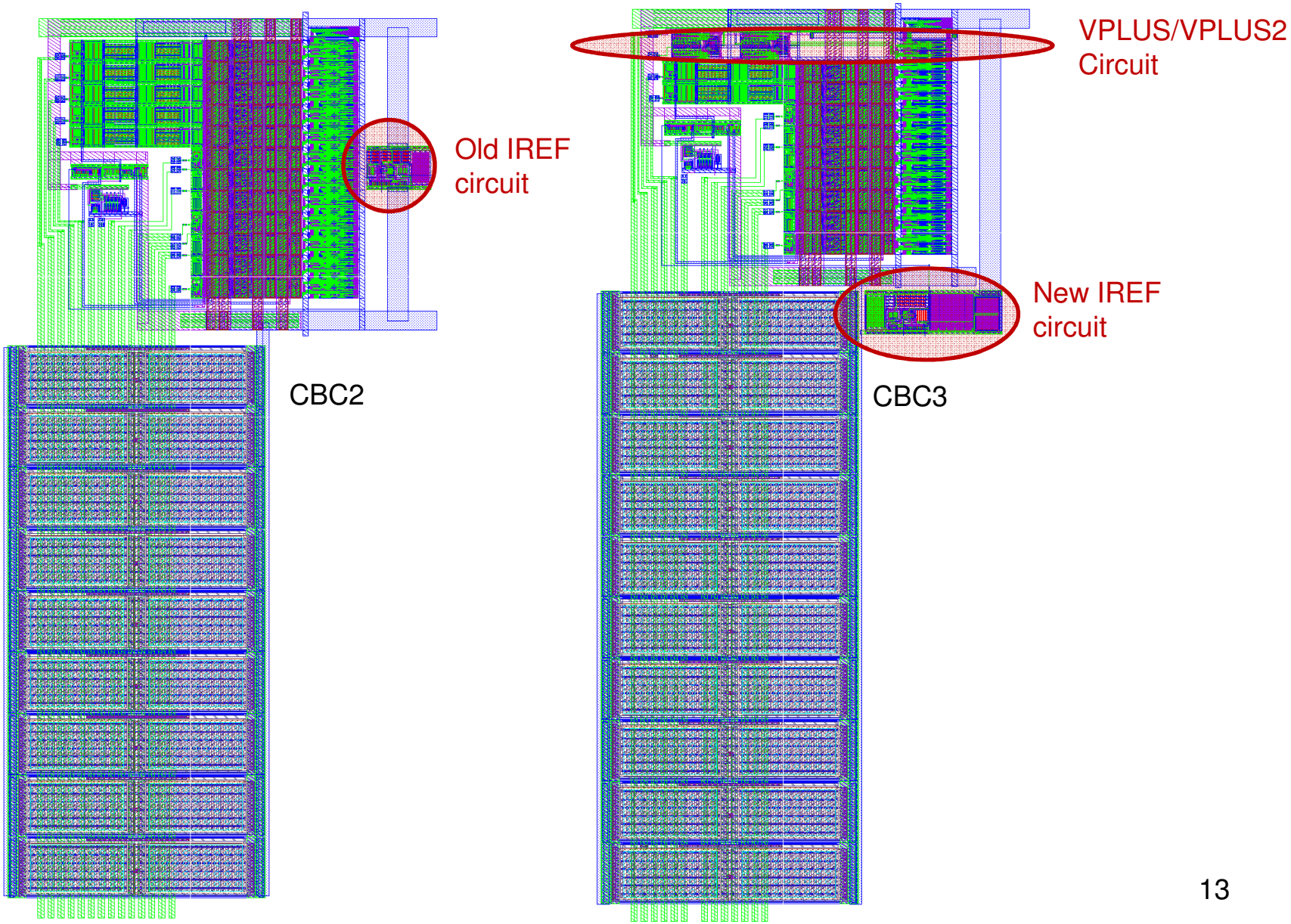


1025 um x 800 um
dominated by resistors
high W*L for matching
post layout INL/DNL < 0.5 LSB for all corners

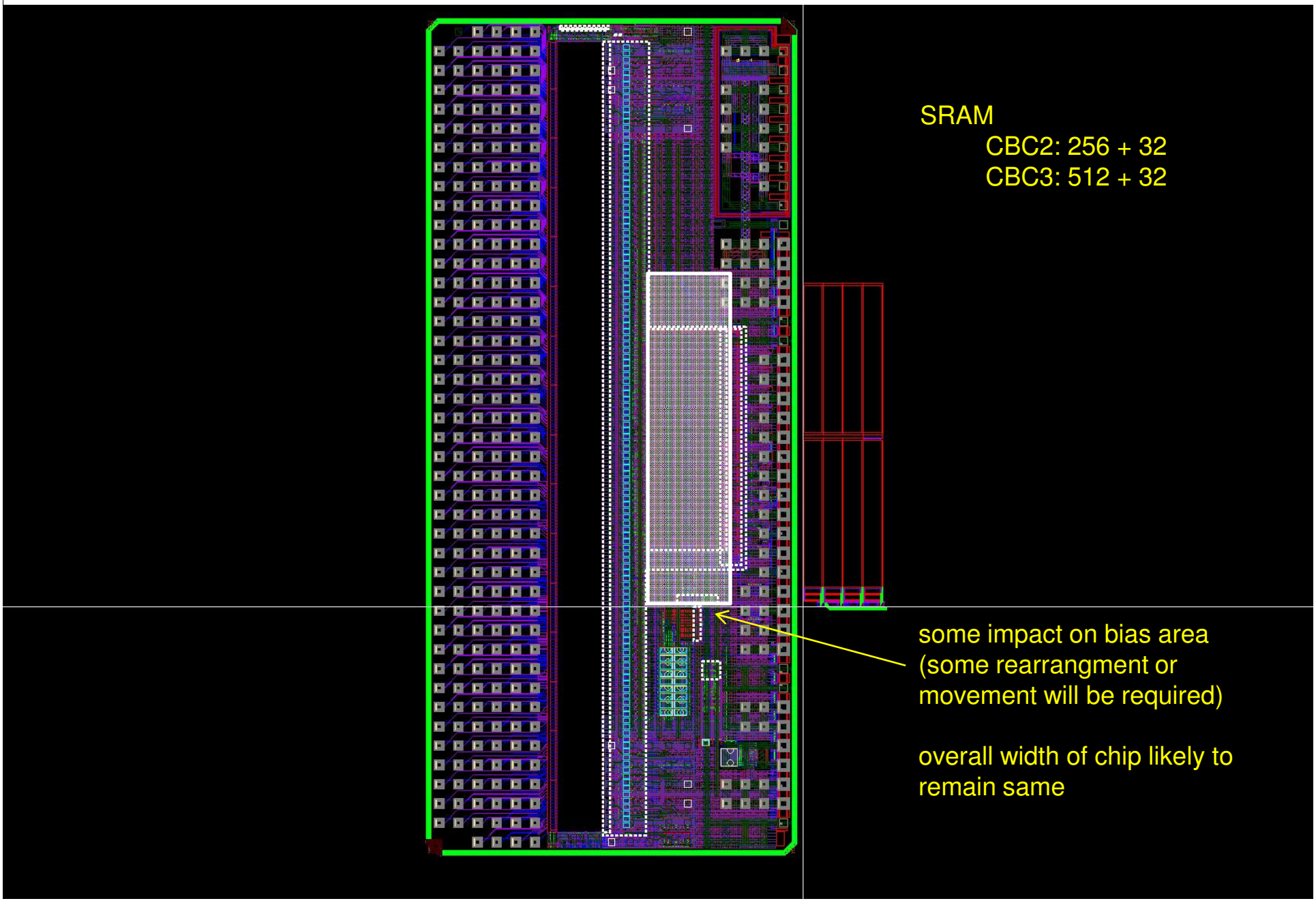
beta multiplier postamp fedback circuit complete
255 um x 296 um



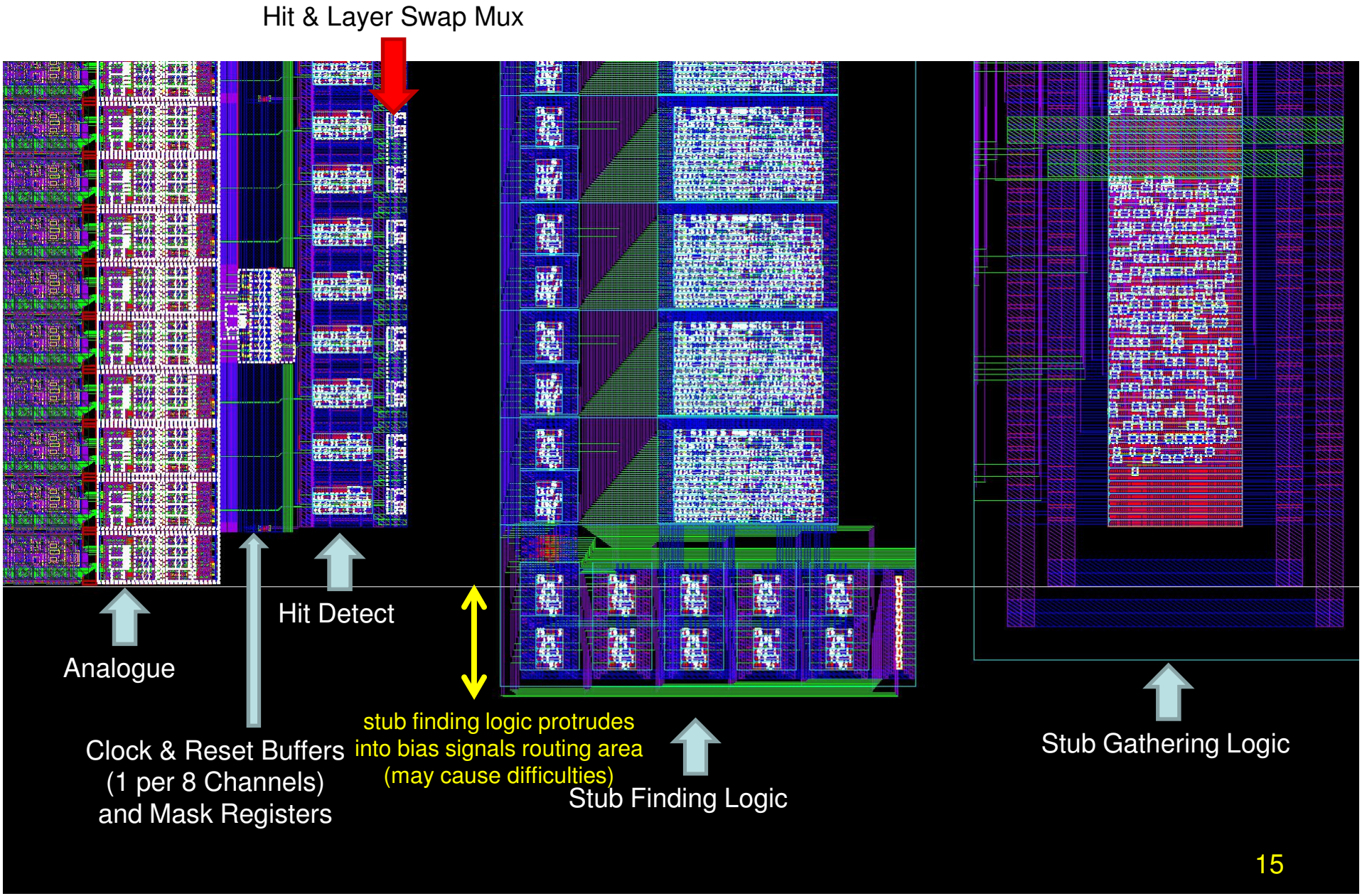
CBC2/CBC3 Bias Block Layouts



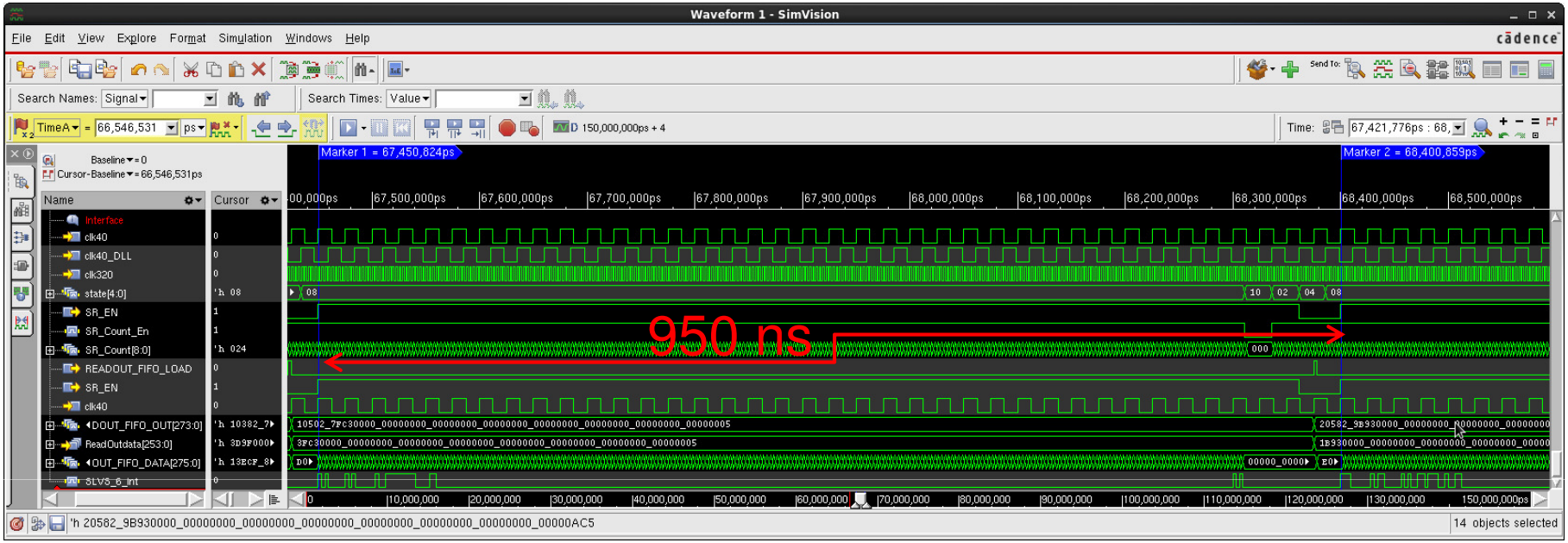
New SRAM overlay of CBC2

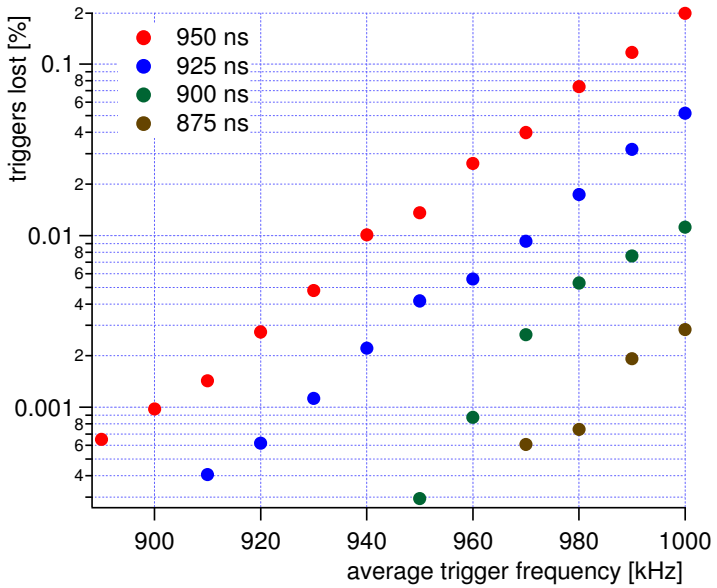


Top level progress



output frame length





output frame will begin on a 40 MHz clock boundary

difficult to avoid extra 40 MHz clock cycles at end of frame

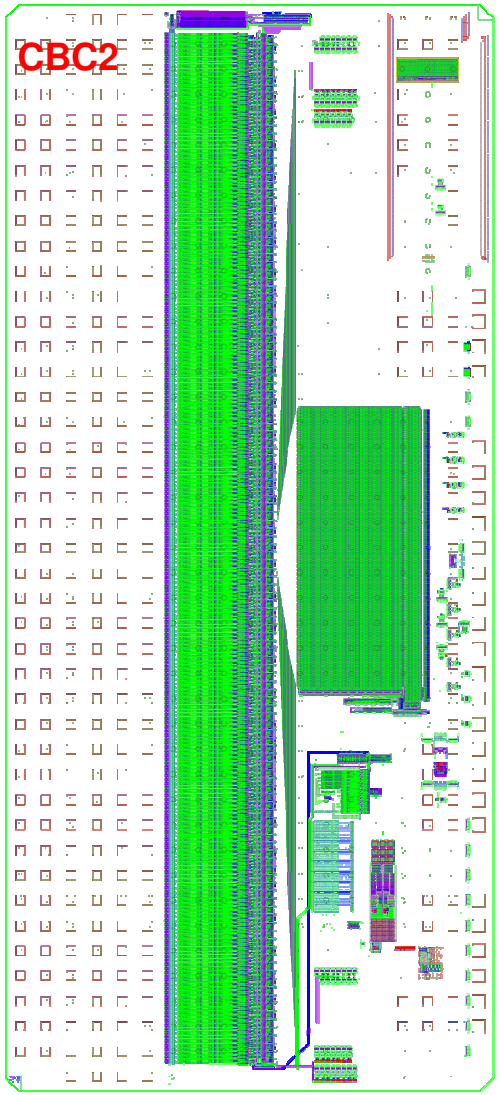
=> overall frame length 950 nsec

=> ~ 0.2% triggers lost at average 1 MHz trigger rate

(negligible inefficiency at 750 kHz)

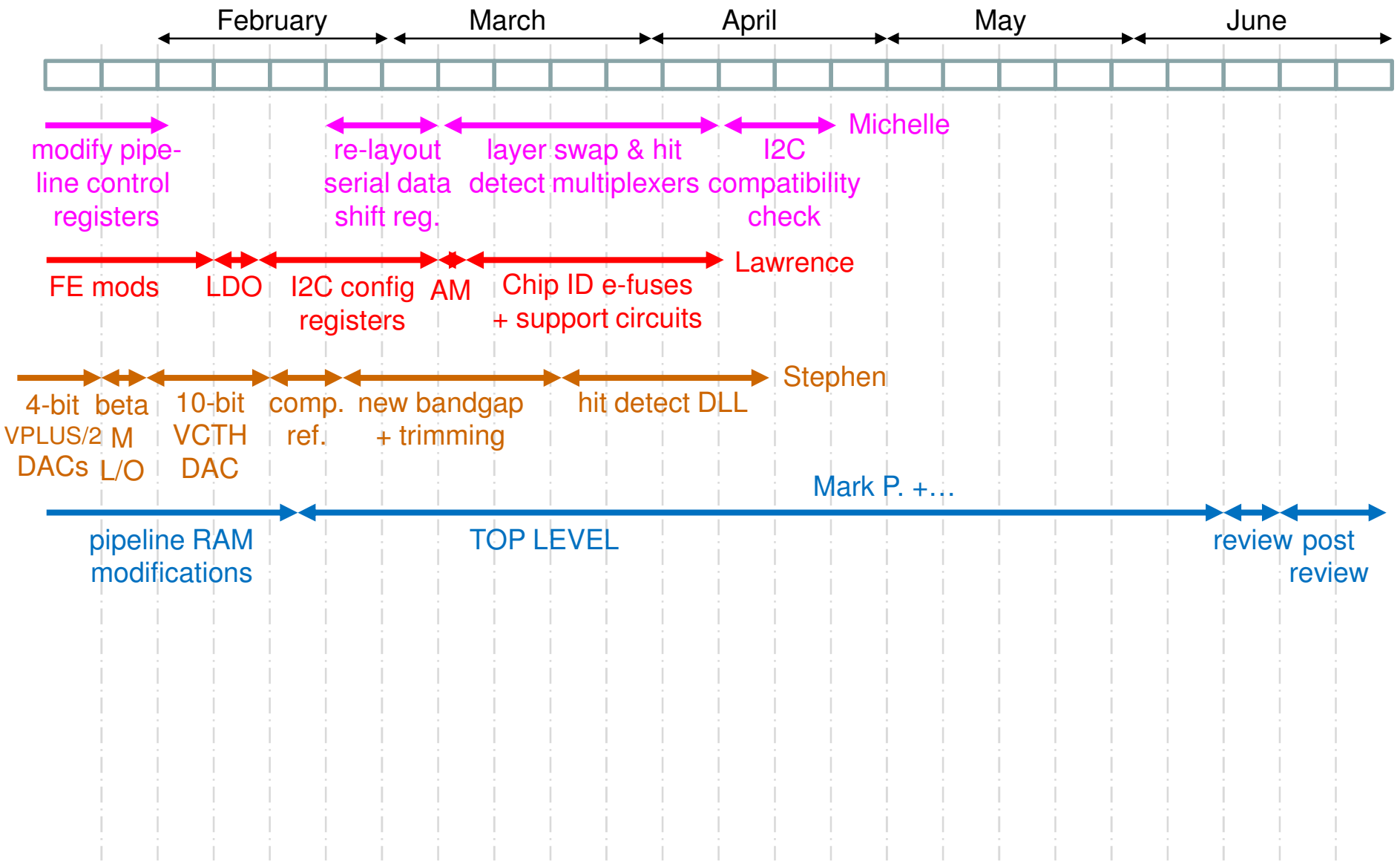
summary / final remarks/questions

- from last time
  - wafer sharing details
    - any progress on likely area ratio of CBC:SCA asics?
  - bump-bond pad design requirements (baseline CBC2 design)
- I2C specification
  - some divergence from Kostas' spec.
- 40 MHz clock presence
  - decision?
- CBC3 vertical dimensions
  - would help if hybrid design could allow some growth - few 100 um's?



extra

schedule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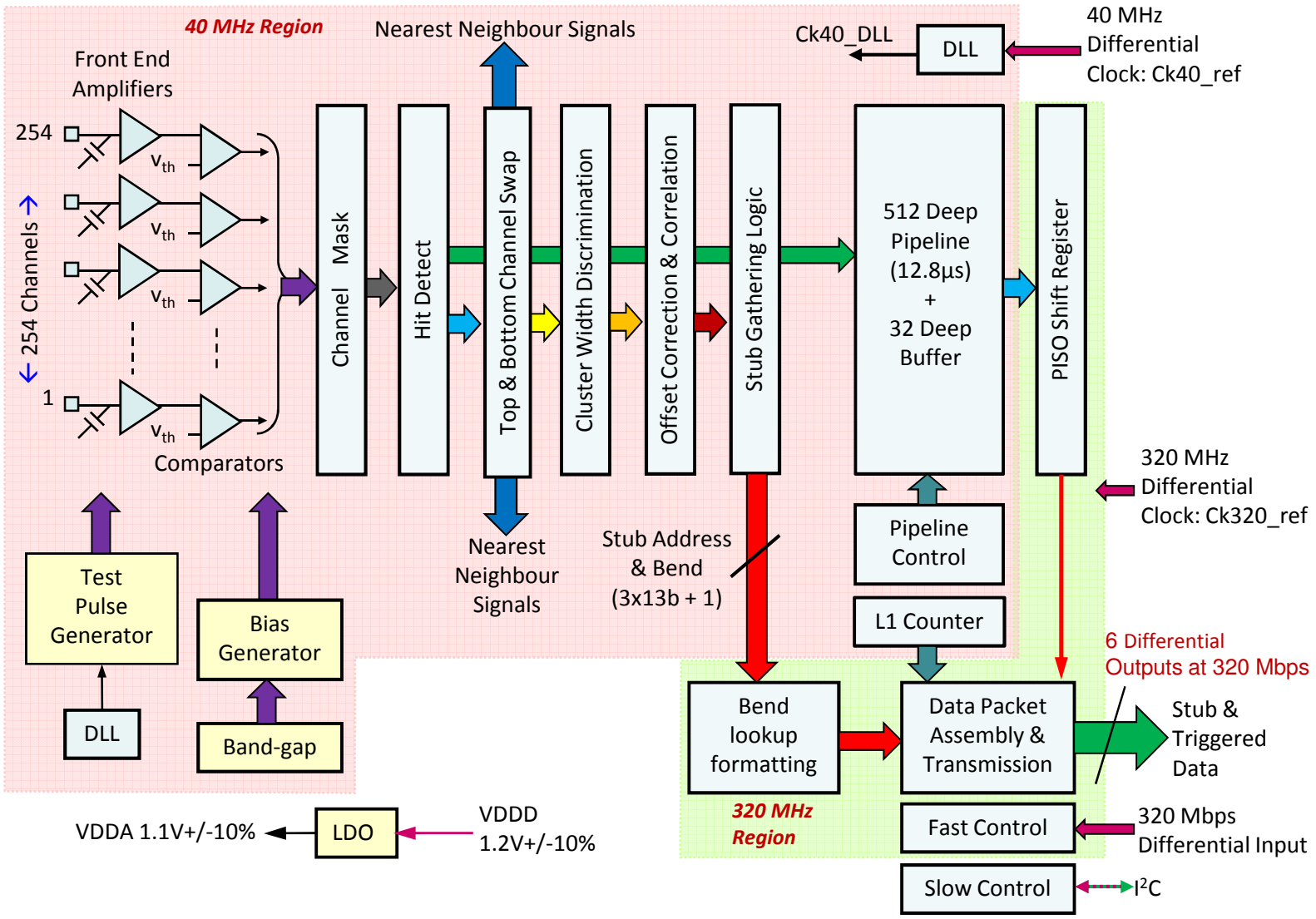


CBC3 digital interfaces

reminder of main changes/new features

stub gathering logic, address and bend transmission
- 8 bit stub seed address (1/2 strip resolution)
- 4 bit bend info (location of cluster in window layer)

up to 3 stubs data transmitted to CIC /BX
- 6 diff pairs @ 320 Mbps

pipeline cell modifications and length increase (12.8usec)

single 320 Mbps fast control line

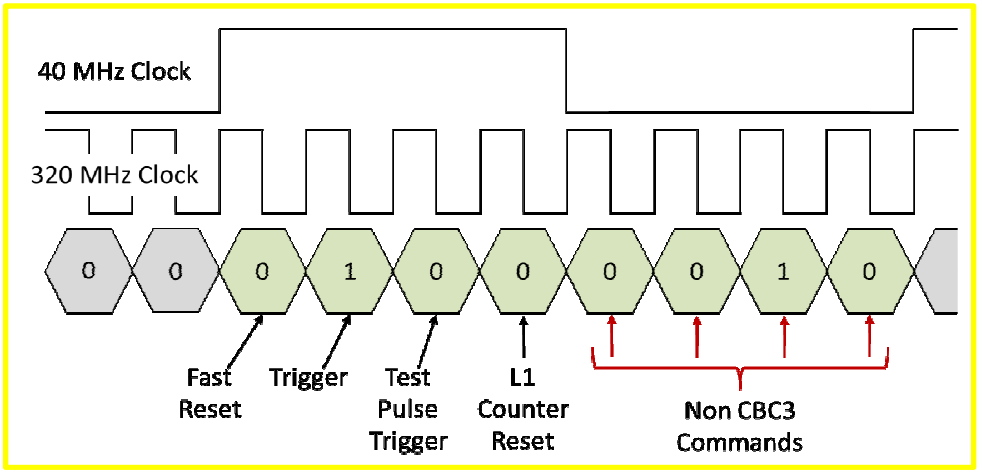
up to 1 MHz L1 triggering capability
- readout data frame < 1 usec

output data

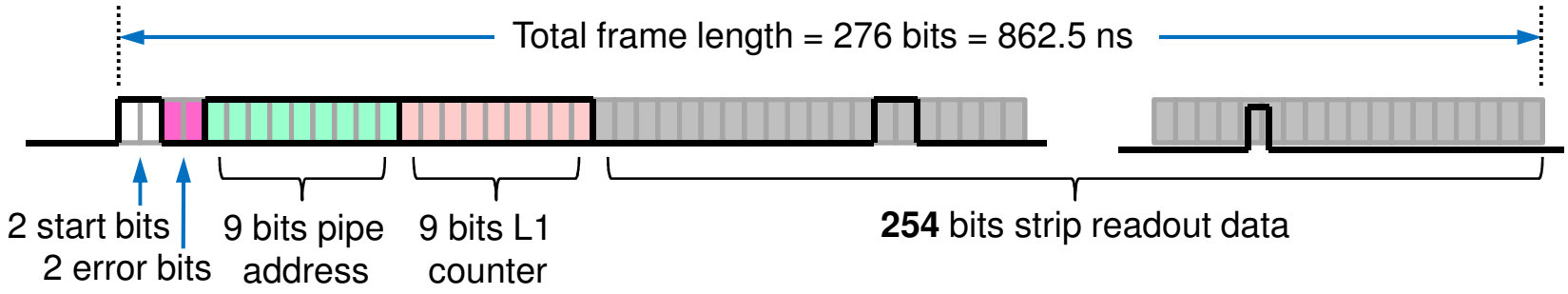
25 ns

S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B2	SoF	**R**
S1	S2	S3	B2	OR254	**R**
S1	S2	S3	B2	Error	**R**
S1	S2	S3	B2	**Sync**	**R**

(R = L1 triggered readout data)

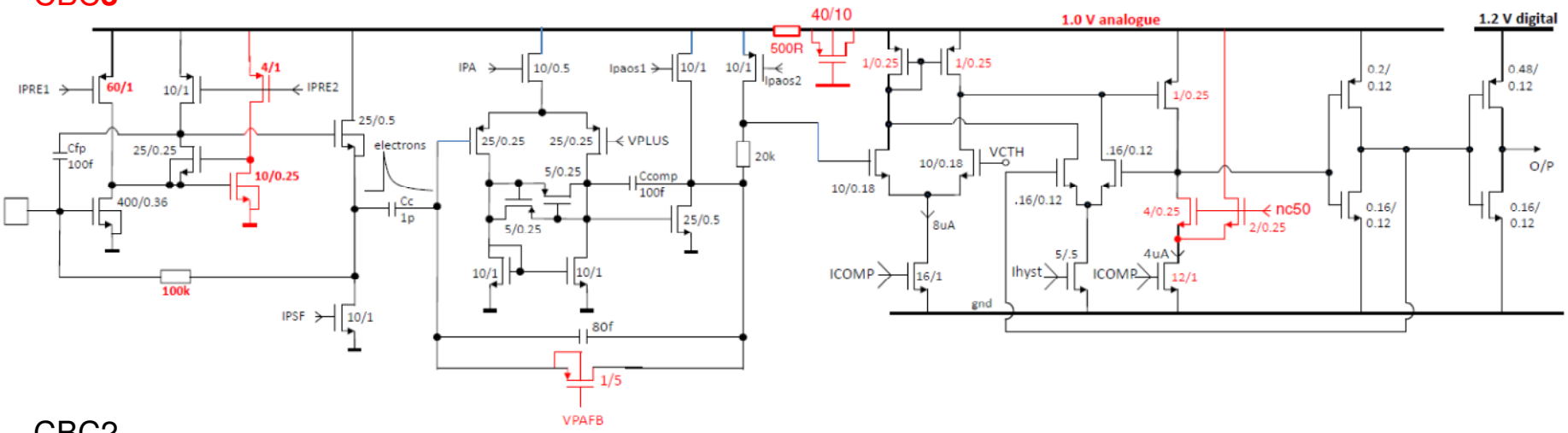


Readout data frame



front end design changes complete

CBC**3**



CBC2