CBC3 preparations

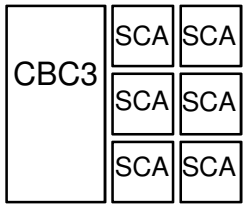
- CBC3
  - production status
  - documentation
  - test system ideas
    - hardware & software
  - test plan schedule
  - modelling
  - sync pattern generation

systems meeting, 20th September, 2016.

CBC3 production

CBC3 sharing wafer with GBT-SCA chip

1 CBC3 : 6 SCA



SCA is wire-bond chip
CBC3 has one wire-bond column

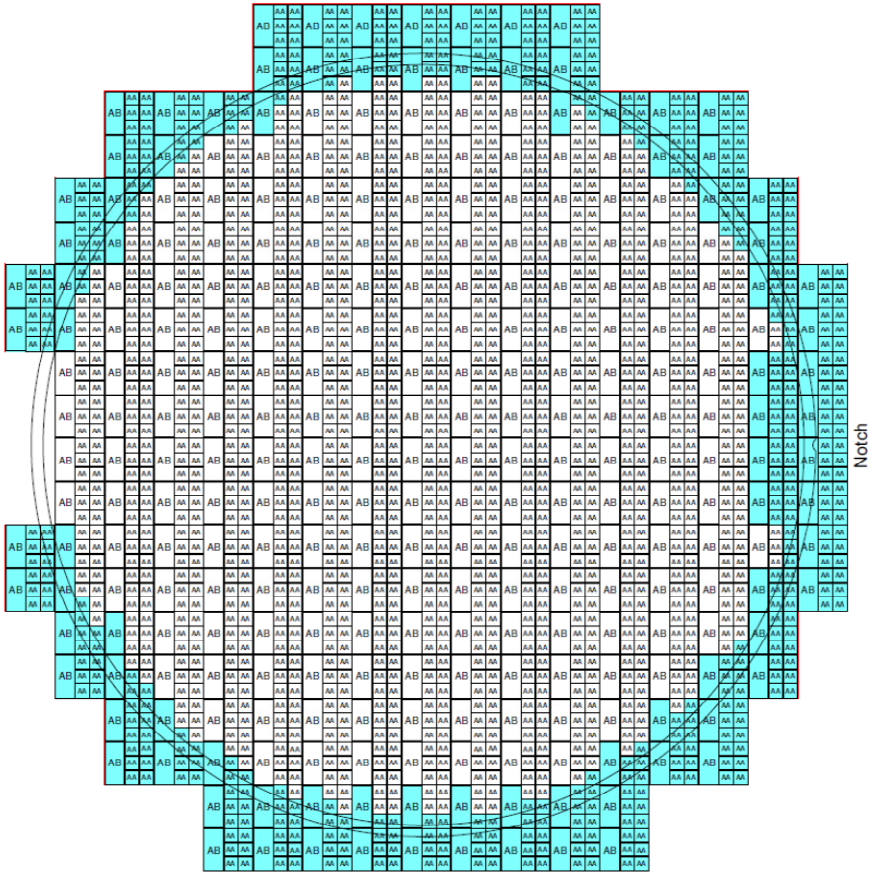
186 CBC3 chips / wafer

6 wafers shipped from MOSIS to CERN 18th October

1 will be thinned (280 um) & diced

½ CBC3 dice (93) available
(more than enough)

5 to be used for bumping



=> ~850 bumpable chips

if necessary can buy more engineering wafers later (if available) or a full production lot

CBC3 documentation

for the less familiar a user manual is required

will certainly appear, but not yet ready

for more expert users (who want to start preparations now)

spec document describes interfaces

http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Technical_Spec_V1p3.docx

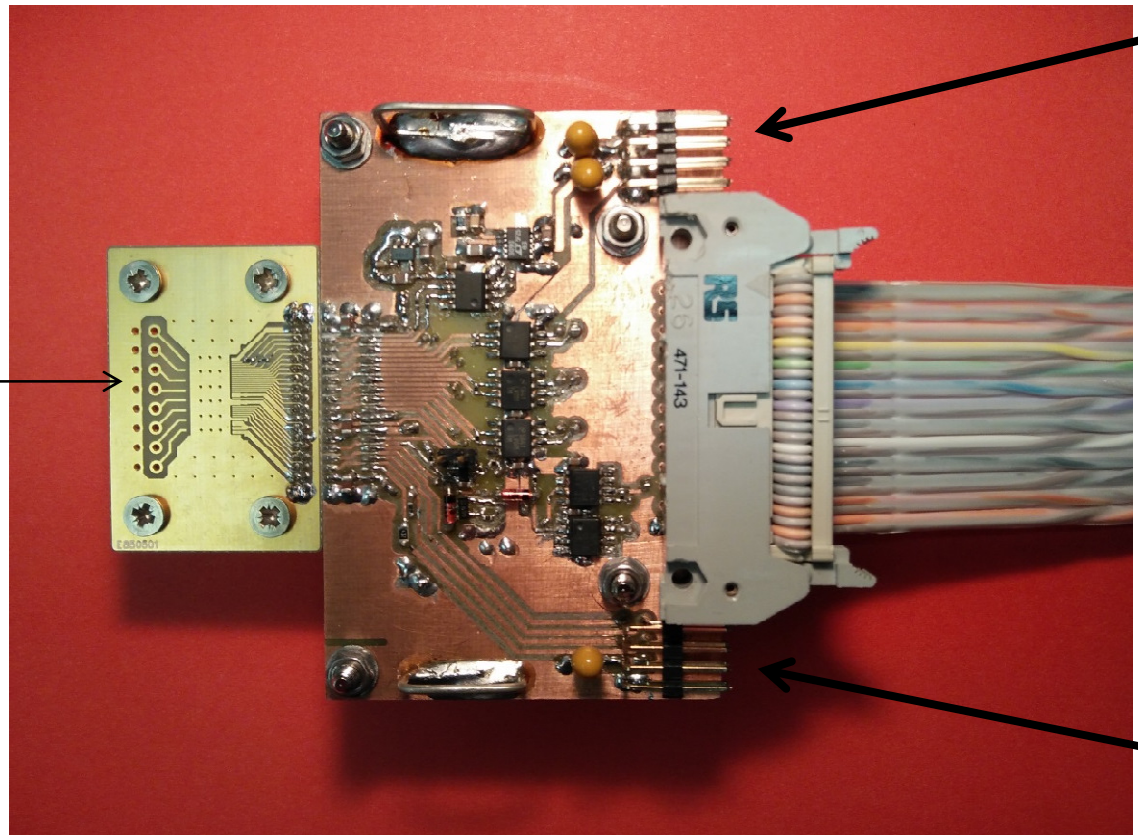
I2C address list

preliminary version exists and being used for DAQ firmware/software development

pad layout

http://www.hep.ph.ic.ac.uk/~dmray/pictures/CBC3_PADS_Footprint1.png

single wirebonded chip test system



+3.3V, -2V

provision to inject charge electrically on a few channels

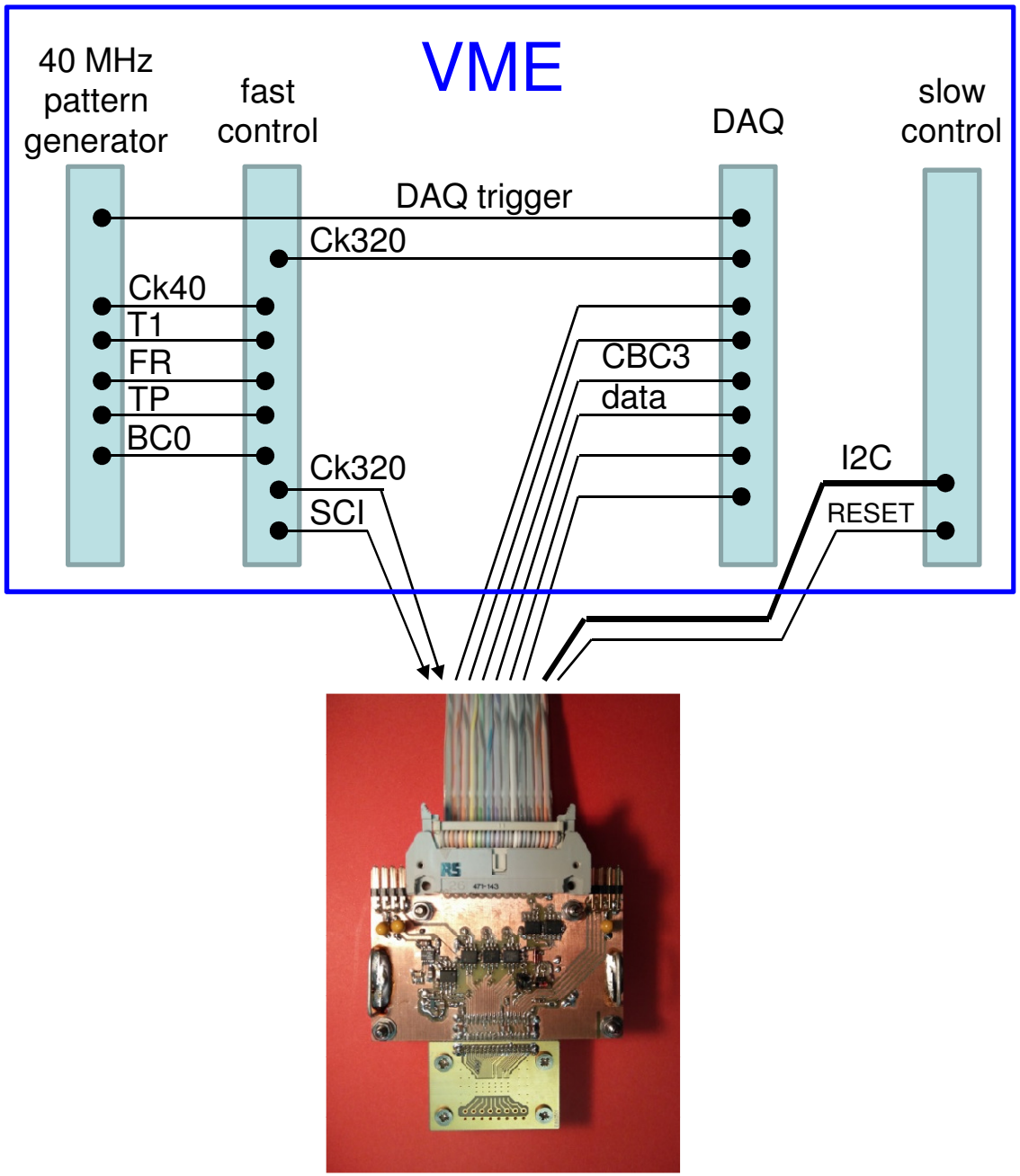
12 LVDS signals
Ck320, SCI inputs
6 output data
SDA to CBC
SDA from CBC
SCK
RESET

1.2 V power,
AMUX,
VDDA,
efuse signals

can be connected to VME DAQ and control system
- first tests, develop probe tests, efuse blowing, ..
- similar interface card will be mounted (piggyback) on probe card ← probe card ordered

can also interface to FMC (FC7)
- will be used for ionising and SEU tests

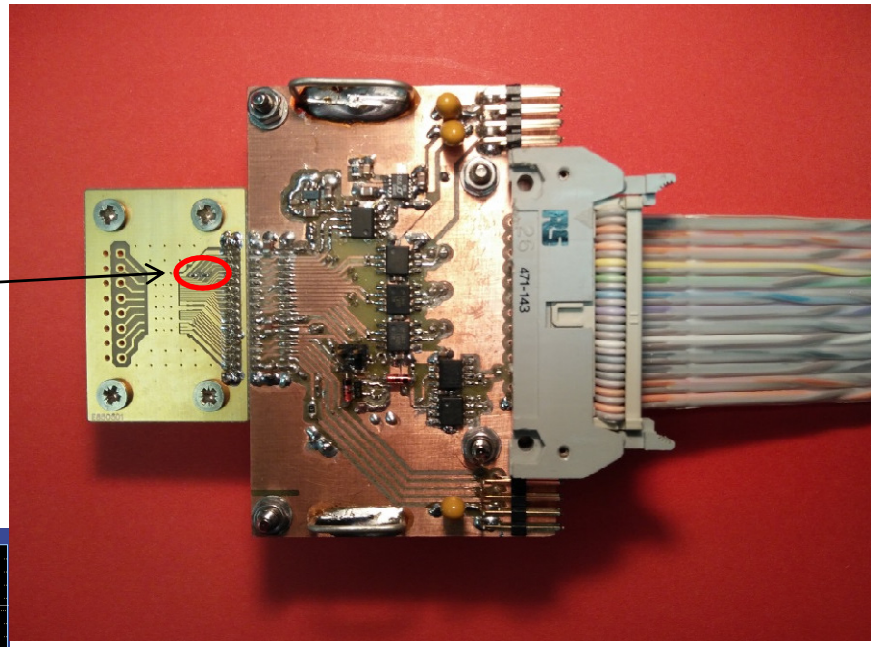
VME DAQ system hardware

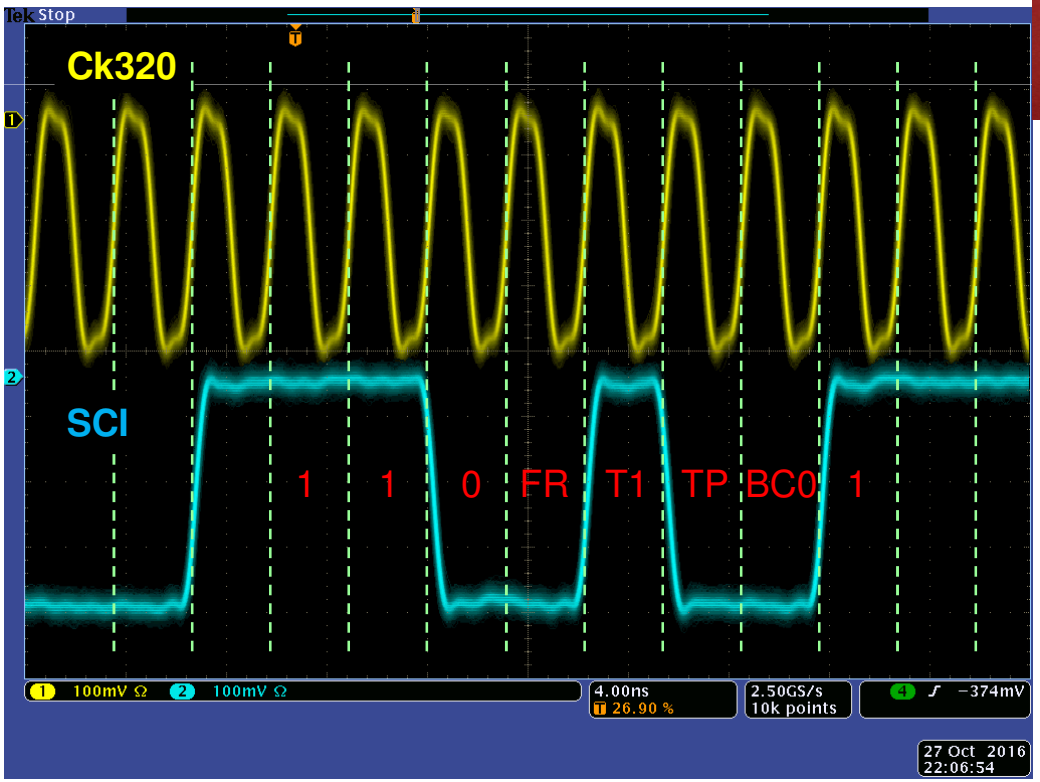


fast control signals from VME system

LVDS signals buffered by DS90LV001 chips
(see last time)

diff. probes here

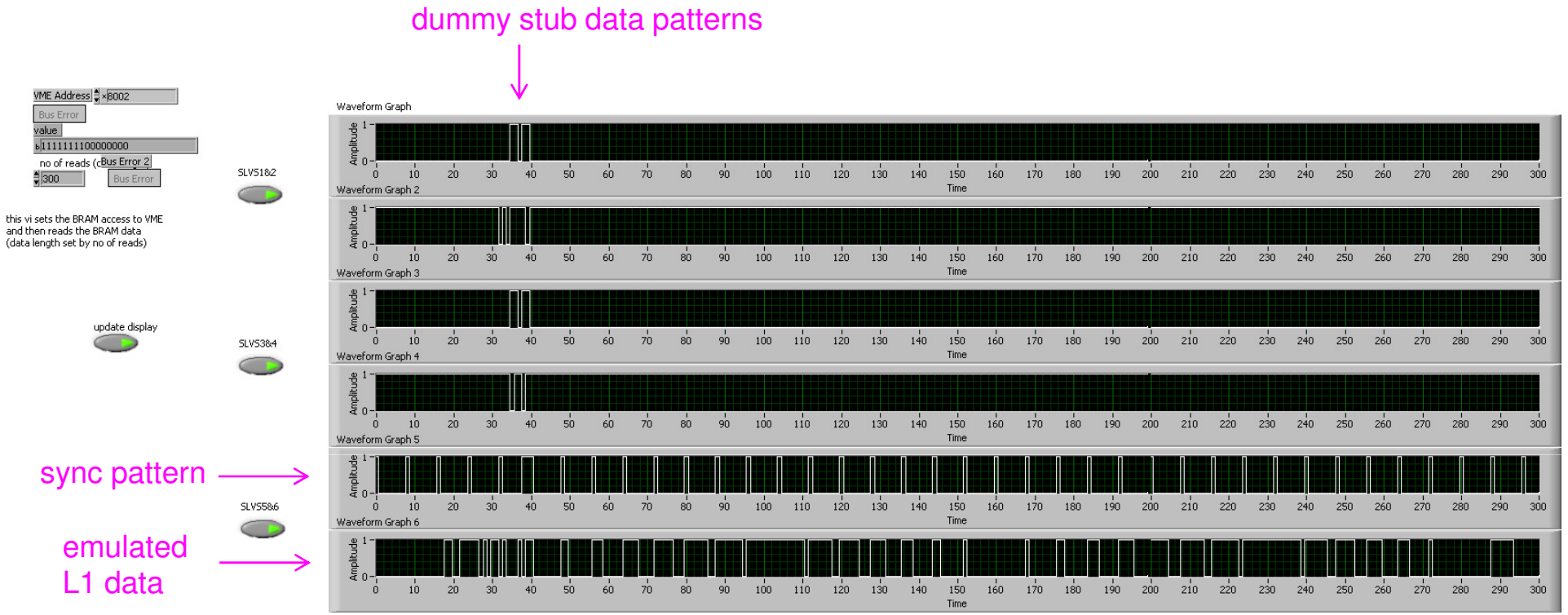




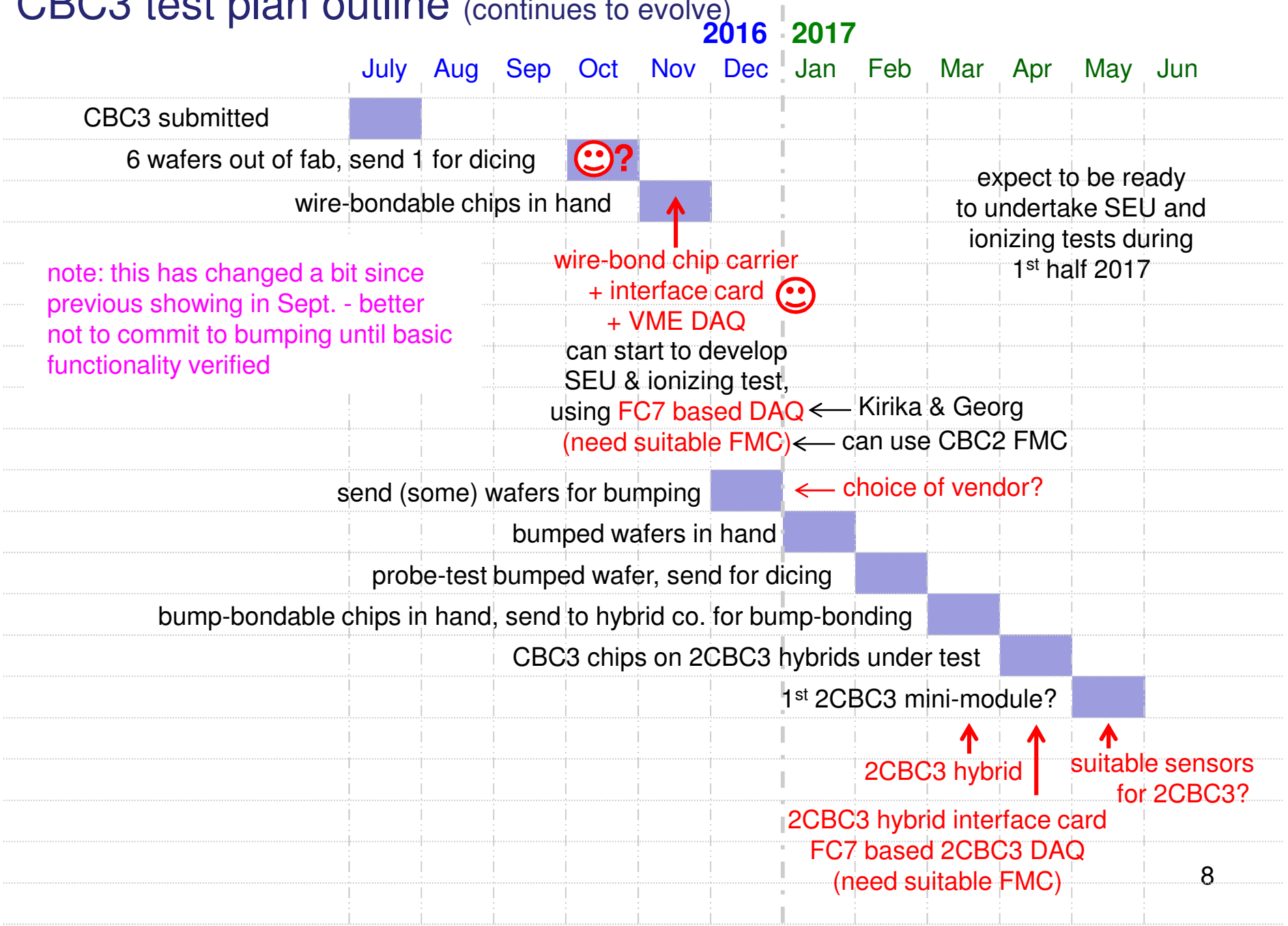
← 320 MHz

← 320 Mbps

basic VME DAQ software ready



CBC3 test plan outline (continues to evolve)



Science & Technology Facilities Council

Stephen Bell, RAL

CBC3 system model requirements

- What are the requirements for the CBC3 system model?
  - What is it to test or interface to? CIC
  - What type of output data is it required to produce?
- What is the level of complexity
  - Cycle accurate?
  - Simplified FE analogue circuitry as digital on/off signals?
- What tool environment is it to be used in?

- Current status
  - Mixed-signal model created and runs with Cadence AMS simulator
  - Mixture of RTL, gate level and transistor level blocks are modelled

CIC sync pattern generation thoughts

SLVS<5> has the sync bit

SLVS<1>, <2> , <3> and <4> can have fixed repetitive data by setting VCTH so that all channels are permanently firing, and then using channel mask to unmask 3 specific seed and window channel combinations

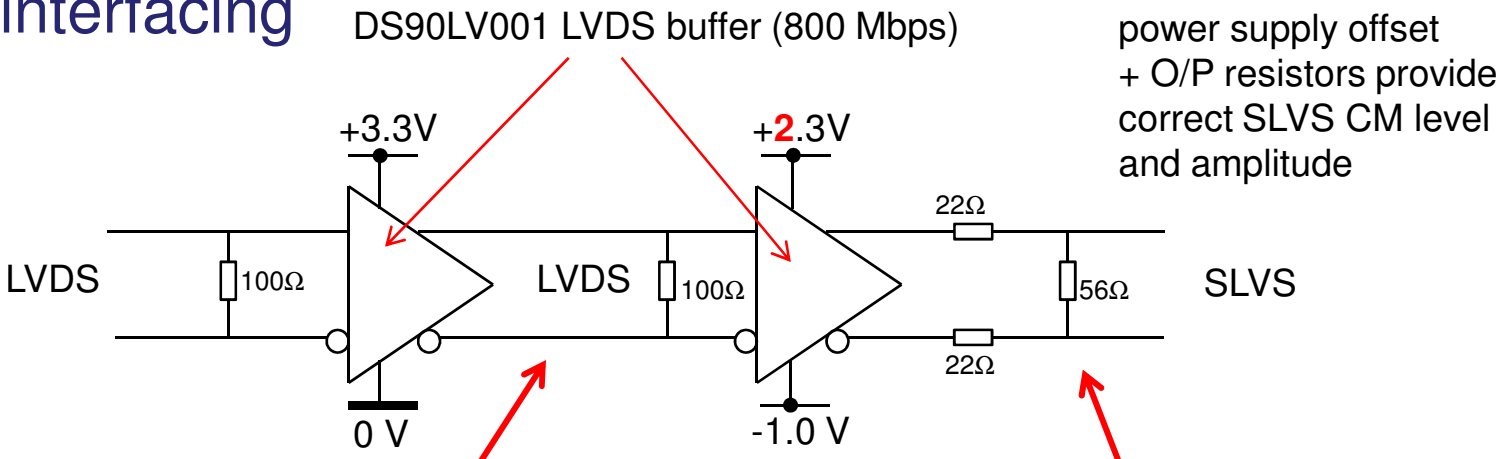
SLVS<6> can also have fixed repetitive data by triggering readout, but not a 25 nsec repetitive pattern

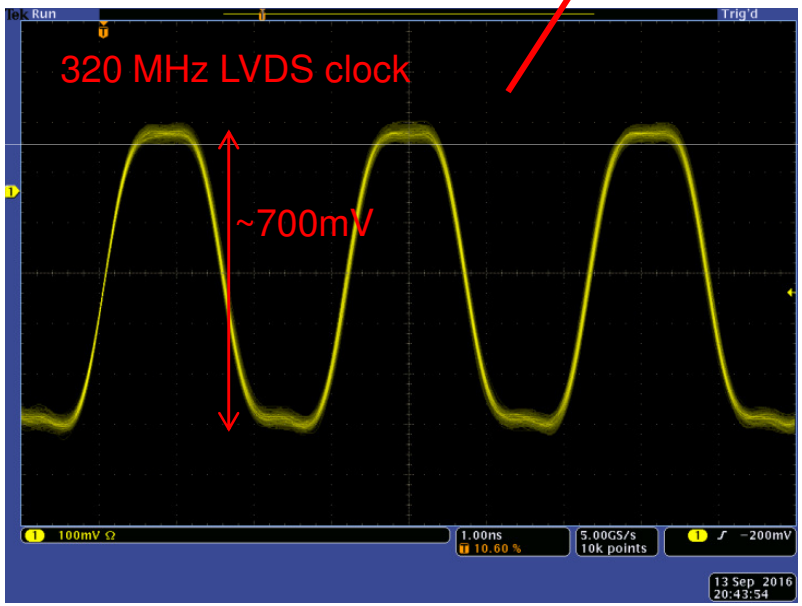
SLVS <1> …. <6>

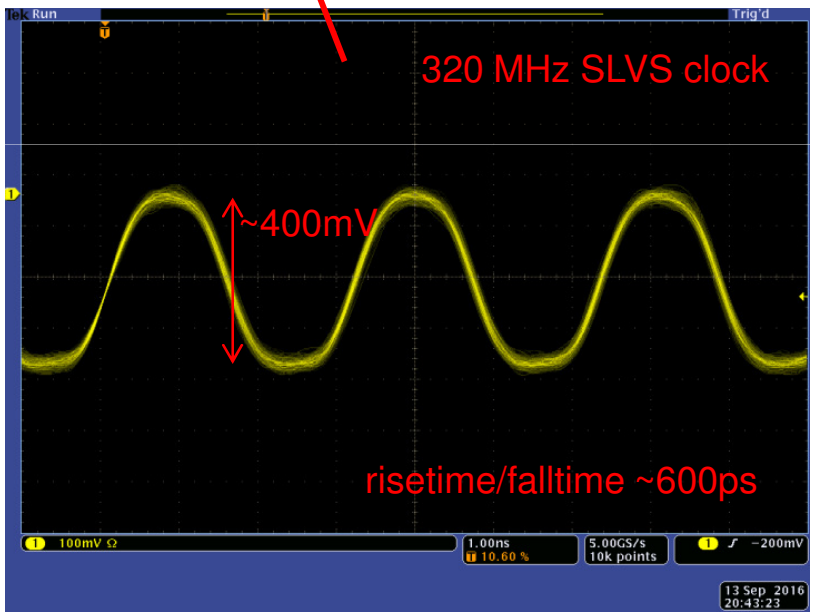
S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	**R**
S1<6>	S2<6>	S3<6>	B2<2>	Error	**R**
S1<5>	S2<5>	S3<5>	B2<1>	OR254	**R**
S1<4>	S2<4>	S3<4>	B2<0>	SoF	**R**
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	**R**
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	**R**
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	**R**
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	**R**

extra

SLVS interfacing

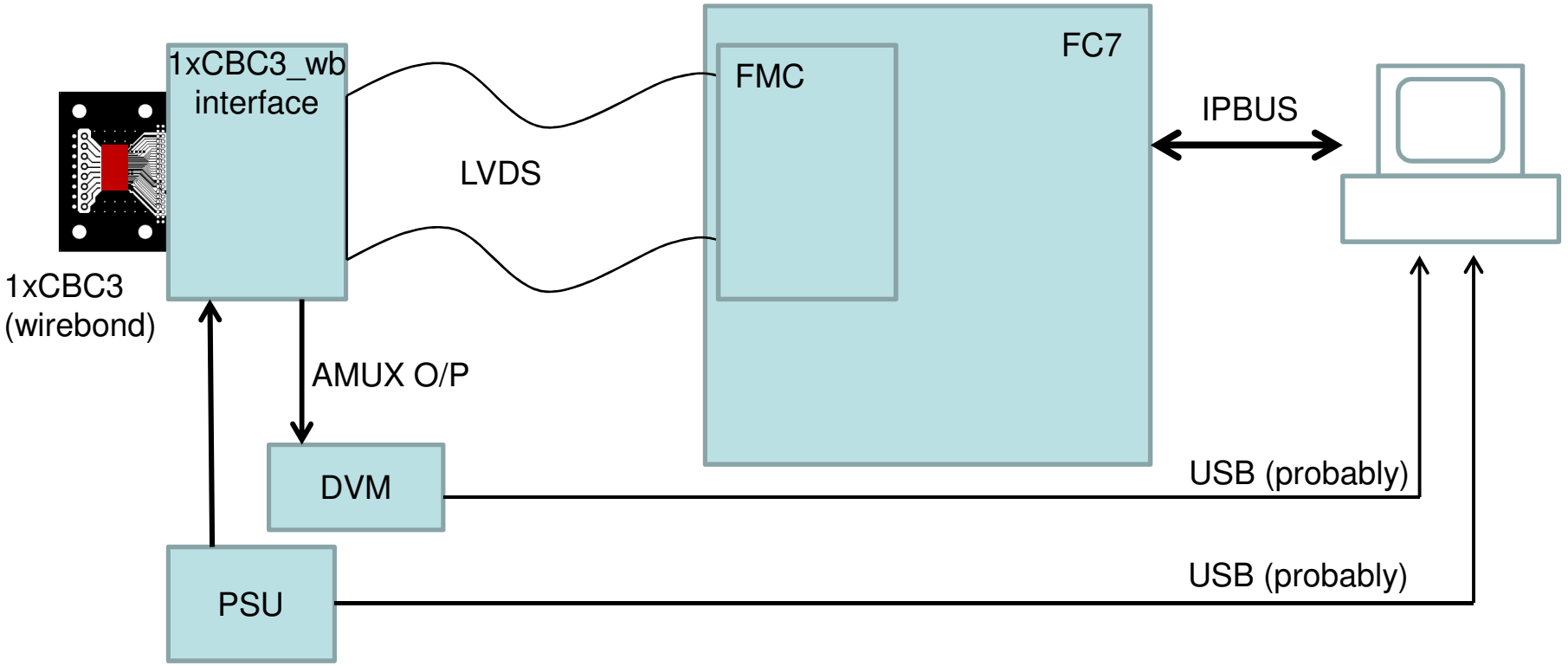






for SLVS -> LVDS just use one DS90LV001 (0 and 3.3V supplies)
CM acceptance range of LV001 can cope with SLVS levels

software - for ionizing and SEU tests (assume UK responsibility)

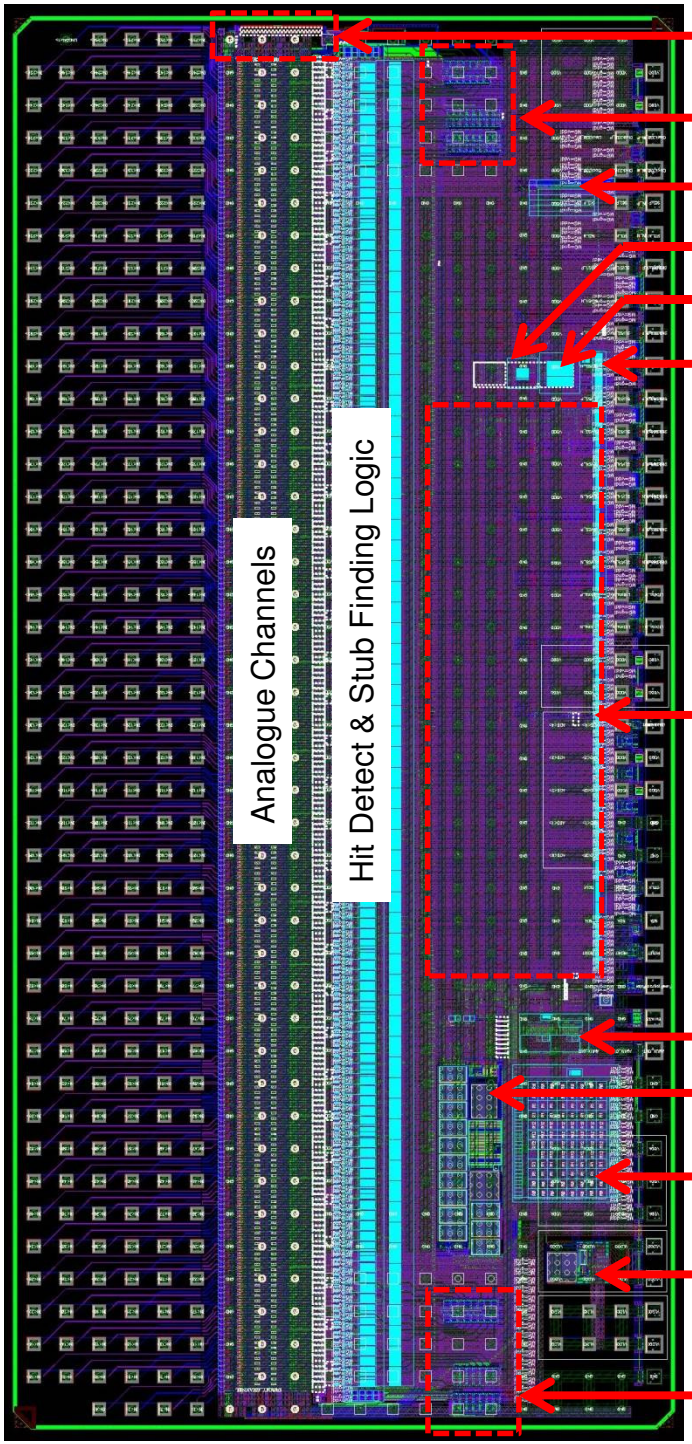


based on CBC2 middle-ware

control and DAQ procedures
PSU current monitoring
AMUX O/P monitoring

} processes need to be synchronized (e.g. monitor PSU current and/or AMUX O/P while sweeping I2C parameter)
data-logging (time-stamping) required for ionizing tests

CBC3



test pulse circuit

I/O to neighbour

DLL

bend LUT

data assembly

L1 counter & FIFO

512 deep pipeline & O/P buffer

bandgap

I2C & biases

10b DAC for VCTH

LDO

I/O to neighbour

final layout picture for reference

20 columns, 43 rows
(1 more column than CBC2)

5.25 mm x 11 mm

CBC3 digital interfaces

output data: up to 3 stubs data transmitted to CIC/BX
6 SLVS diff pairs @ 320 Mbps

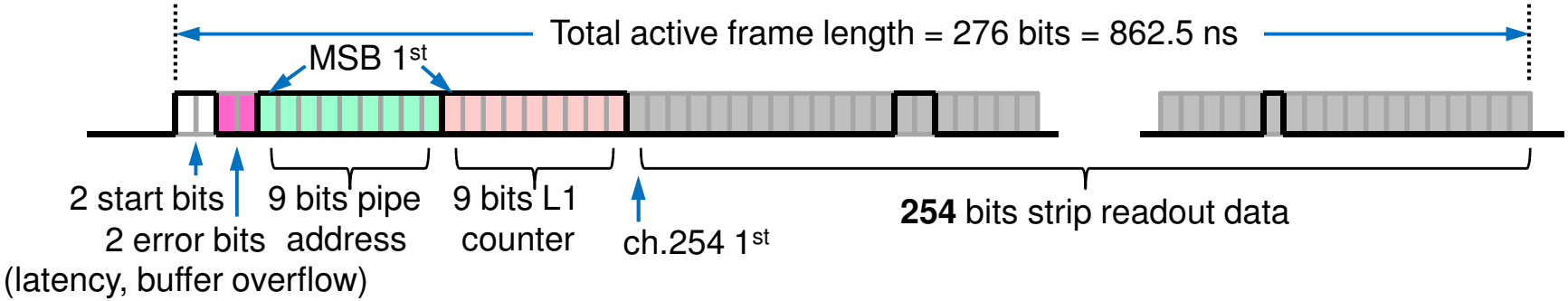
25 ns

S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	**R**
S1<6>	S2<6>	S3<6>	B2<2>	Error	**R**
S1<5>	S2<5>	S3<5>	B2<1>	OR254	**R**
S1<4>	S2<4>	S3<4>	B2<0>	SoF	**R**
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	**R**
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	**R**
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	**R**
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	**R**

R = L1 triggered readout data
time flow **top** to **bottom** (e.g. S1<7> output first)

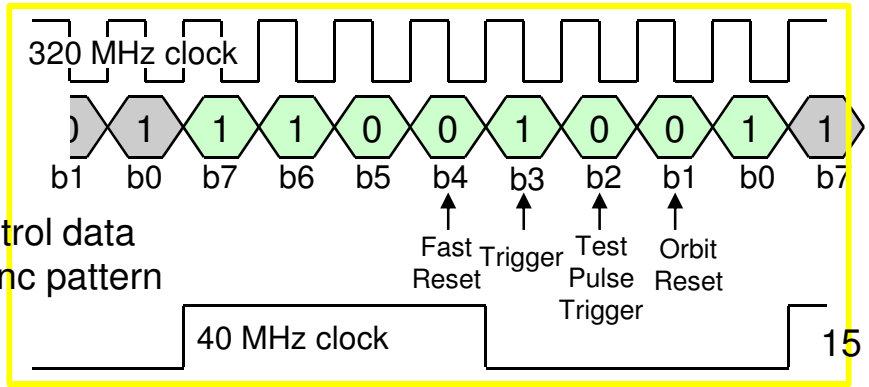
readout data

readout data frame length 950 nsec
=> up to 1 MHz L1 triggering capability



fast control

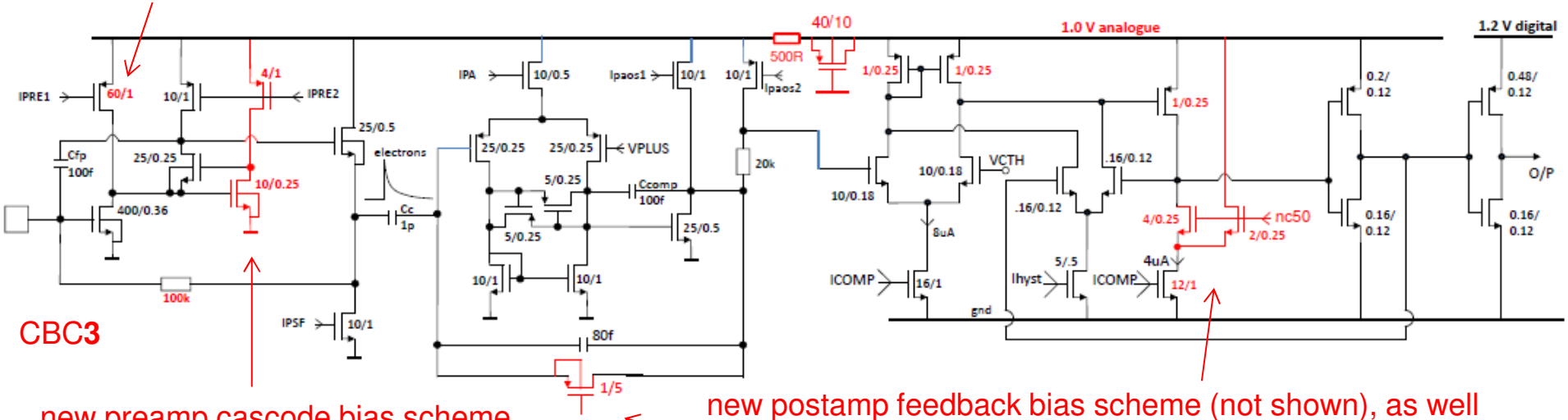
320 MHz clock
320 Mbps fast control line



40 MHz generated from fixed sync pattern in fast control data
normal command structure can't be confused with sync pattern

CBC2 vs. CBC3

increase in bias FET
allows higher currents

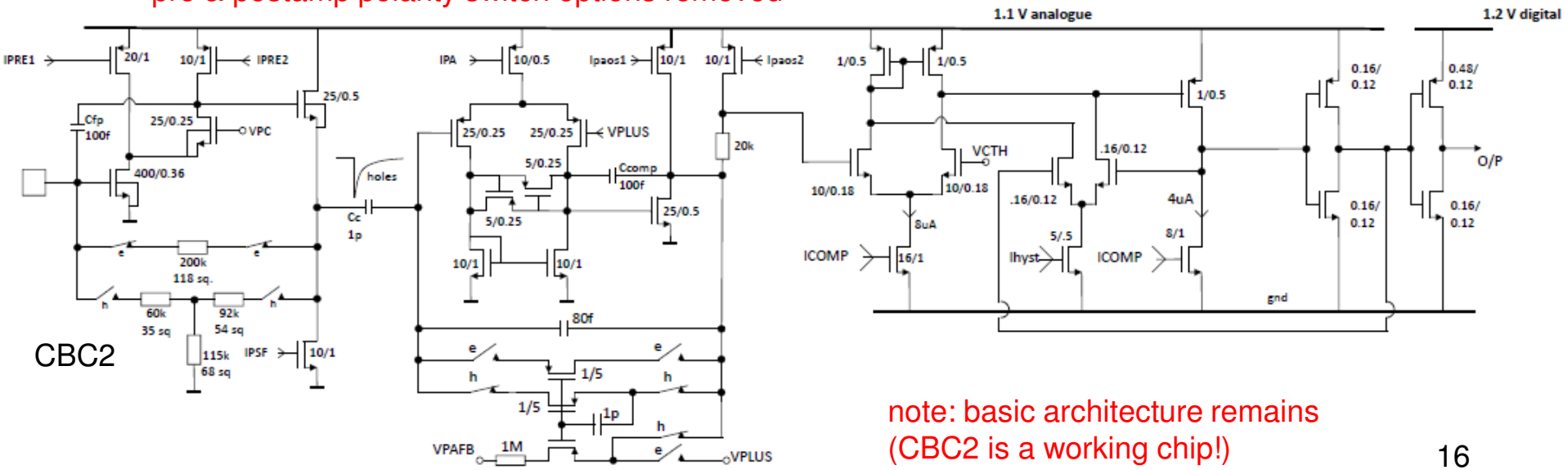


CBC3

new preamp cascode bias scheme
to eliminate “shadow effect”

new postamp feedback bias scheme (not shown), as well as current neutral comparator, addresses CM effects observed when many channels fire

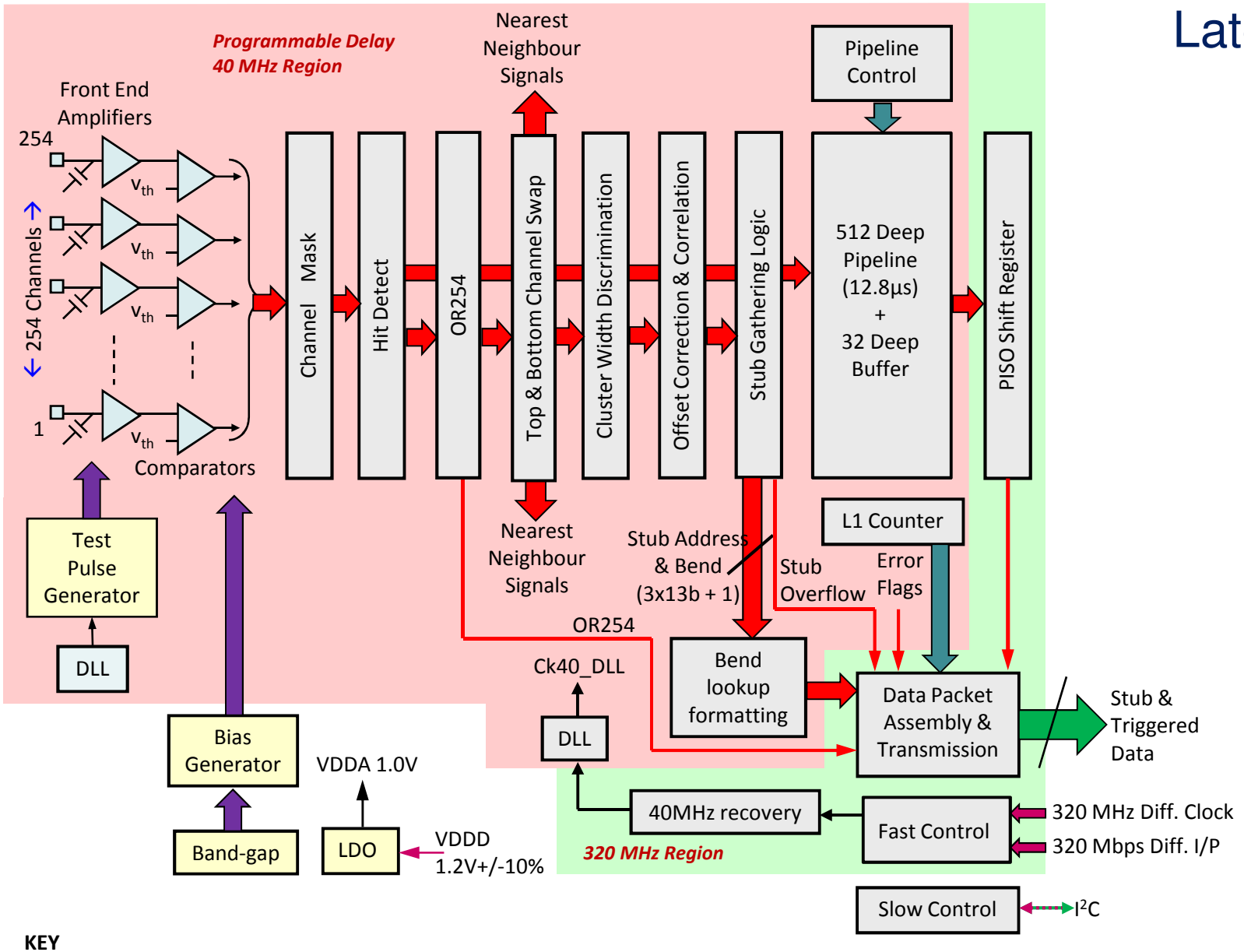
pre & postamp polarity switch options removed



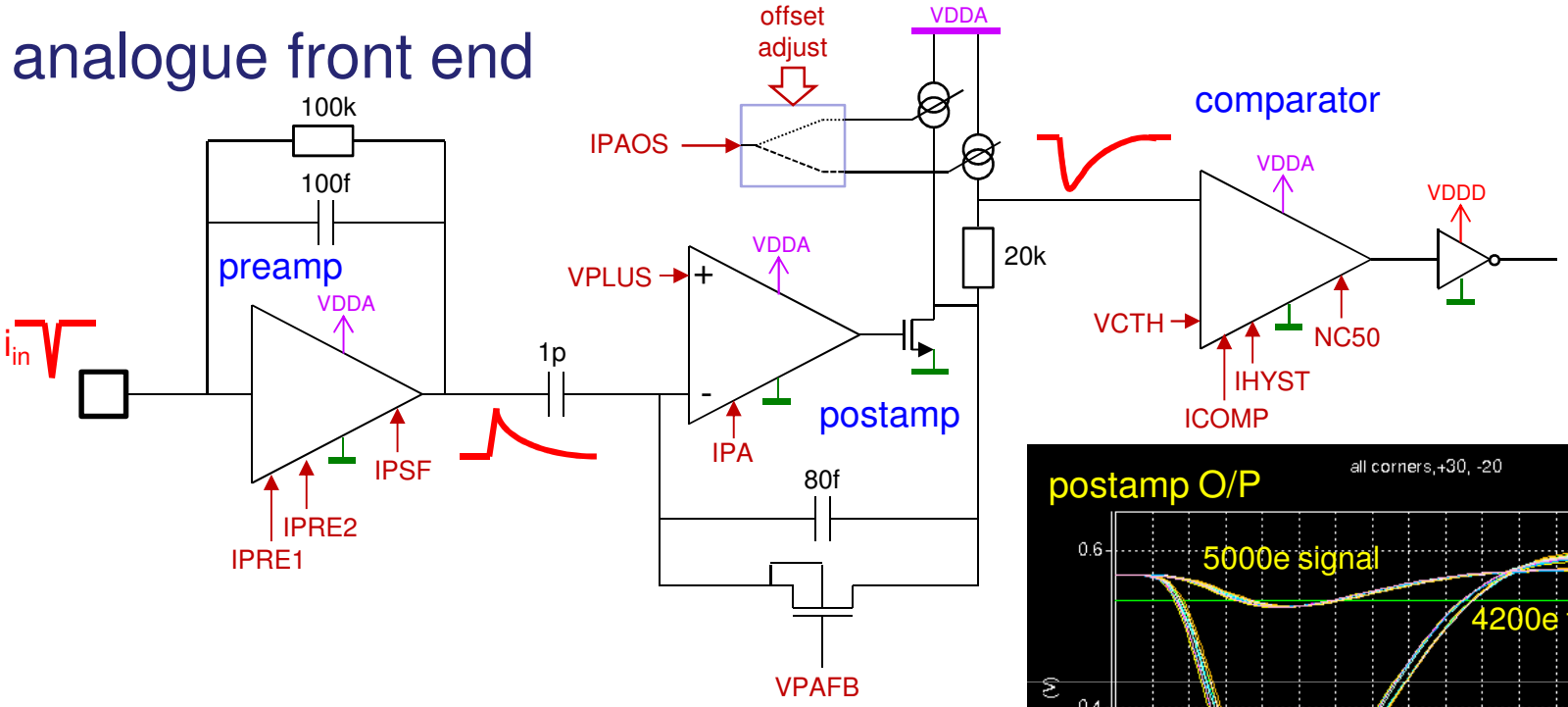
CBC2

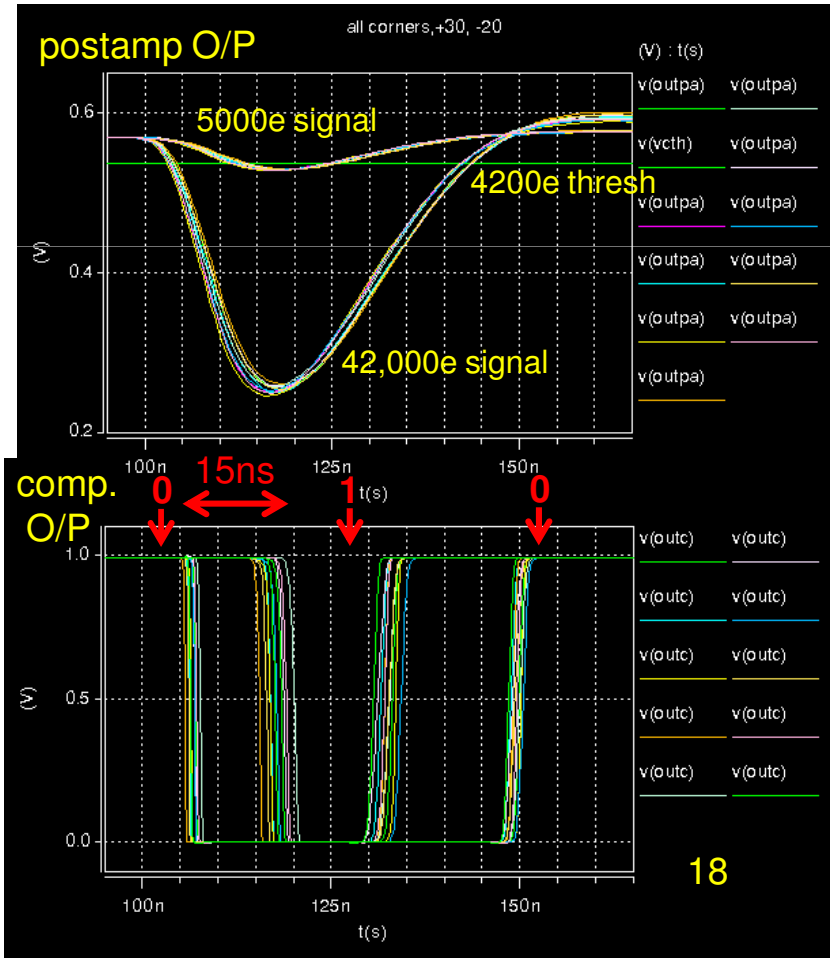
note: basic architecture remains
(CBC2 is a working chip!)

Latest Block Diagram



analogue front end



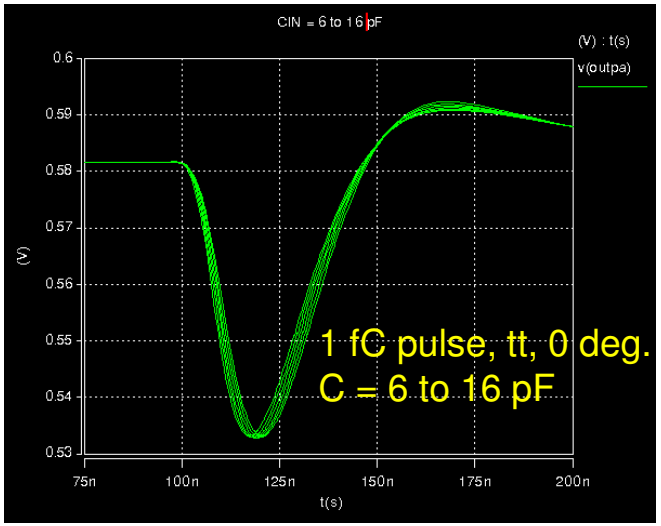


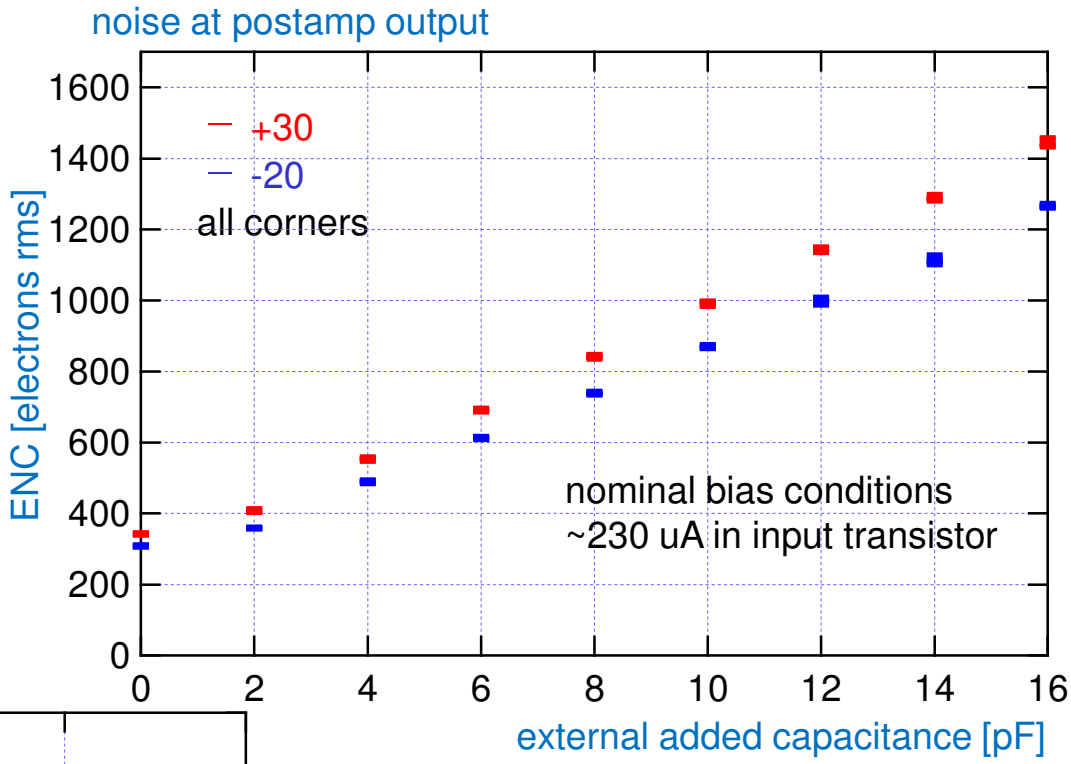
main design changes

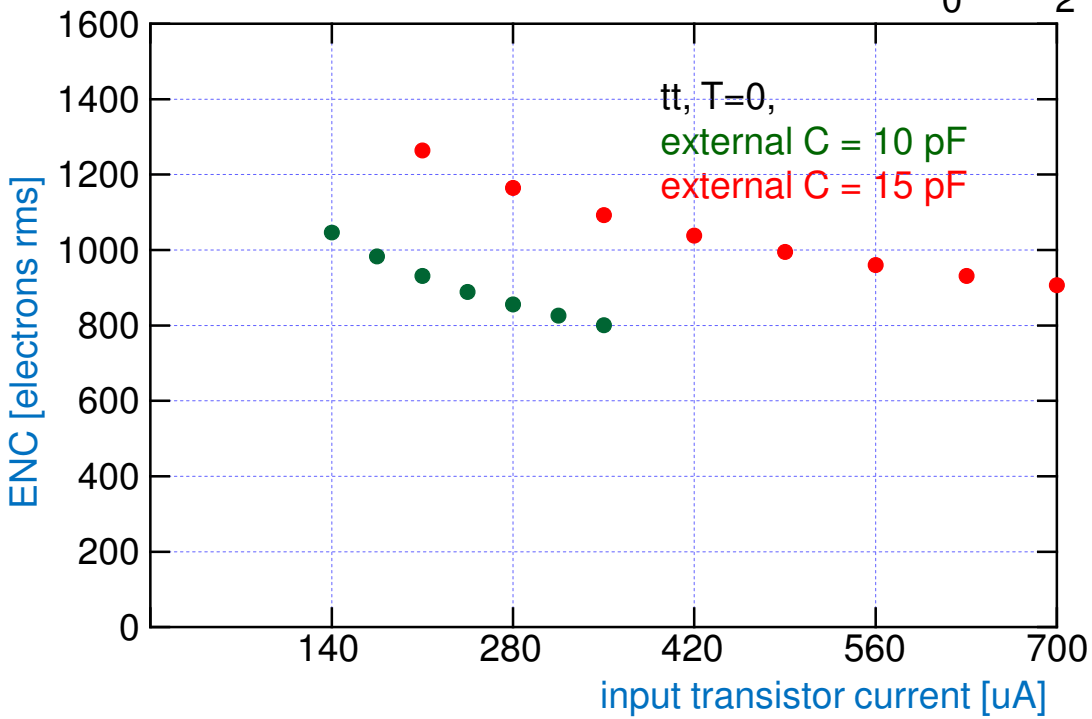
optimised for n-in-p sensors
faster shaping (return to baseline within 50 ns)
VCTH linear, monotonic and 10-bit
CBC2 “shadow” and CM effects addressed

post-layout timewalk simulation

noise







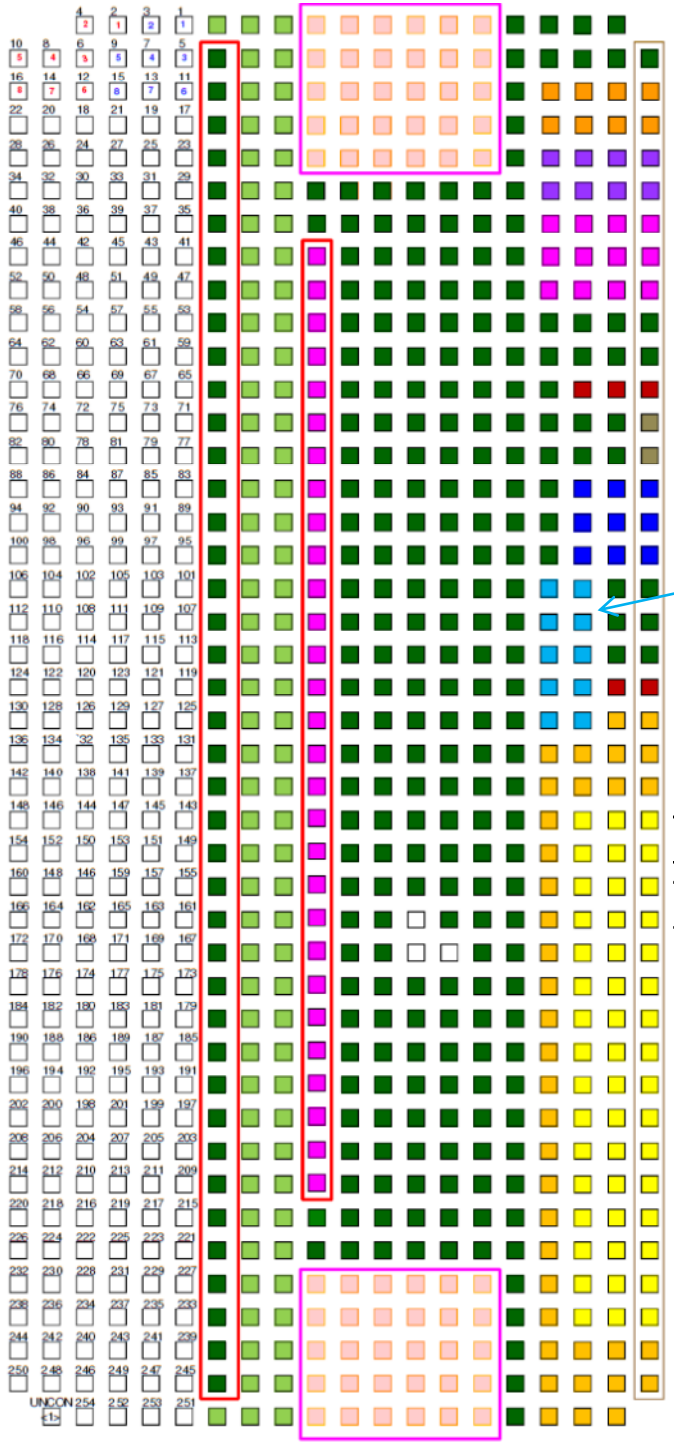
post-layout simulations

1000e achievable for external capacitance up to ~10 pF at preamp input (for acceptable power consumption)

no strong dependence on process corners

pulse shape/height varies not much over quite large input capacitance range

pad allocations



pads as viewed on hybrid surface
(as if looking through chip)

right-most column for wire-bond / wafer probe

like CBC2 gives access to internal
bias currents and voltages

chip ID can be set by e-fuses (19 bits)
will be programmed at wafer probe time
every chip will have unique ID

CERN PMOS bandgap reference
also trimmed by e-fuses (6 bits)

for detailed picture, prepared by Lawrence Jones, showing all pads labelled, download:

http://www.hep.ph.ic.ac.uk/~dmray/pictures/CBC3_PADS_Footprint1.png

note: downloadable picture shows pads as should be laid out on hybrid surface (flipped version of pads on chip)