CBC matters

CBC2
- wafer probing status

CBC3
- production status
- documentation
- test system ideas
  - hardware & software
- test plan schedule

systems meeting, 20th September, 2016.

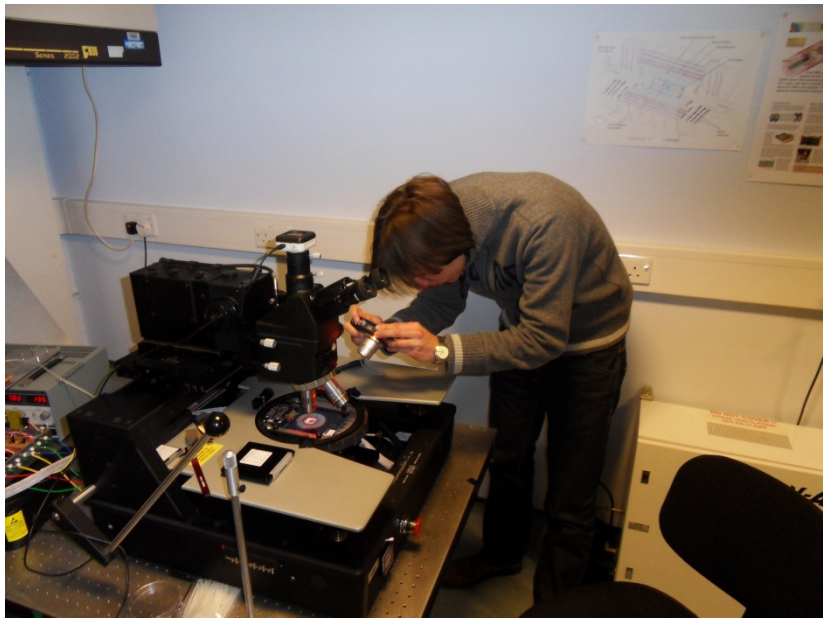
CBC2 wafer probing

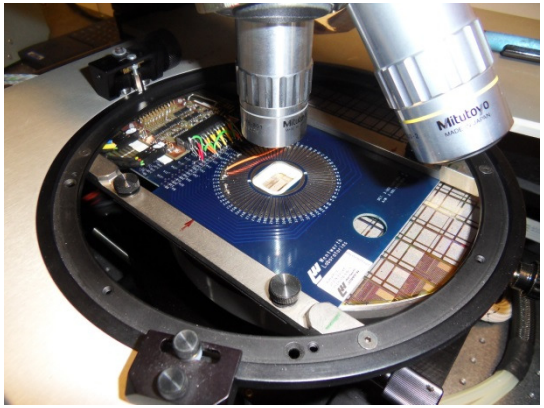
last 4 wafers probed

rigorous functionality tests, see:

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2014/wafer_testing_Sept_14.pdf

all I2C registers, channels, pipeline locations
s-curves for pedestals and response to test pulse
bias current/voltage sweeps, power, …..

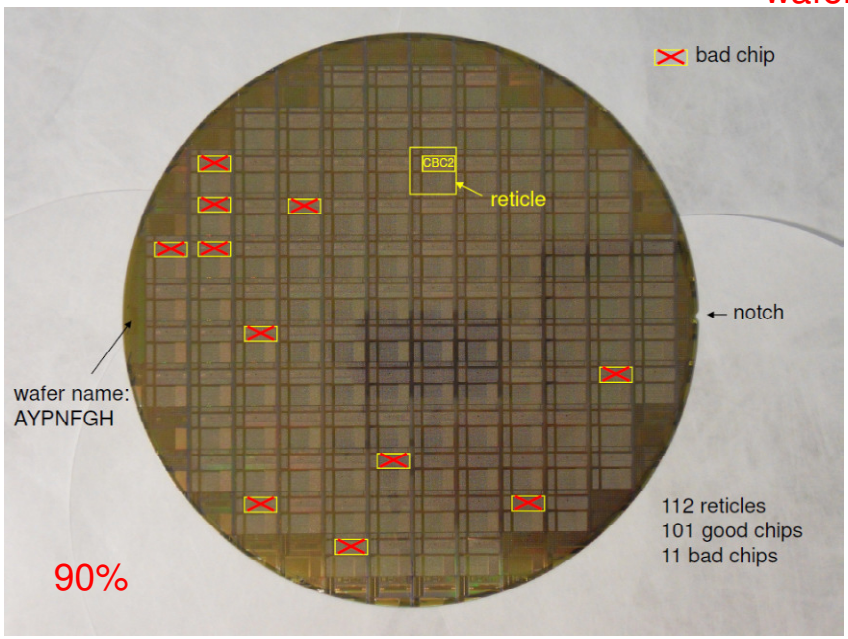


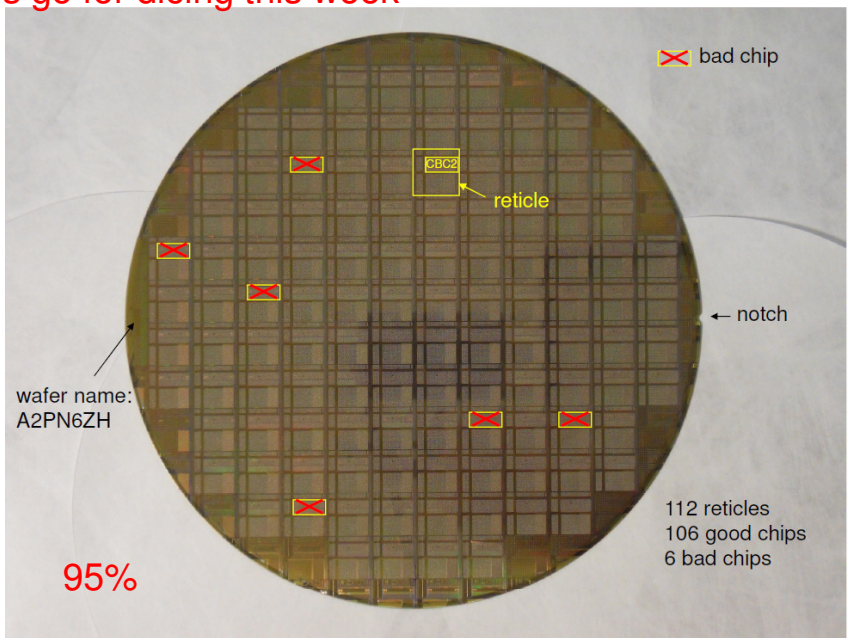


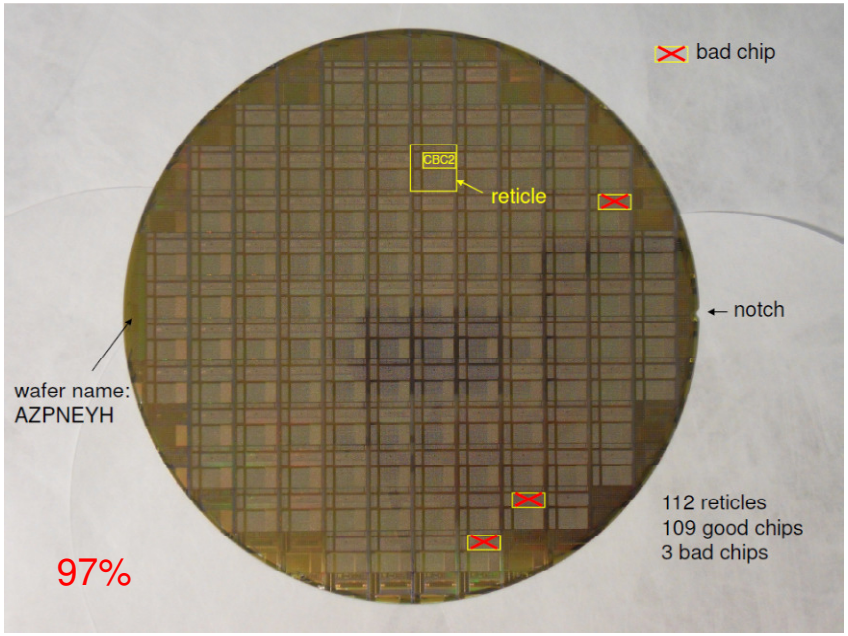
CBC2 wafer probing

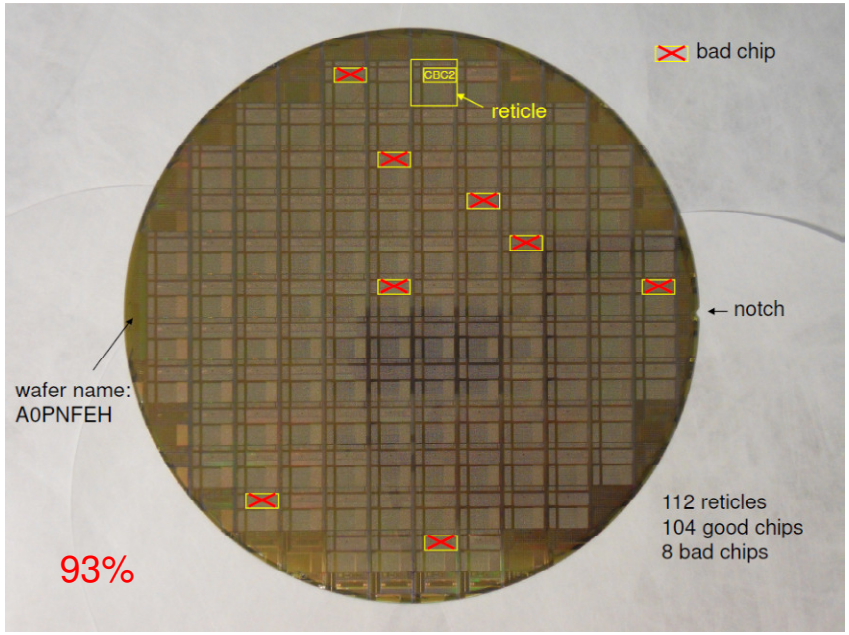
420 good chips

wafers go for dicing this week

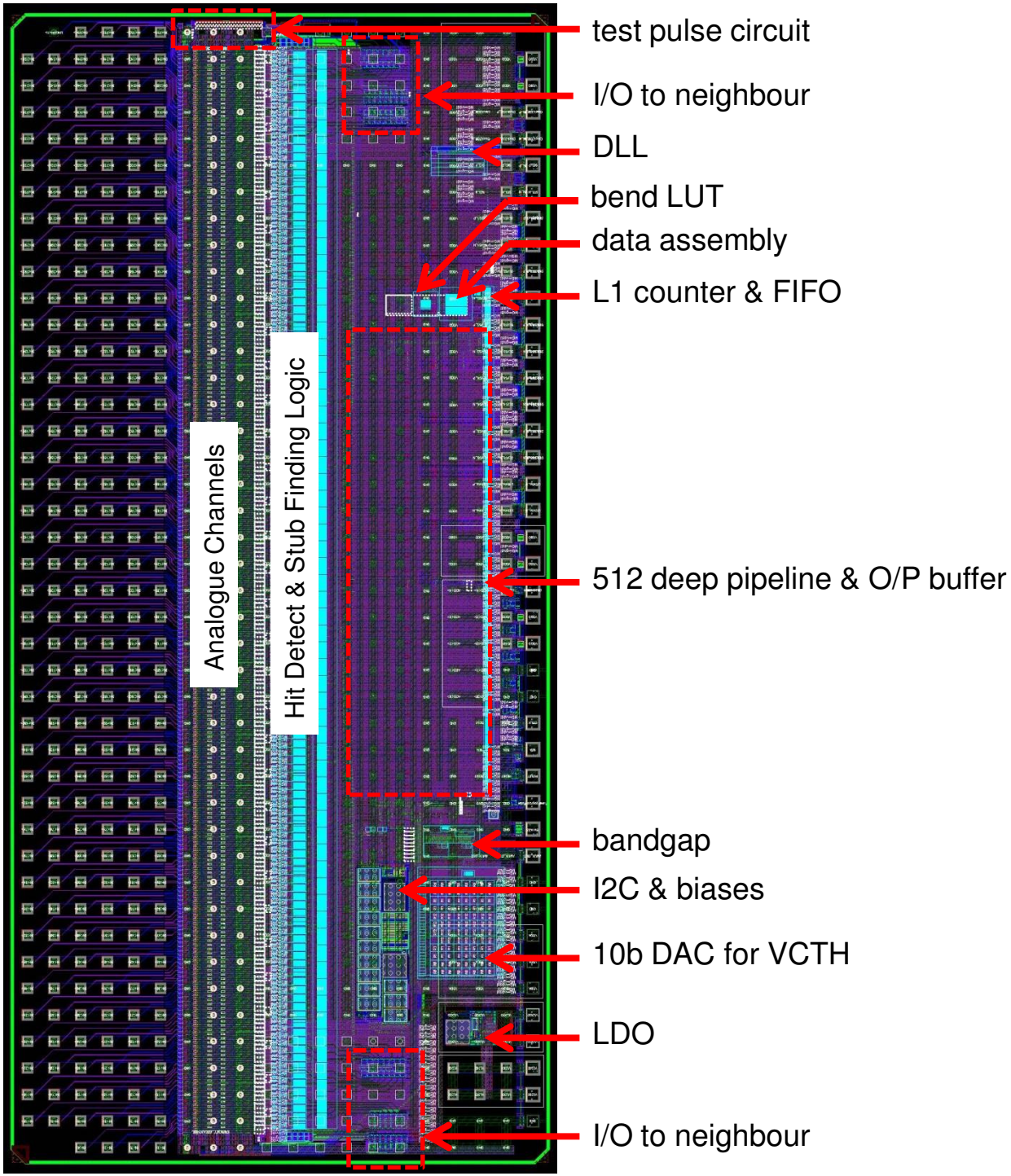








CBC3



test pulse circuit

I/O to neighbour

DLL

bend LUT

data assembly

L1 counter & FIFO

512 deep pipeline & O/P buffer

bandgap

I2C & biases

10b DAC for VCTH

LDO

I/O to neighbour

final layout picture for reference

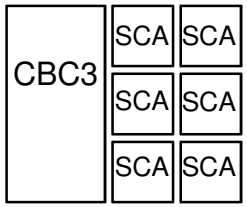
20 columns, 43 rows
(1 more column than CBC2)

5.25 mm x 11 mm

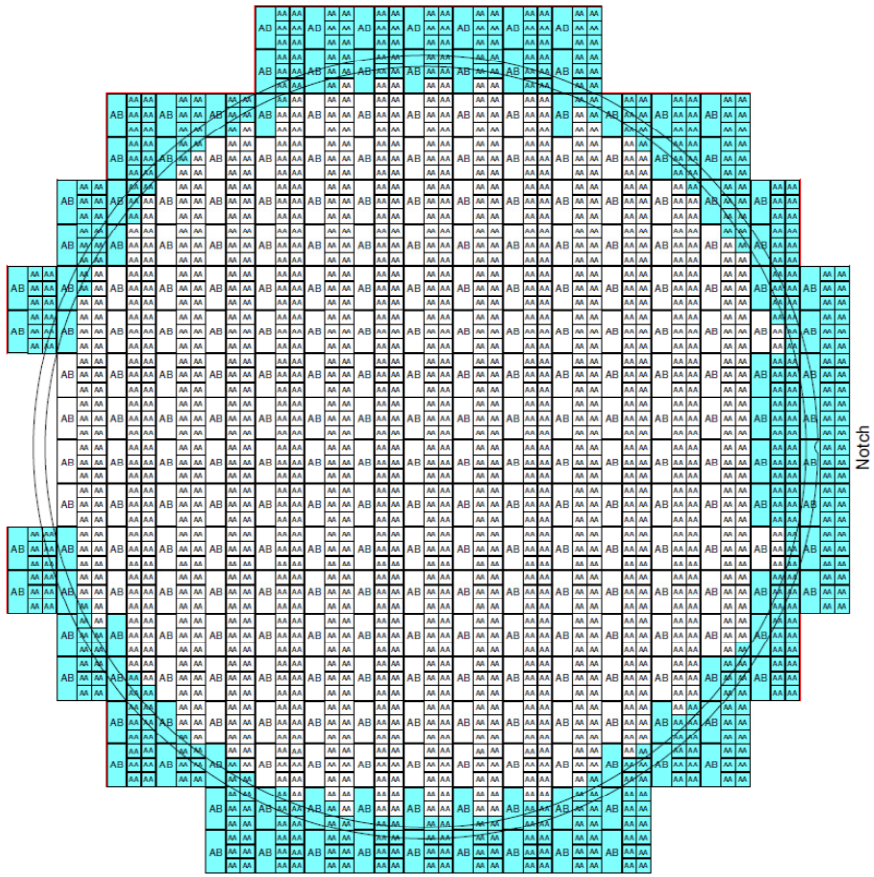
CBC3 production

CBC3 sharing wafer with GBT-SCA chip

1 CBC3 : 6 SCA



SCA is wire-bond chip
CBC3 has one wire-bond column



186 CBC3 chips / wafer

fast production on 2 month turnaround

6 wafers (initially) to be delivered un-bumped

1 will be immediately diced
5 to be used for bumping

=> ~850 bumpable chips

if necessary can buy more engineering wafers later (if available)
or a full production lot

?

latest info from Kostas: “7 engineering wafers from the initial lot @ RTAT. GF ships **10/10/16**,
MOSIS will receive and ship to CERN on 11/10/16”

bump pad size

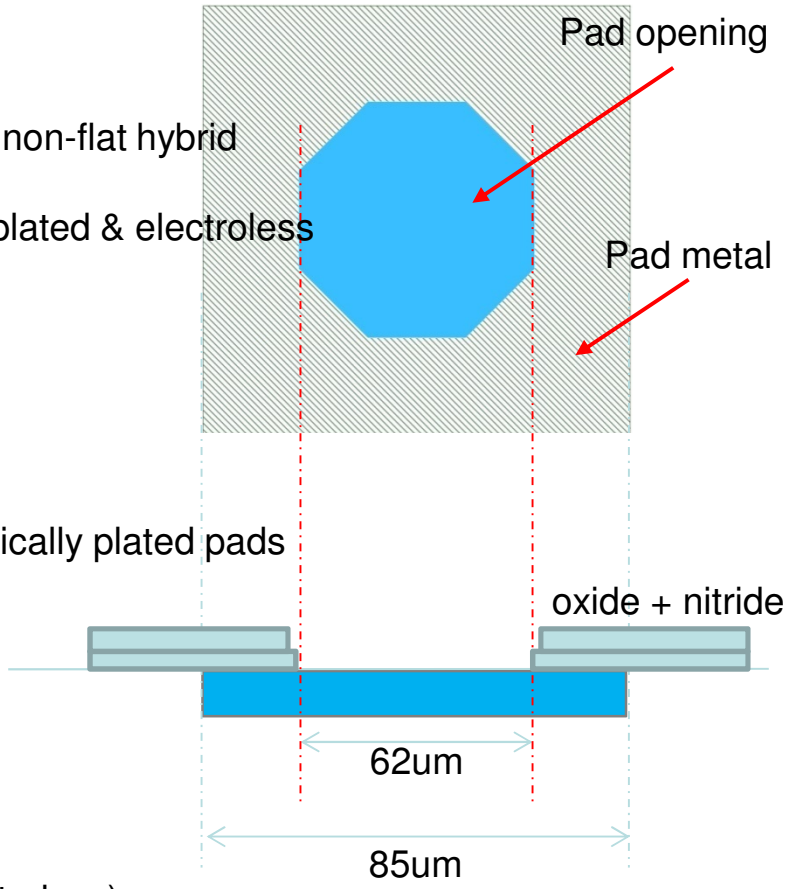
IBM process used for CBC2 - no longer available

large bump size (~ 150 um), good for compensating for non-flat hybrid

investigations by Georges - 2 approaches available - electroplated & electroless

electroplated - most widely used in industry
but thin (~20um) photoresist masks => small bump size
=> not favoured for CBC3

electroless - more often used for prototyping
bumps mechanically deposited through stencil on chemically plated pads
bump diameter up to 2 x pad diameter



after discussions (and further investigations by Francois)

pad size decision

62 um opening allowing bump size up to ~125 um (electroless)
bit less than CBC2 but still quite large
could still probably be used with electroplated technique

same size as used for CERN DCDC chip
compatible with default bump-bonding pad size offered by TSMC

note: we are omitting polyimide finish on first wafers in case it interferes with bump-bond processing - could be added on subsequent wafer orders if we want

CBC3 documentation

for the less familiar a user manual is required

will certainly appear, but not yet ready

for more expert users (who want to start preparations now)

spec document describes interfaces

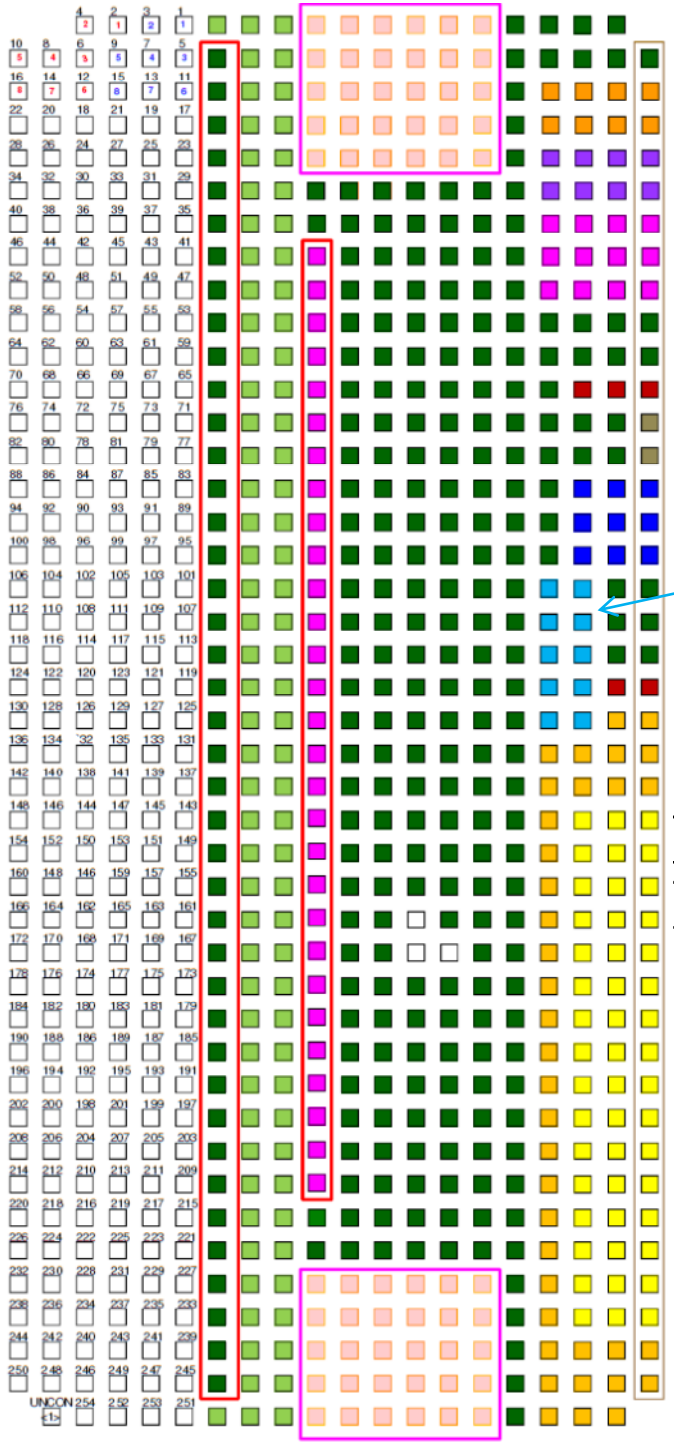
http://www.hep.ph.ic.ac.uk/~dmray/CBC_documentation/CBC3_Technical_Spec_V1p3.docx

I2C address list

Lawrence has prepared, Mark (Prydderch) is checking, available soon

pad layout (next slide)

pad allocations



pads as viewed on hybrid surface
(as if looking through chip)

right-most column for wire-bond / wafer probe

like CBC2 gives access to internal
bias currents and voltages

chip ID can be set by e-fuses (19 bits)
will be programmed at wafer probe time
every chip will have unique ID

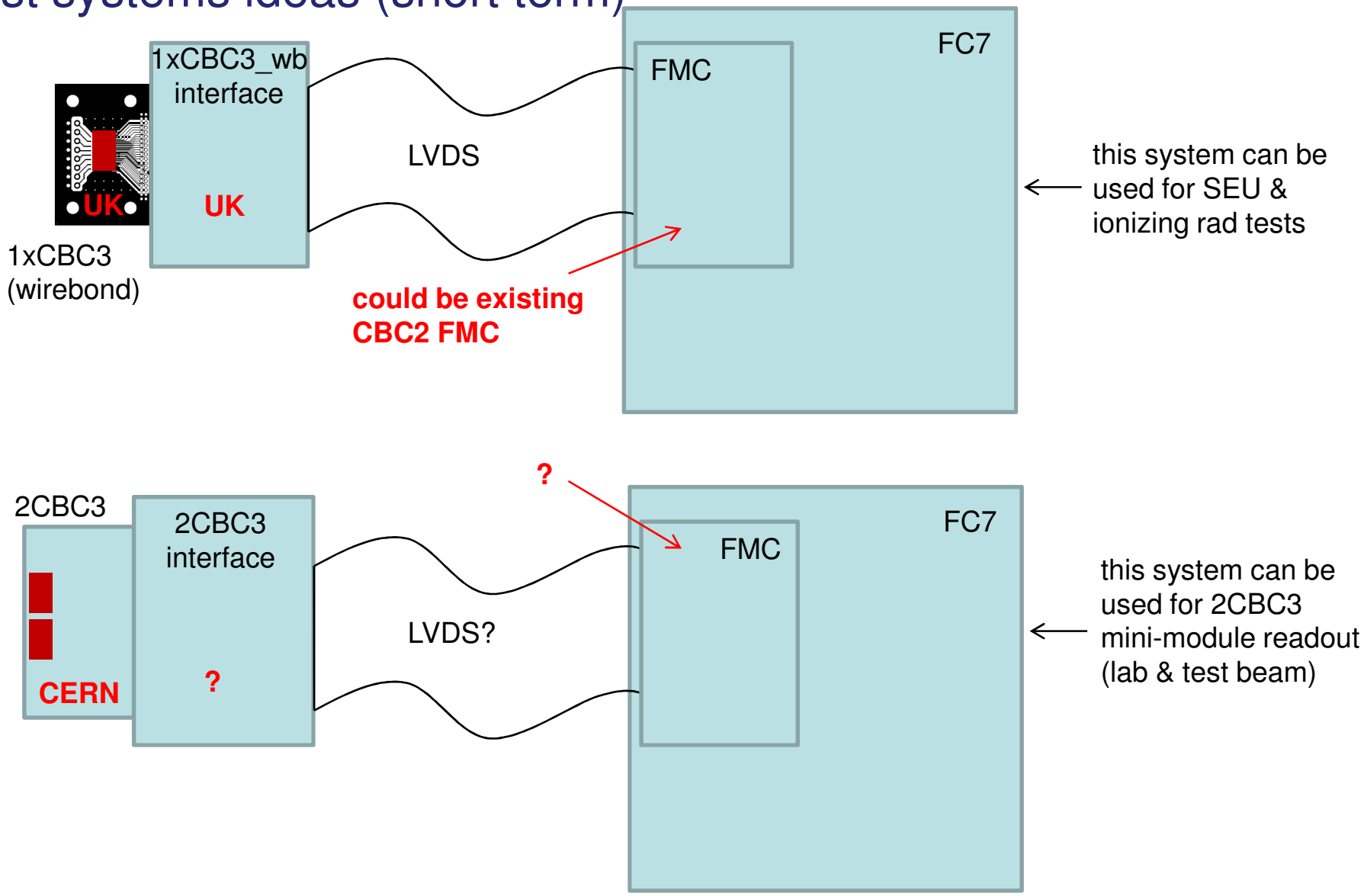
CERN PMOS bandgap reference
also trimmed by e-fuses (6 bits)

for detailed picture, prepared by Lawrence Jones, showing all pads labelled, download:

http://www.hep.ph.ic.ac.uk/~dmray/pictures/CBC3_PADS_Footprint1.png

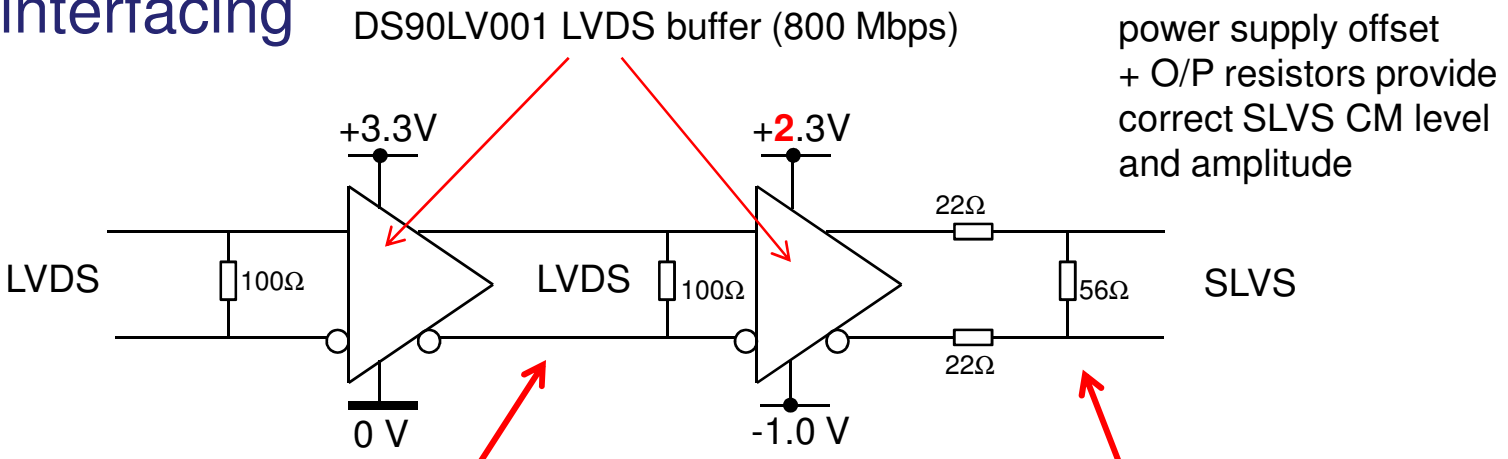
note: downloadable picture shows pads as should be laid out on hybrid surface (flipped version of pads on chip)

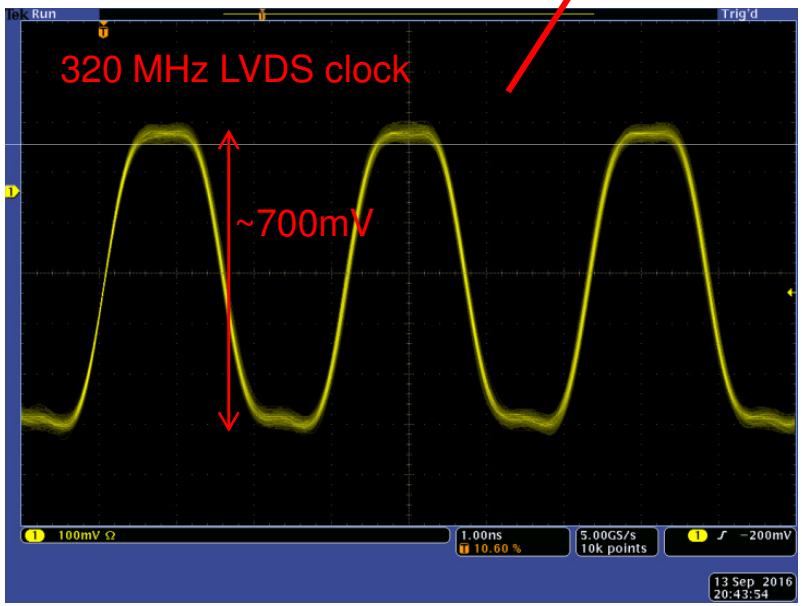
test systems ideas (short term)

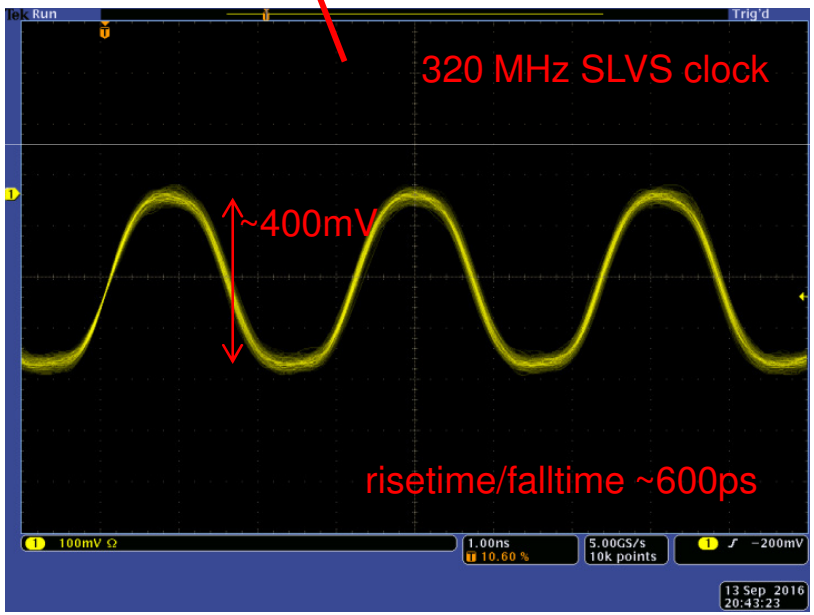


(there will also be a VME DAQ system for early tests, wafer probe, detailed behaviour diagnosis - like for CBC2)

SLVS interfacing



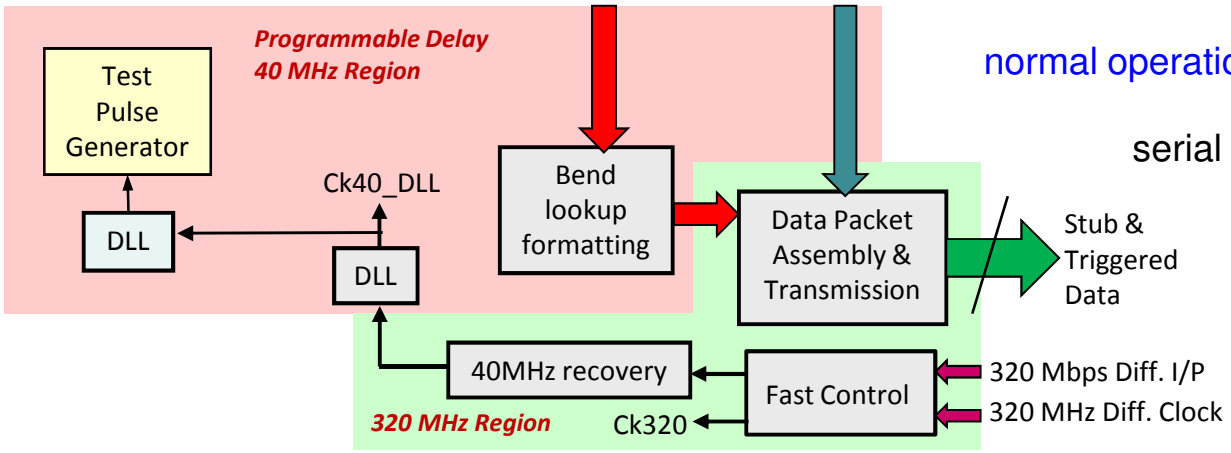




for SLVS -> LVDS just use one DS90LV001 (0 and 3.3V supplies)
CM acceptance range of LV001 can cope with SLVS levels

40 MHz test mode

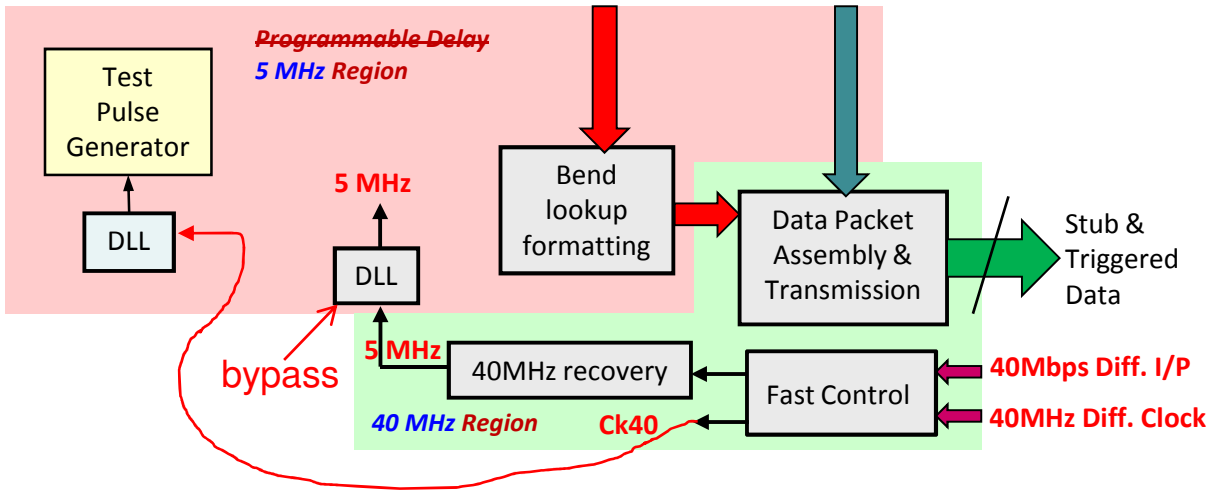
if necessary (e.g. for wafer probing) can run chip at 40 MHz



normal operation

serial command interface (SCI) @ 320 Mbps

320 MHz clock



40 MHz test mode

change 320 -> 40 MHz (Ck40)

run SCI at 40 Mbps

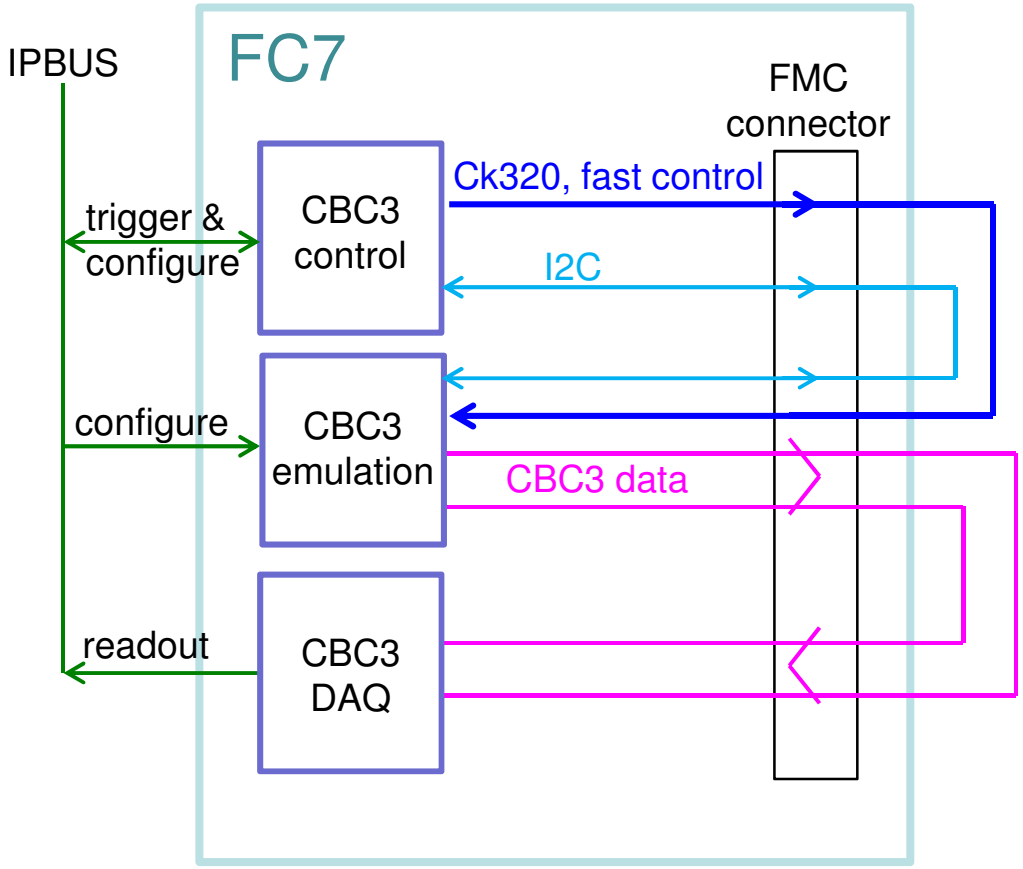
on-chip recovered clock is 5 MHz

bypass 40 MHz DLL
(have to - it will not capture)

feed Test Pulse DLL from Ck40

CBC3 initial test system development: control & DAQ

Kirika Uchida



CBC3 control

generates 320 MHz clock
encodes control signals on fast control line
(fast reset, test pulse trig., L1A, orbit reset)
implements I2C interface

CBC3 emulation

simple emulation for DAQ development
(extend to more accurate emulation in future)

responds to fast control signals
for example
test pulse trigger produces stubs
L1A produces data frame
(data patterns can be configurable)

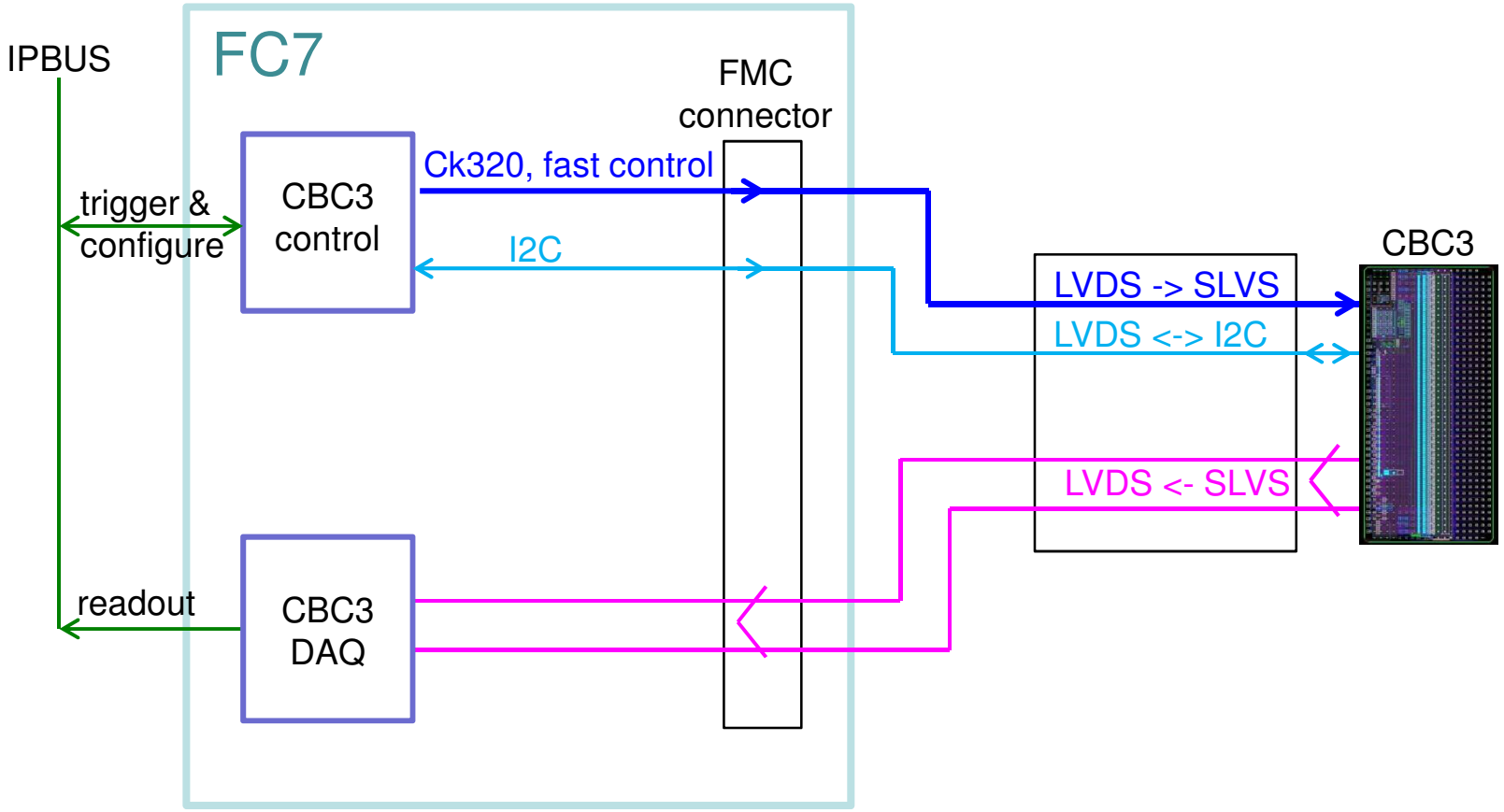
CBC3 DAQ

data timing tuning
capture data, stub & data matching

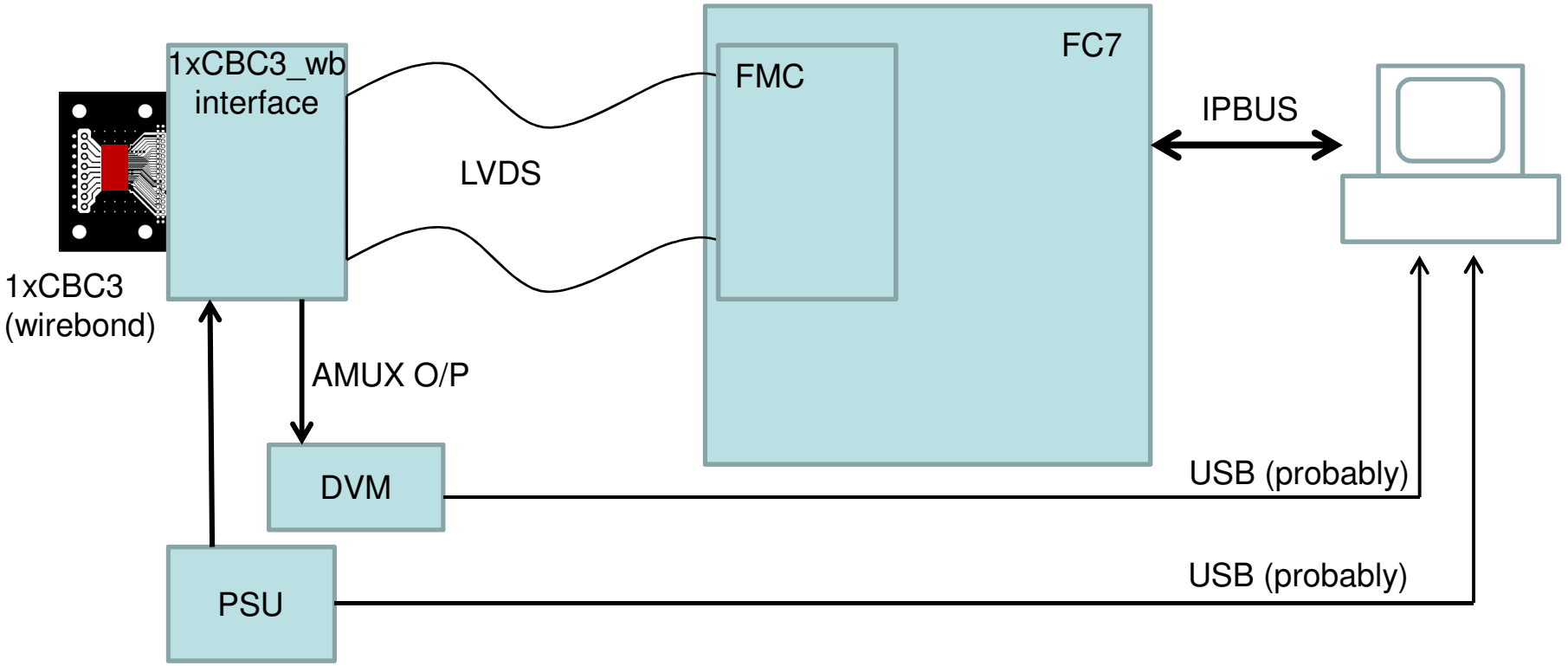
green = done
red = in progress

CBC3 initial test system development: control & DAQ

Kirika Uchida



software - for ionizing and SEU tests (assume UK responsibility)

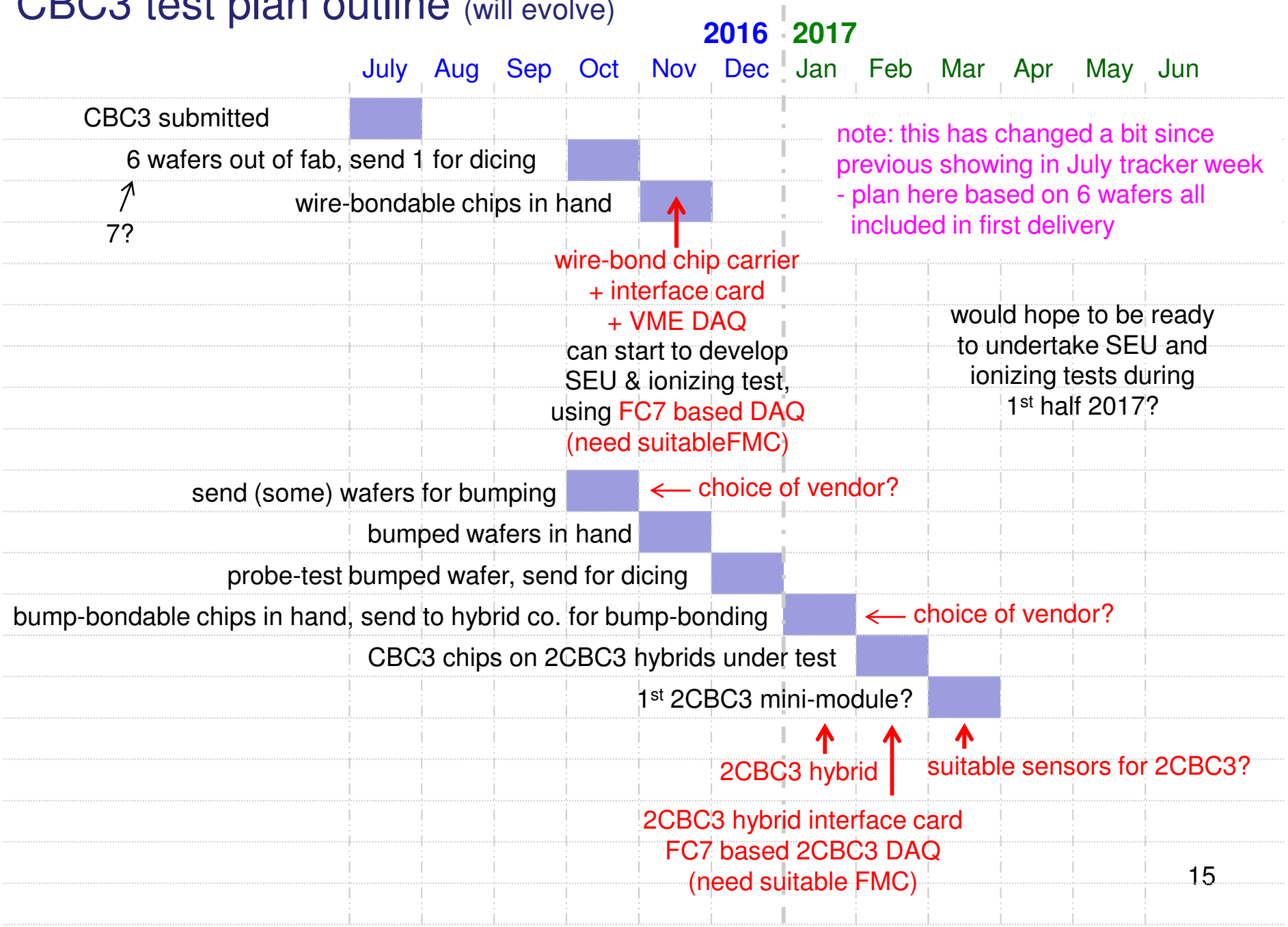


based on CBC2 middle-ware

control and DAQ procedures
PSU current monitoring
AMUX O/P monitoring

} processes need to be synchronized (e.g. monitor PSU current and/or AMUX O/P while sweeping I2C parameter)
data-logging (time-stamping) required for ionizing tests

CBC3 test plan outline (will evolve)



extra

CBC3 digital interfaces

output data: up to 3 stubs data transmitted to CIC/BX
6 SLVS diff pairs @ 320 Mbps

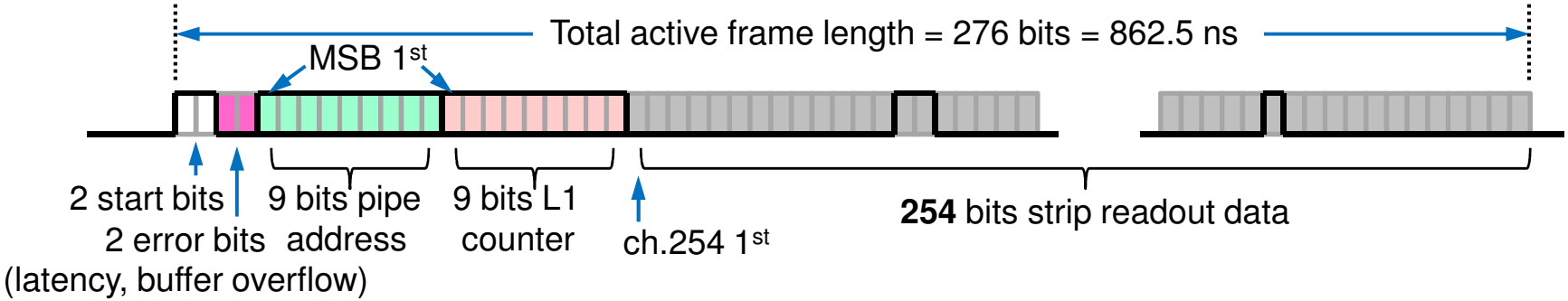
25 ns

S1<7>	S2<7>	S3<7>	B2<3>	**Sync**	**R**
S1<6>	S2<6>	S3<6>	B2<2>	Error	**R**
S1<5>	S2<5>	S3<5>	B2<1>	OR254	**R**
S1<4>	S2<4>	S3<4>	B2<0>	SoF	**R**
S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	**R**
S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	**R**
S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	**R**
S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	**R**

R = L1 triggered readout data
time flow **top** to **bottom** (e.g. S1<7> output first)

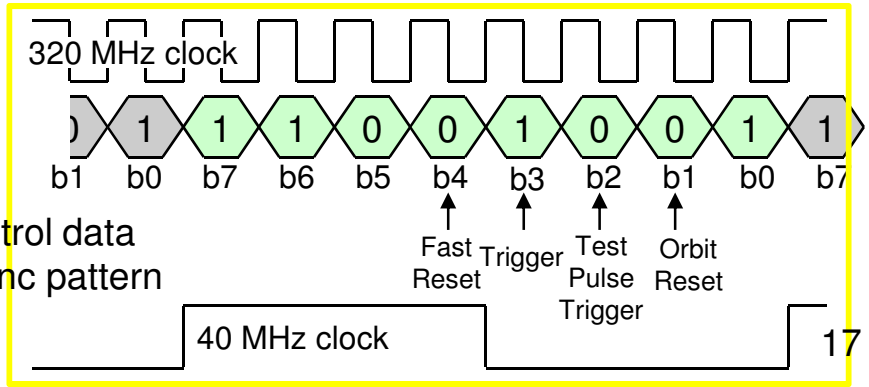
readout data

readout data frame length 950 nsec
=> up to 1 MHz L1 triggering capability



fast control

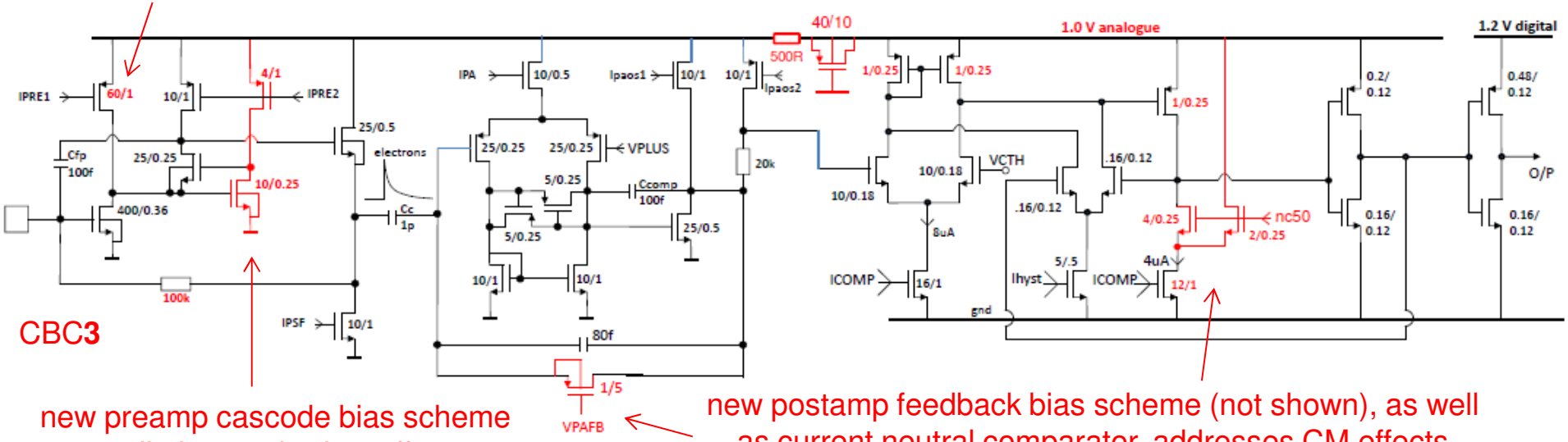
320 MHz clock
320 Mbps fast control line



40 MHz generated from fixed sync pattern in fast control data
normal command structure can't be confused with sync pattern

CBC2 vs. CBC3

increase in bias FET
allows higher currents

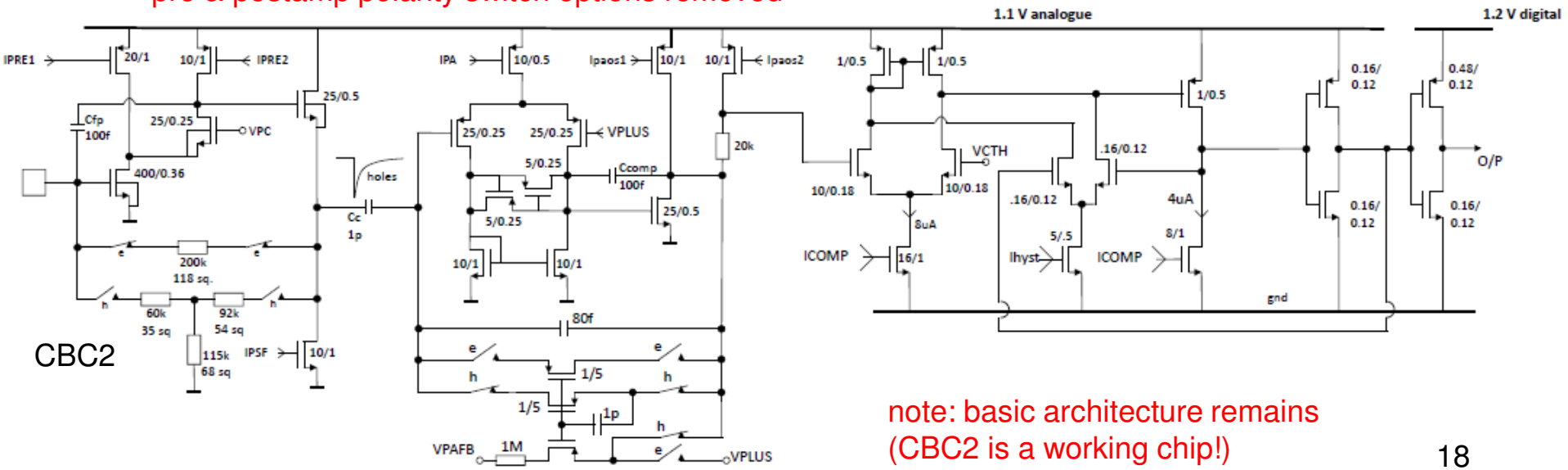


CBC3

new preamp cascode bias scheme
to eliminate “shadow effect”

new postamp feedback bias scheme (not shown), as well as current neutral comparator, addresses CM effects observed when many channels fire

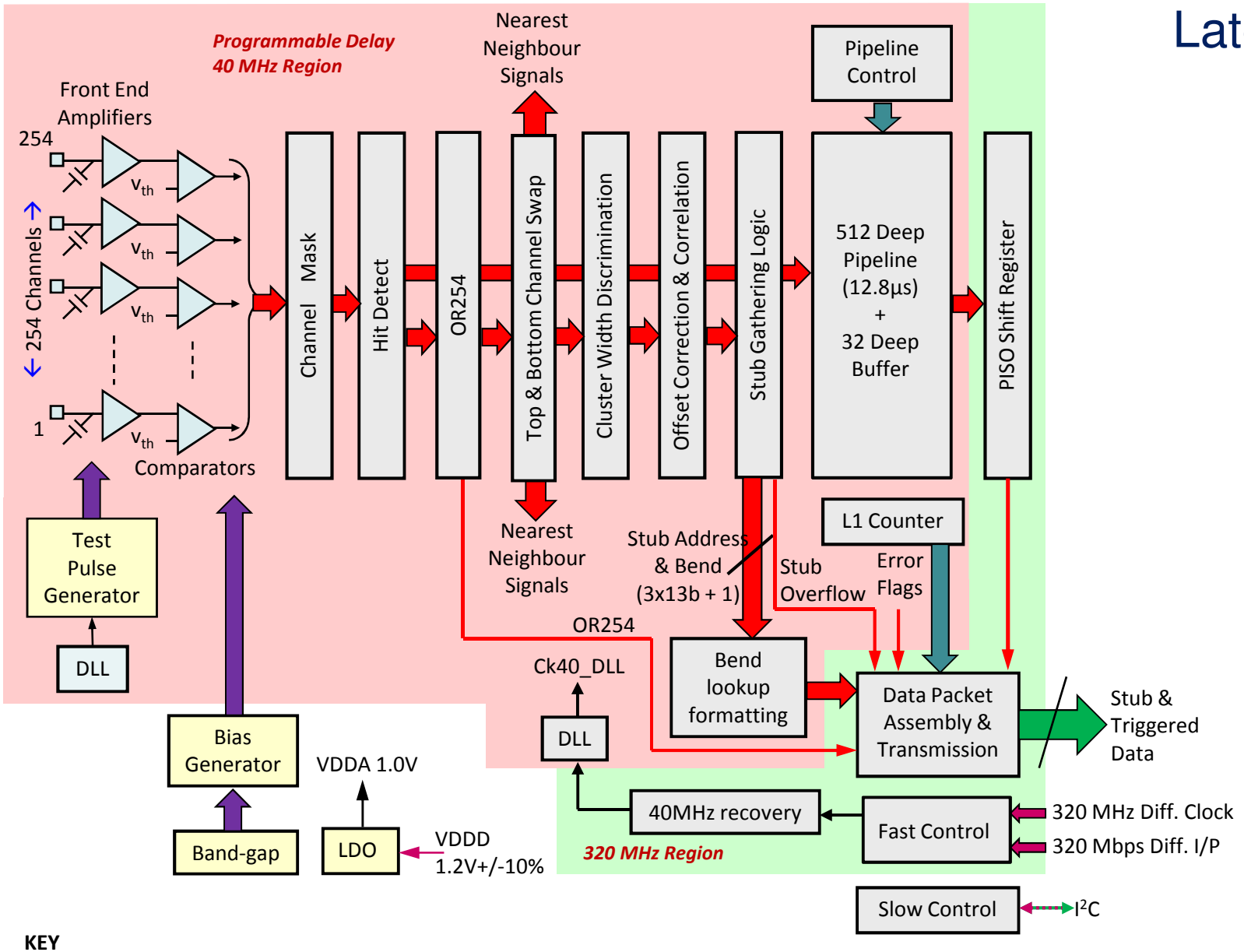
pre & postamp polarity switch options removed



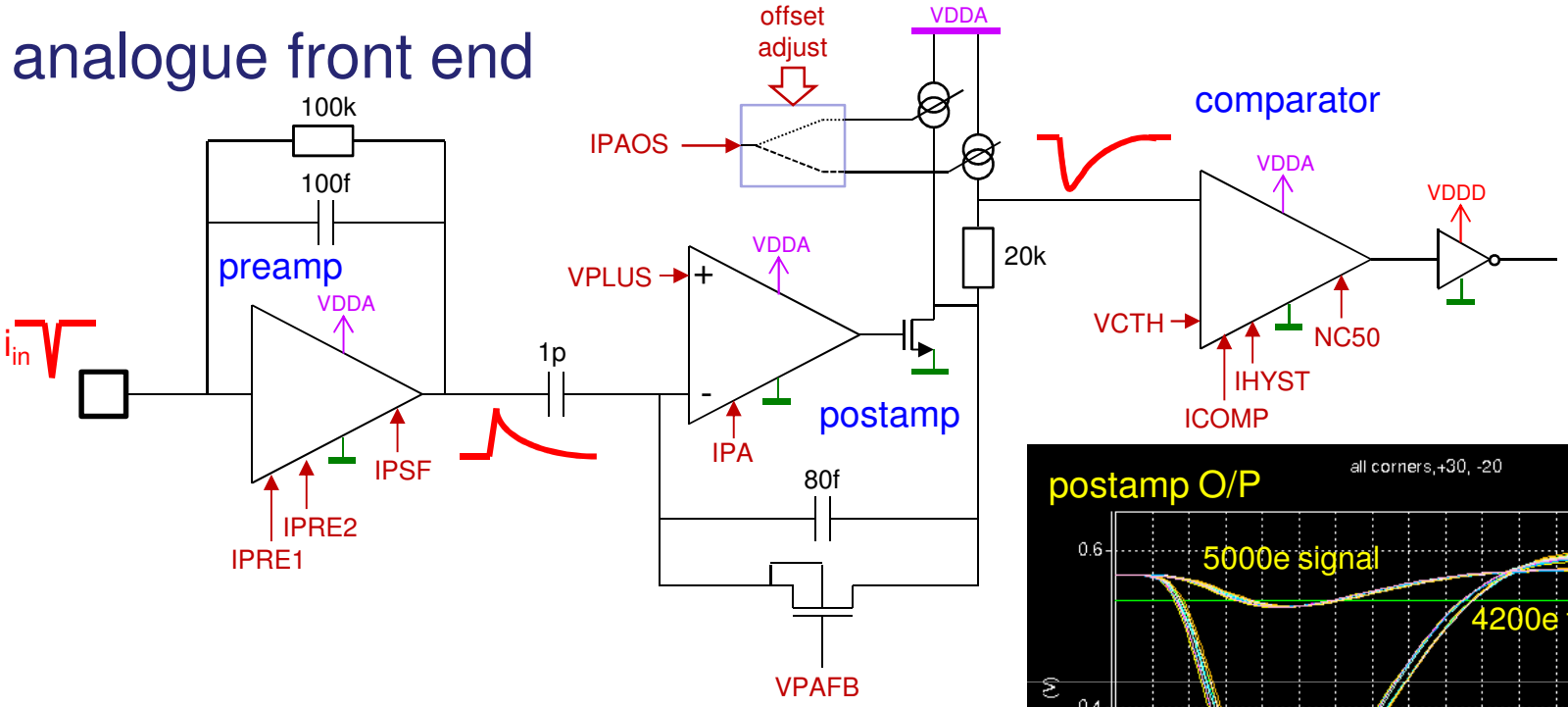
CBC2

note: basic architecture remains
(CBC2 is a working chip!)

Latest Block Diagram



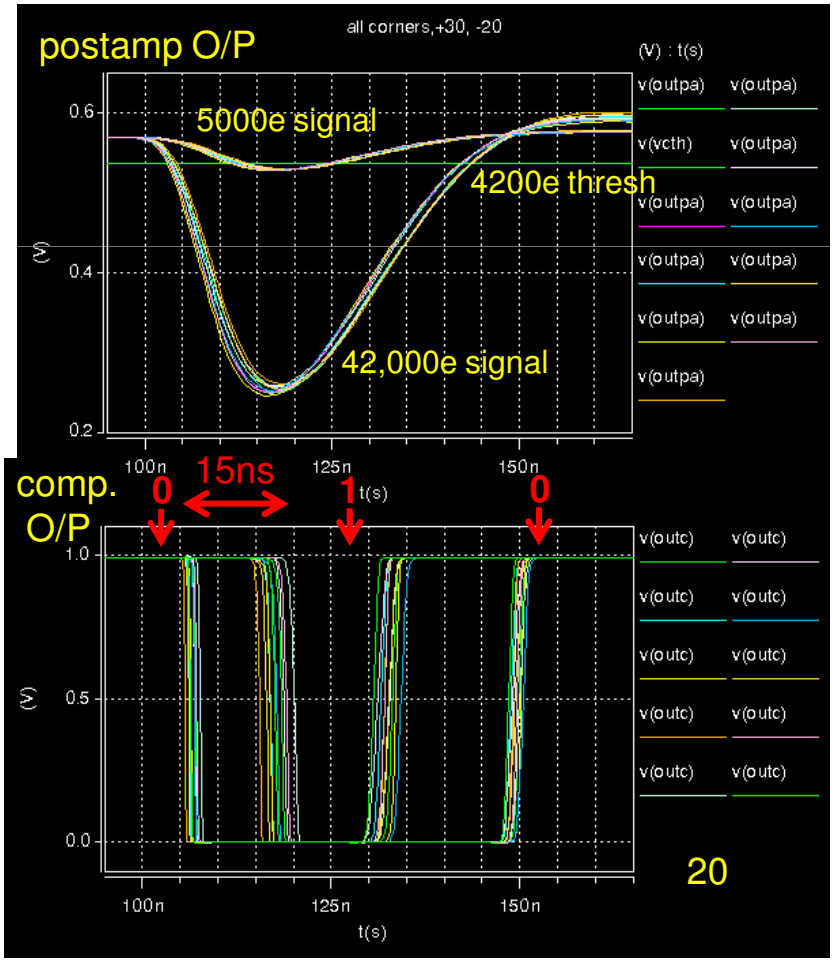
analogue front end



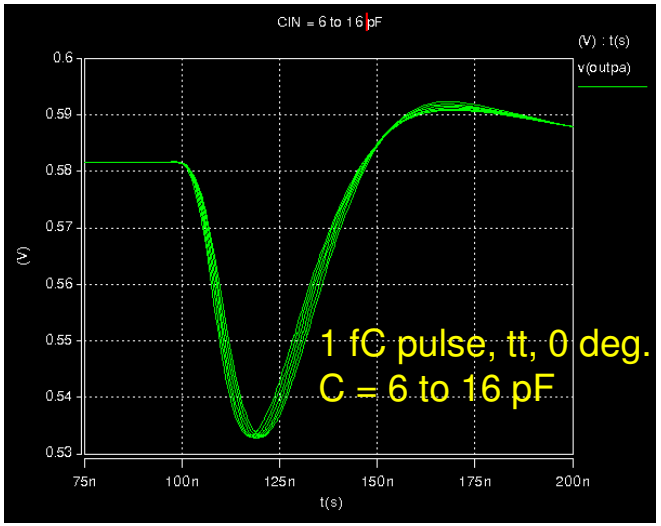
main design changes

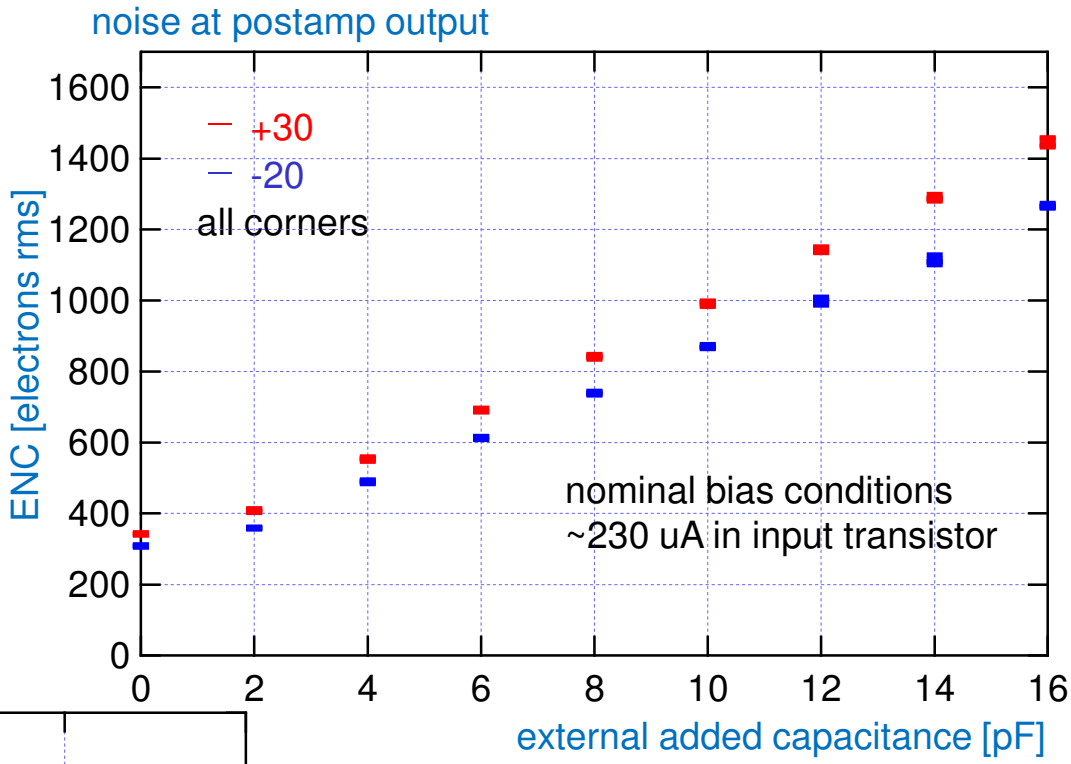
optimised for n-in-p sensors
faster shaping (return to baseline within 50 ns)
VCTH linear, monotonic and 10-bit
CBC2 “shadow” and CM effects addressed

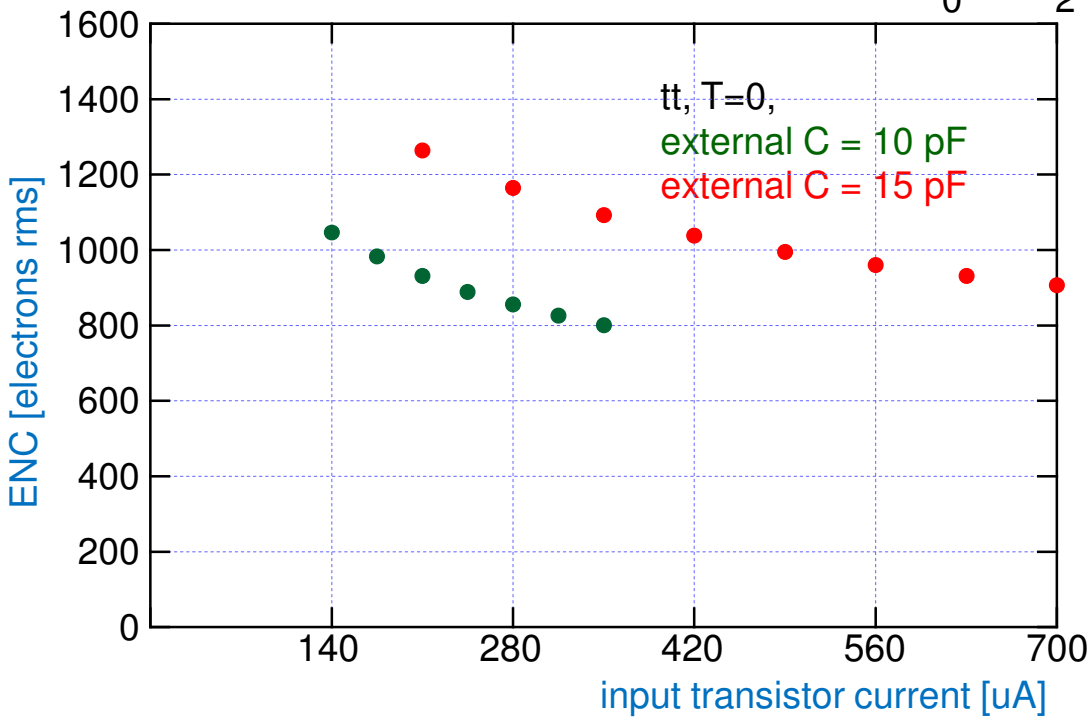
post-layout
timewalk
simulation



noise







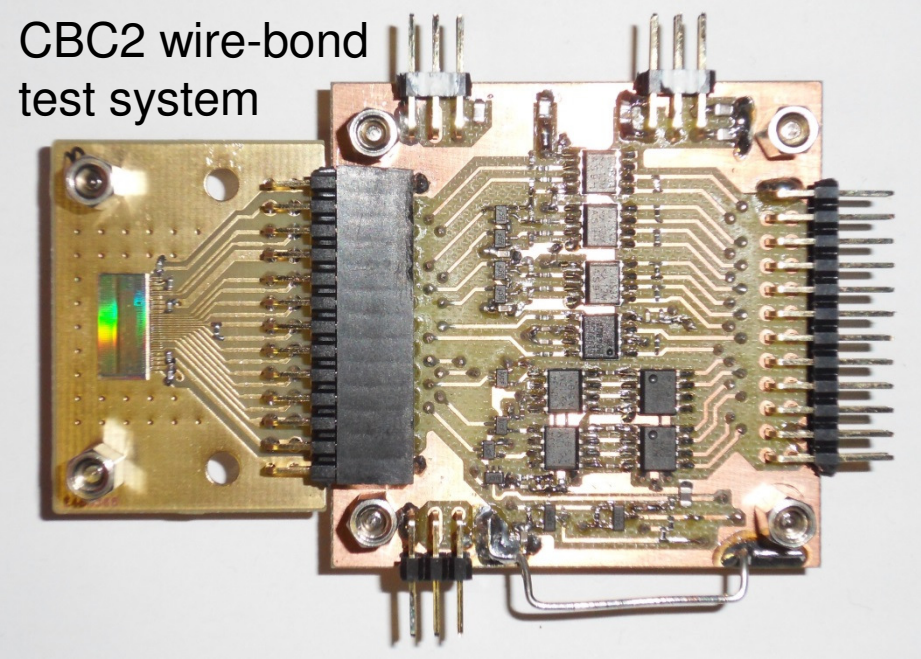
post-layout simulations

1000e achievable for external capacitance up to ~10 pF at preamp input (for acceptable power consumption)

no strong dependence on process corners

pulse shape/height varies not much over quite large input capacitance range

1st tests



1st diced chips will be wire-bondable

can follow similar test procedures to CBC2

make single chip carrier + interface board

useful for:

- developing wafer probe tests
- ionizing tests
- SEU tests

need to adapt/develop DAQ hardware/firmware/software to deal with 6 x 320 Mbps data streams