CBC Production QA

what we did for the APV25

what we can/should do for the CBC

- what can be tested at wafer level
- what should be confirmed after hybrid/module assembly

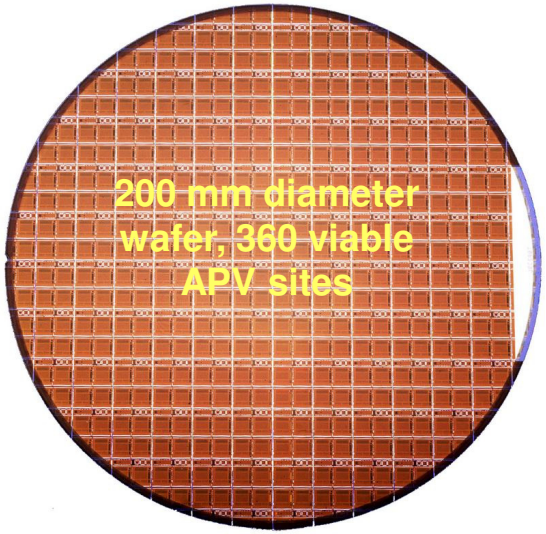
systems test meeting, 3rd March, 2016.

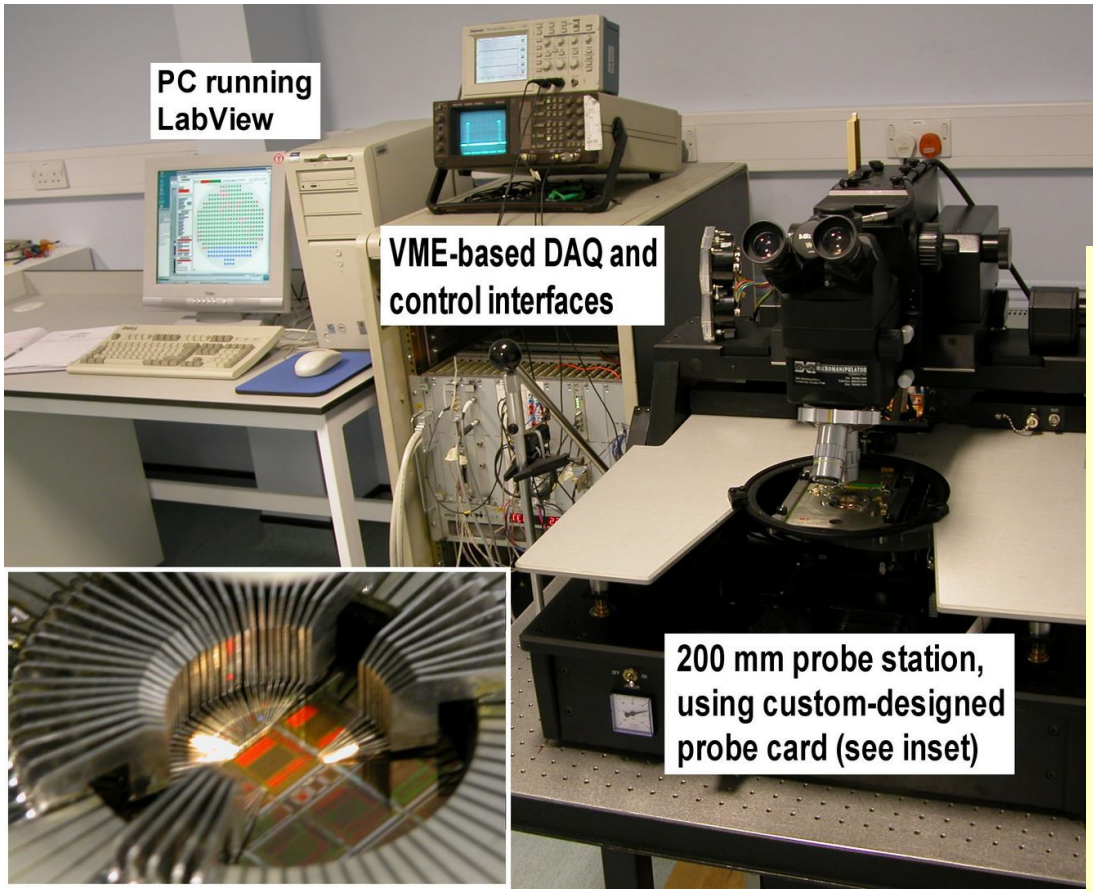
APV25 wafer testing

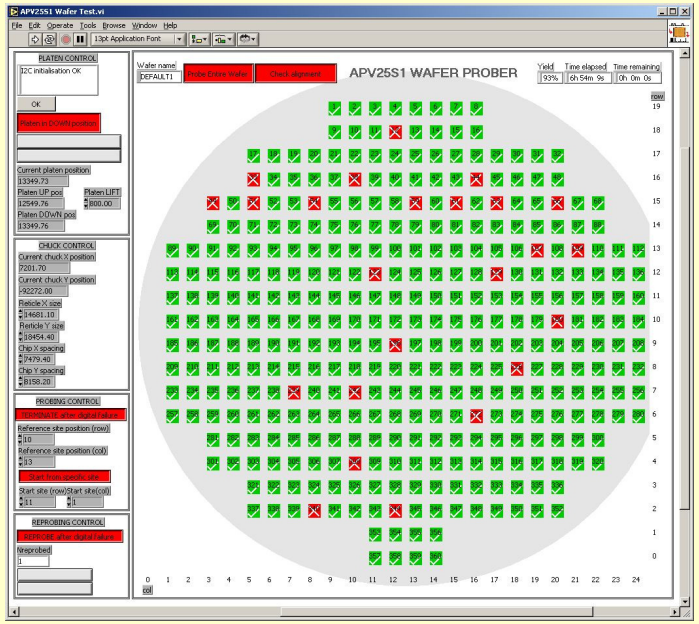
~ 600 wafers (~ 216,000 chips) tested over ~ 4 years

individual chips subjected to detailed testing of analogue/digital functionality -> Known Good Die (KGD)

wafer maps generated for subsequent dicing and picking by hybrid manufacturer







APV25 wafer test software

LabView based, aim for comprehensive fault coverage

digital: chip addressing, stuck bits, pipeline control logic, …..

analogue: supply currents, all channels pulse shapes, all pipeline locations OK, noise, ……

green lights => all tests passed

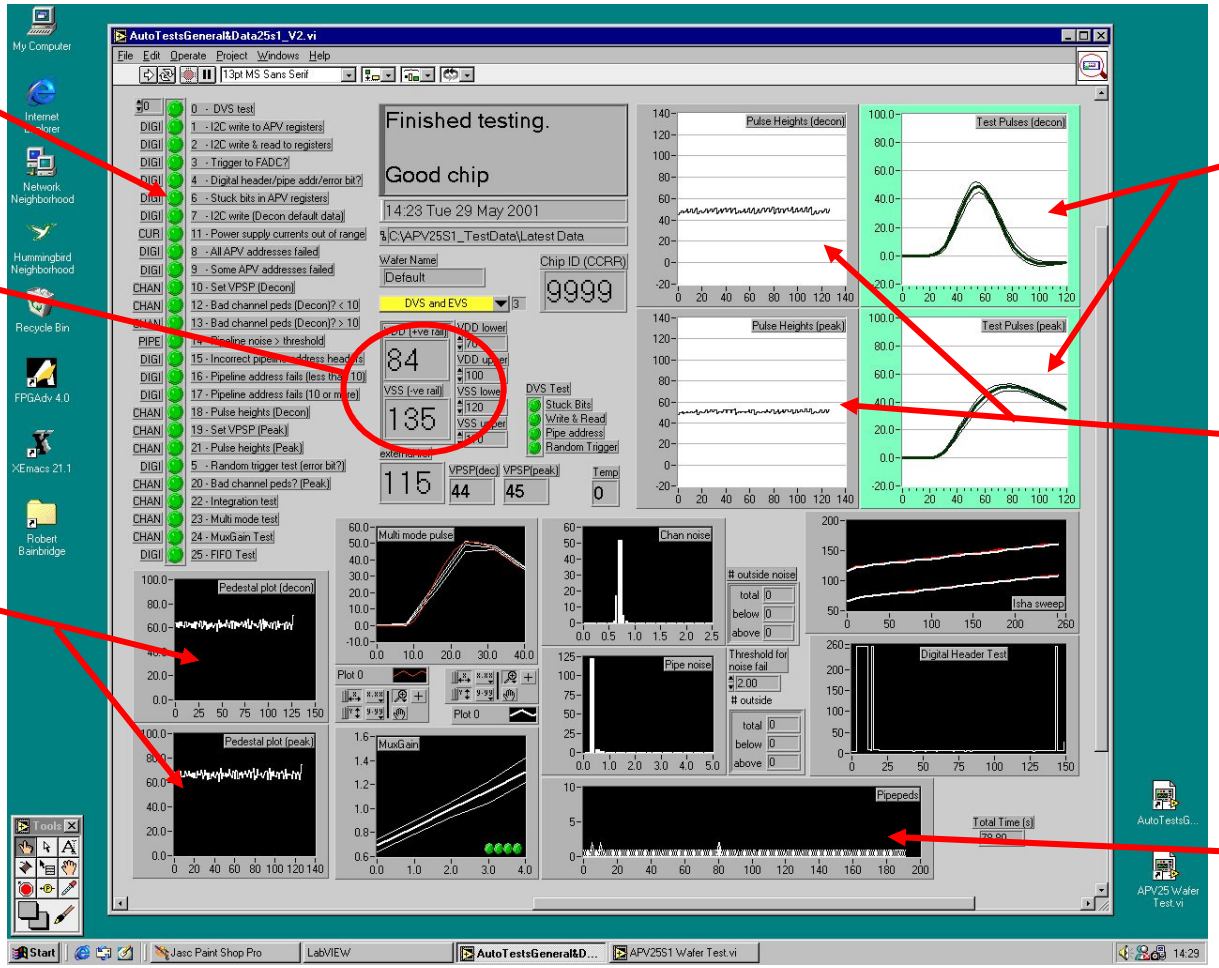
power supply currents

channel pedestals

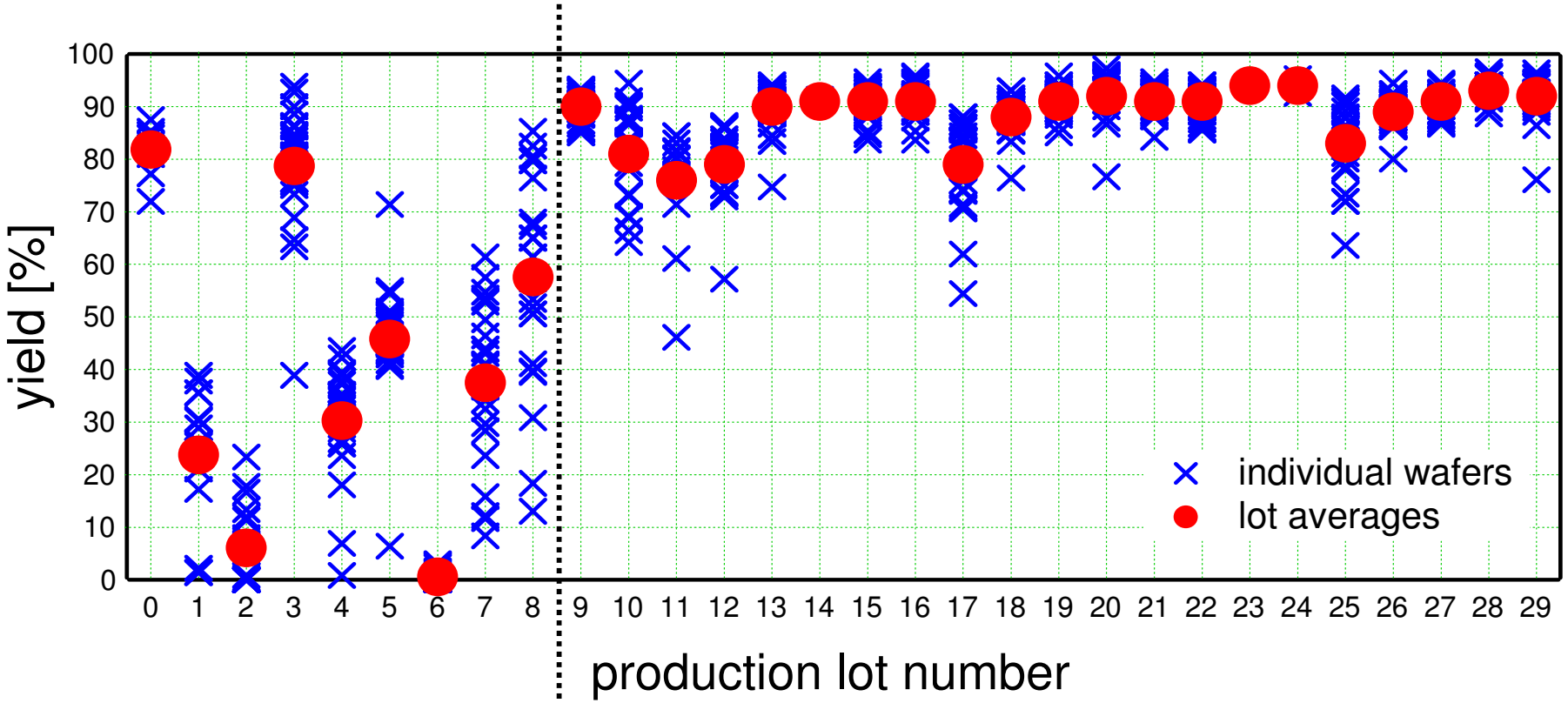
calibration pulse shapes

calibration gain

pipeline pedestals (128 x 192)



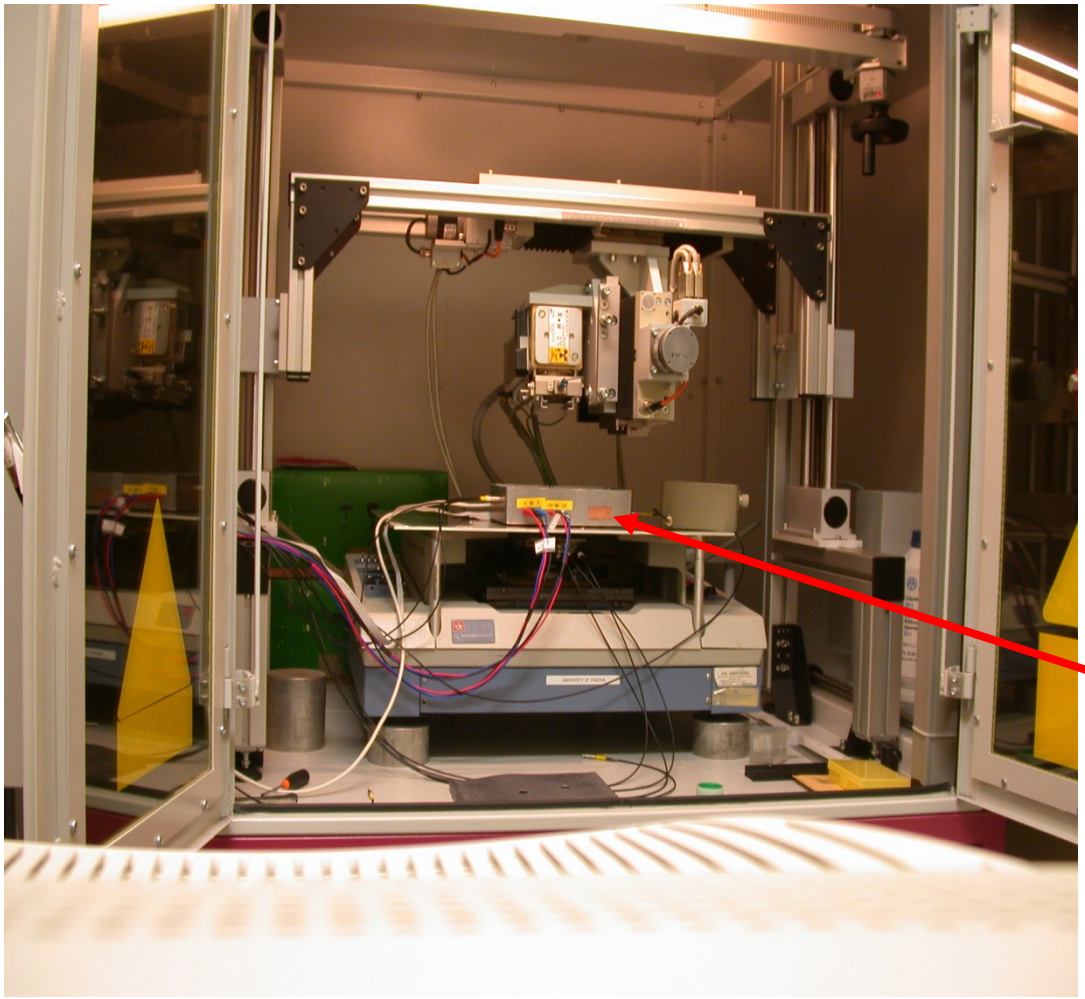
APV25 wafer yield



early lots showed variable yield – metallization problem diagnosed and manufacturing process tweaked
(see P.Barrillon et al, Proceedings of the 10th workshop on electronics for LHC experiments, CERN-LHCC-2004-030, 148-152.)

88.5 % average yield since lot 9
- 414 wafers
- 131,734 pass chips (Known Good Die – KGD)

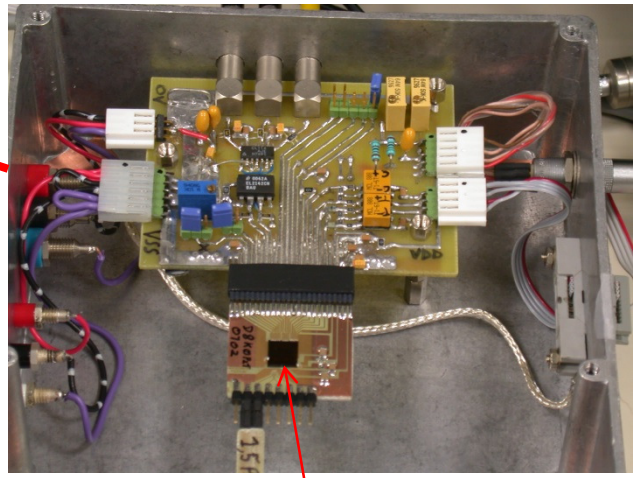
APV25 production QA (IC and Padova)



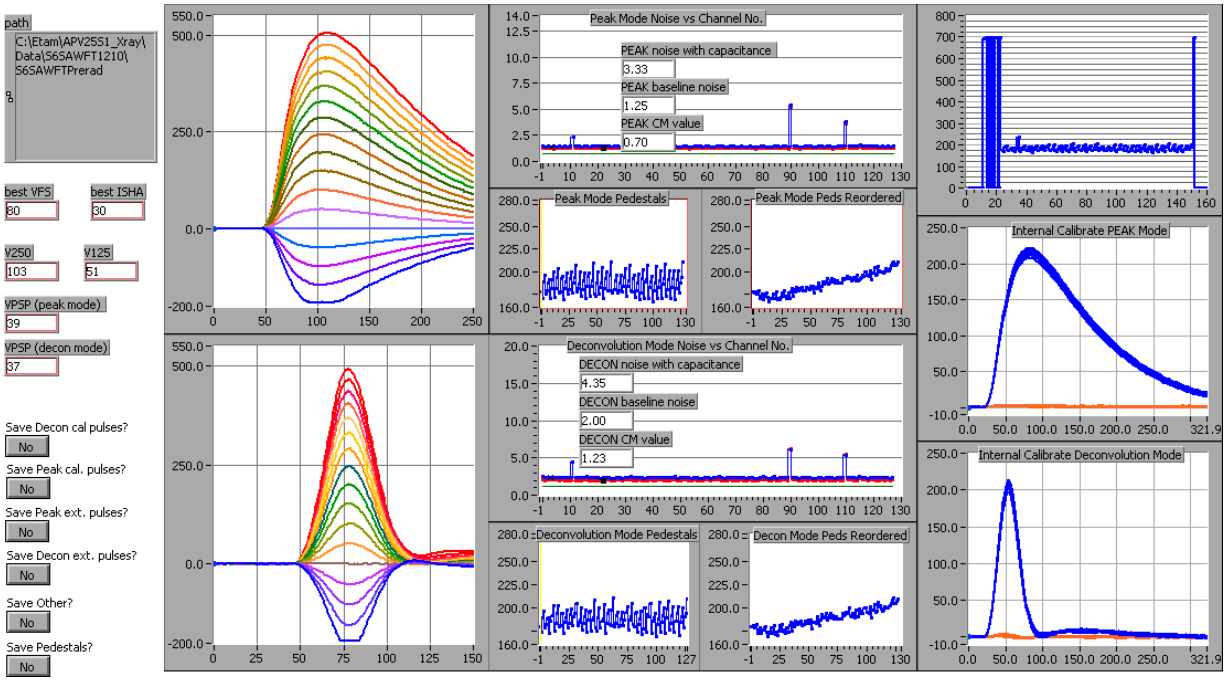
perform more detailed tests (incl. irradiation) on chips already passed wafer test

1 chip/wafer -> more detailed electrical tests

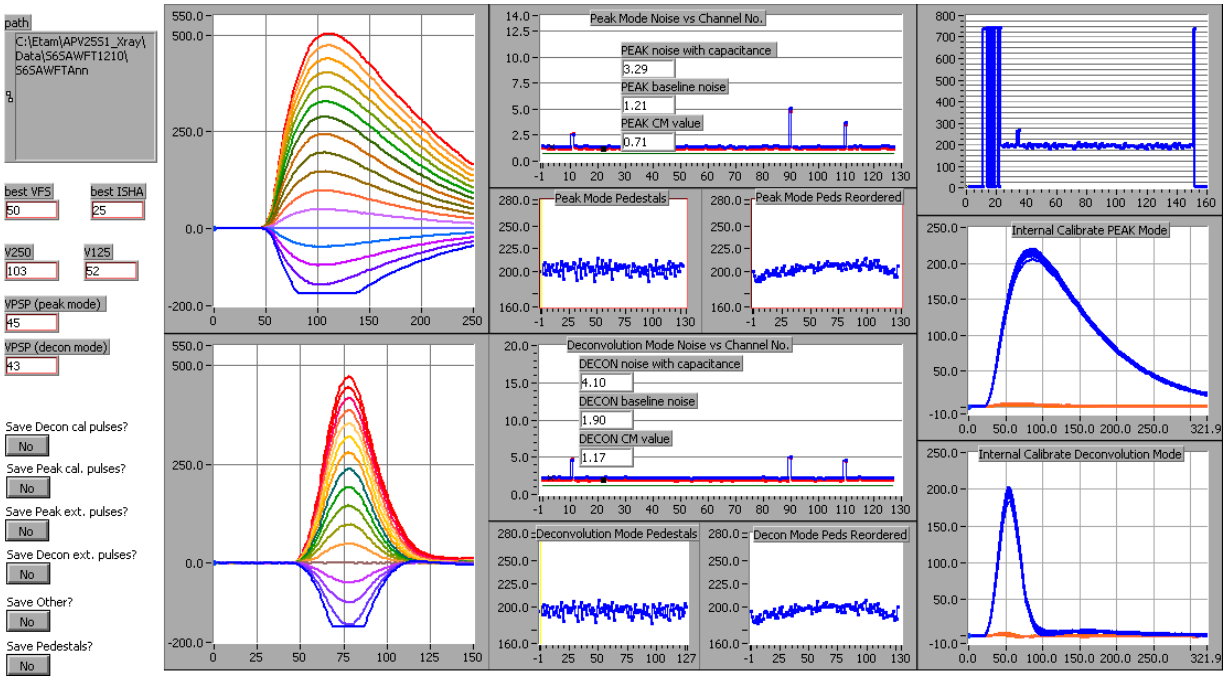
subset (5 chips / wafer lot) irradiated and re-measured



production QA measurements



Pre-rad



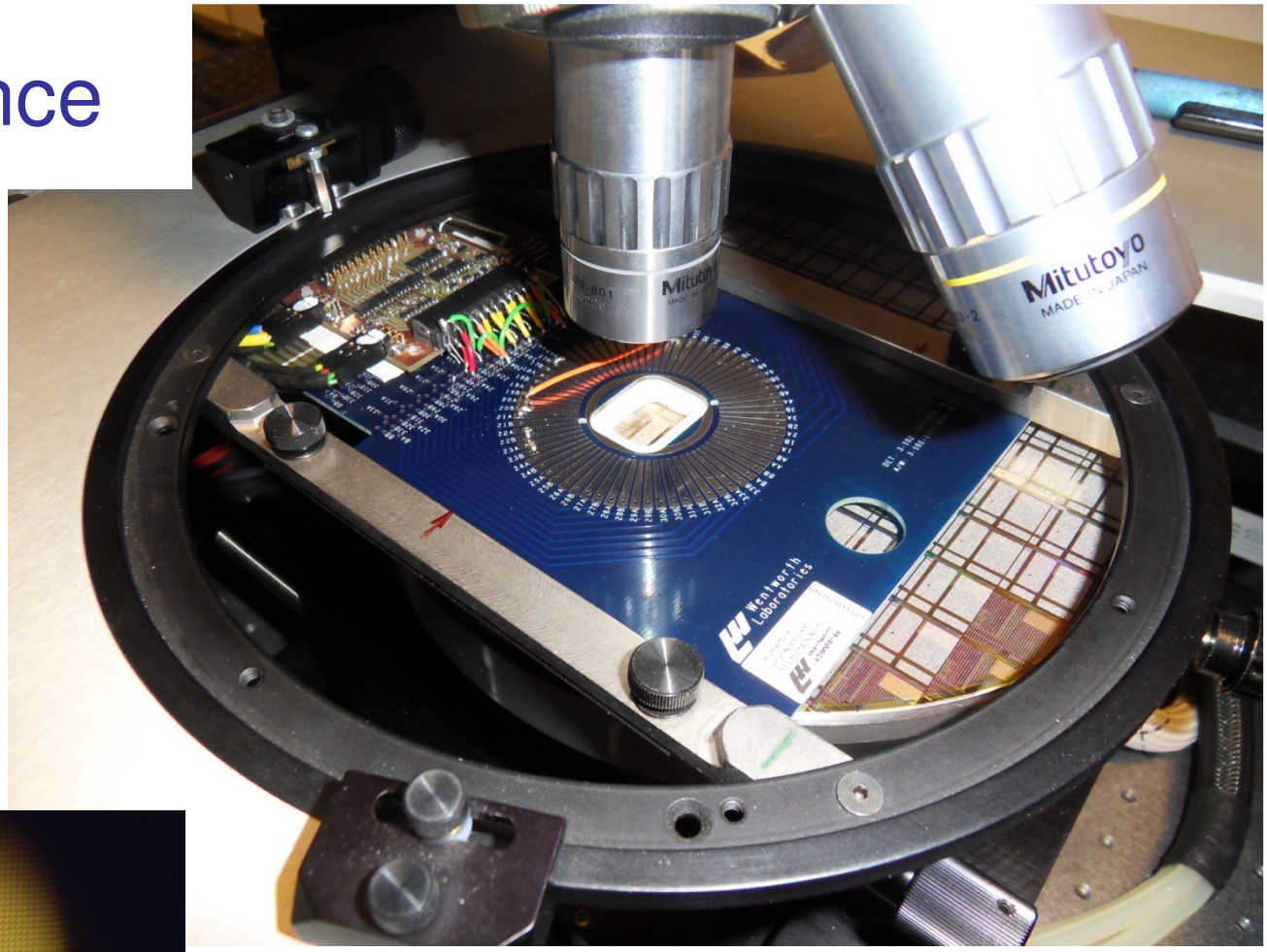
After 10 Mrads + anneal

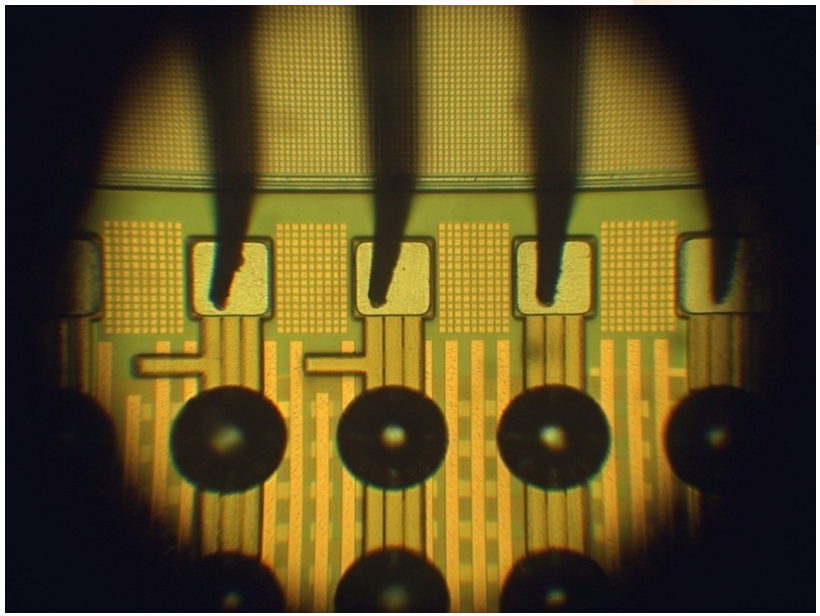
For details of study and results, see:
Production testing and quality assurance of CMS silicon microstrip tracker readout chips
Bainbridge et al, NIM A543, Issue 2-3, 619-644

CBC2 experience

8 wafers produced (4 probed)

yield is high (> 94%)





set of wire-bond pads left for probing

LabView front panel for individual CBC2 chip test

test protocol not final but includes:

- exhaustive digital test (I2C, pipeline)
- s-curves: pedestal and with test pulse
- bias generator via analogue mux
- power consumption

some differences for CBC3

320 MHz operation

output data 6 lines @ 320 Mbps
a lot more data for test DAQ to swallow

single fast control line @ 320 Mbps

plan to run in special 40 MHz test mode for wafer test

e-fuses

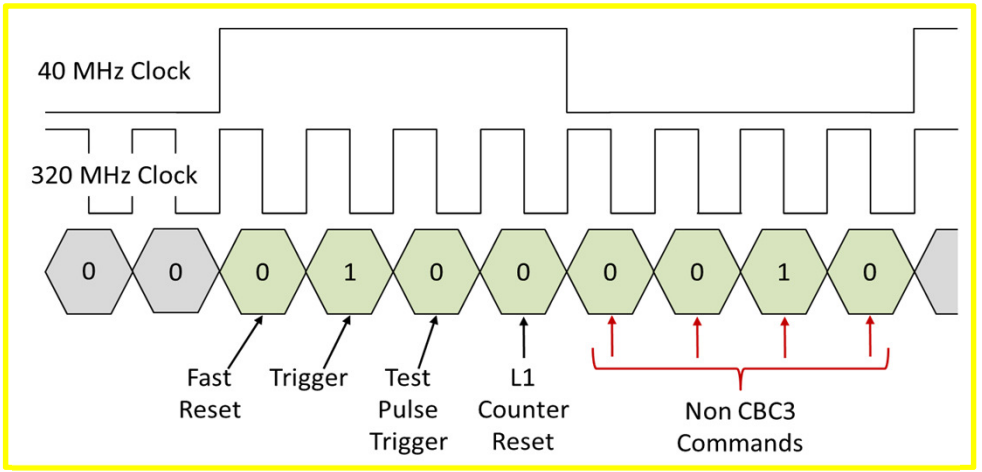
bandgap trimming and unique chip ID
will be programmed during wafer test

output data

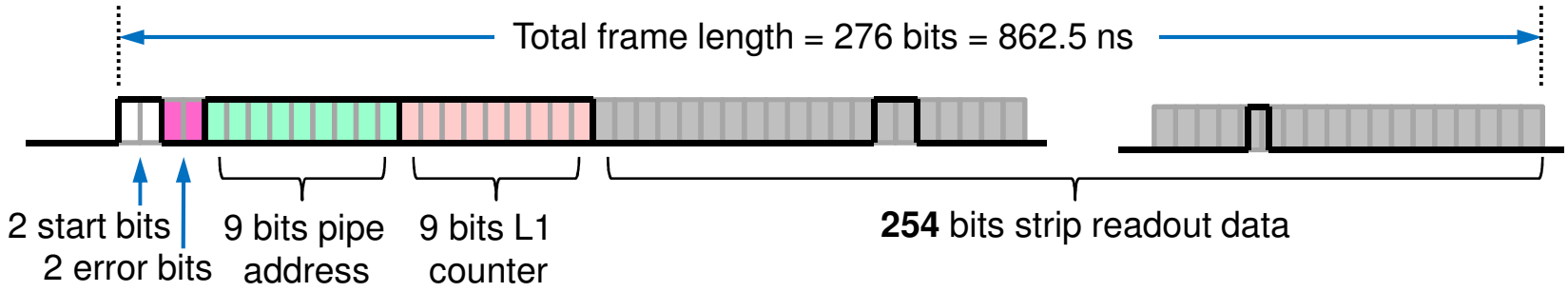
25 ns

S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B1	B3	**R**
S1	S2	S3	B2	SoF	**R**
S1	S2	S3	B2	OR254	**R**
S1	S2	S3	B2	Error	**R**
S1	S2	S3	B2	**Sync**	**R**

(R = L1 triggered readout data)



Readout data frame



CBC production & QA

wafer test

can expect to achieve ~100% coverage of digital logic operation and interconnectivity
no stuck bits anywhere (I2C registers or pipeline/FIFO/buffer RAM/…)

verify performance of all channels using test pulse (TP amplitude accuracy +/-18%)

chip ID and bandgap programming

power consumption and bias generator measurements (analogue mux)

will include DVS and EVS steps (overvoltage stress) to exclude weak chips
can be used as a substitute for burn-in

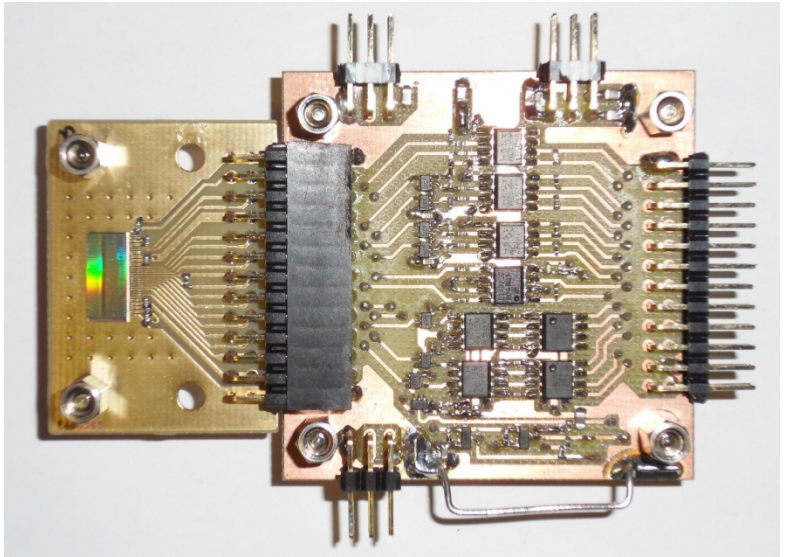
QA

can think about sampling chips from production wafers and subjecting to further tests

could mount face up on test pcbs and irradiate? ⟶

can't get access to input pads without bump-bonding

need to decide what is necessary



CBC production & QA

subsequent tests (on bare hybrid)

important thing to verify successful bump-bonding

antenna test for inputs

on-chip test pulse will find shorts

first time CBCs can be run at 320 MHz

could repeat all chip tests run at wafer probe time
(except analogue mux related)

extra

for reference