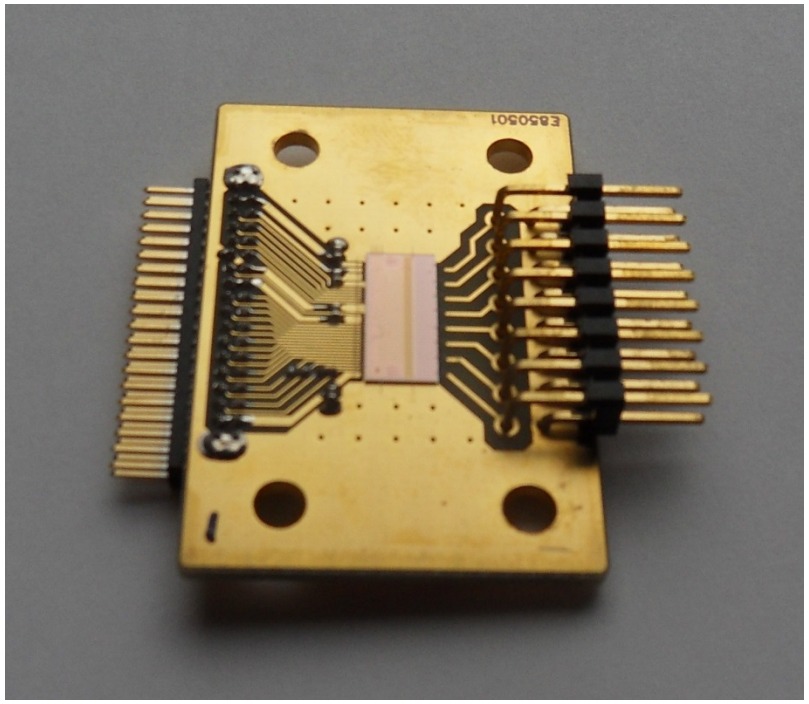
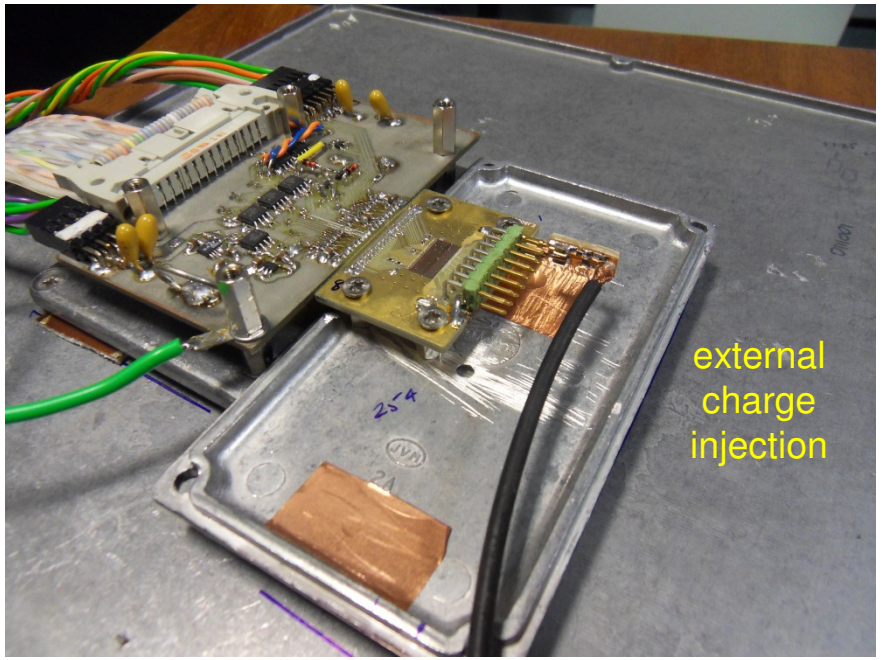
CBC3 single chip studies

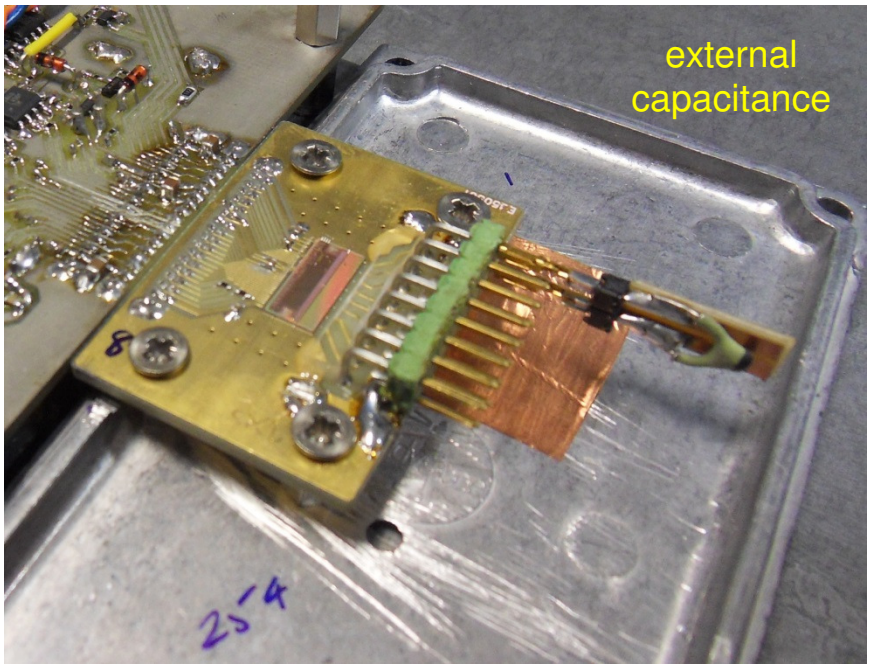
gain, pulse shape & noise
hips response

systems meeting, 6th July, 2017

single-chip test setup







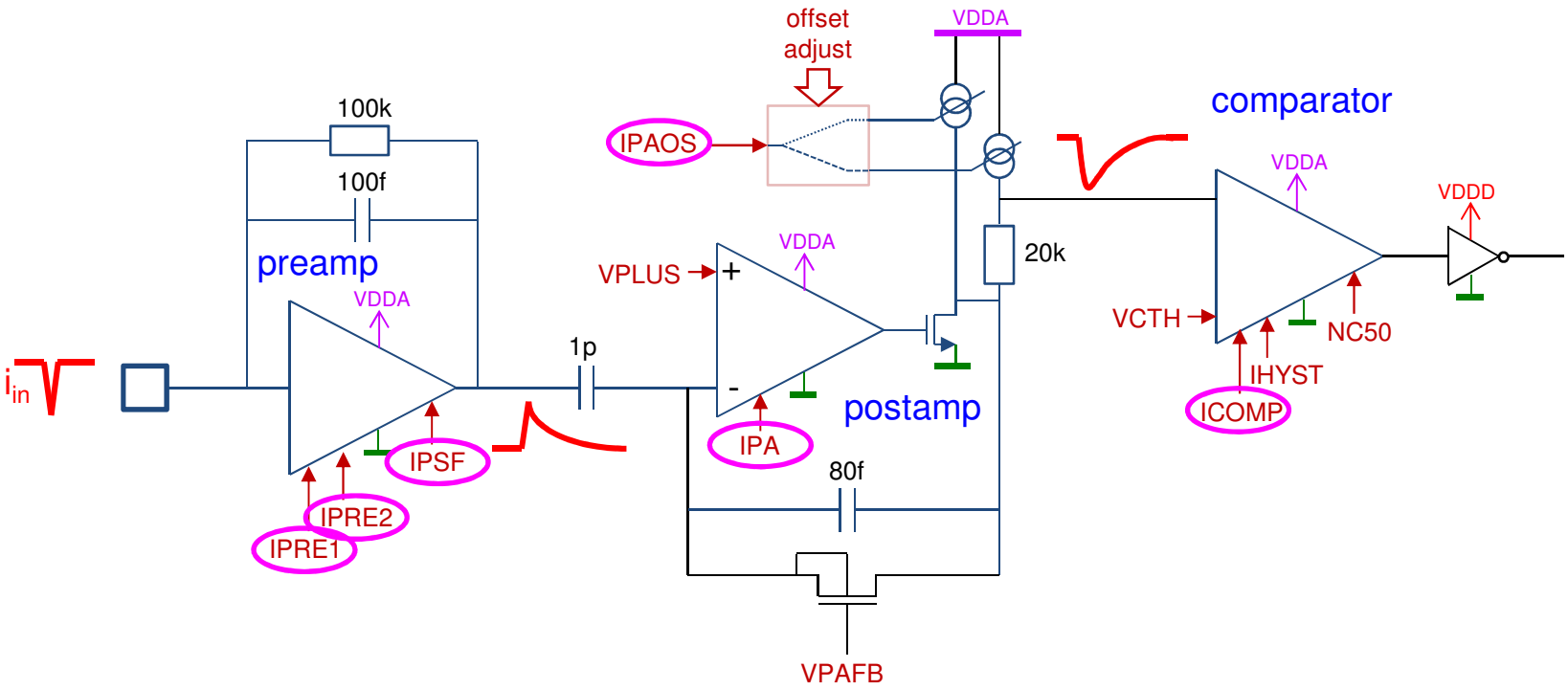
single chip test board has provision to bond 8 inputs

CBC3 bump-bond pads have wire-bondable finish
(unlike CBC2)

can use to inject external (known) charge

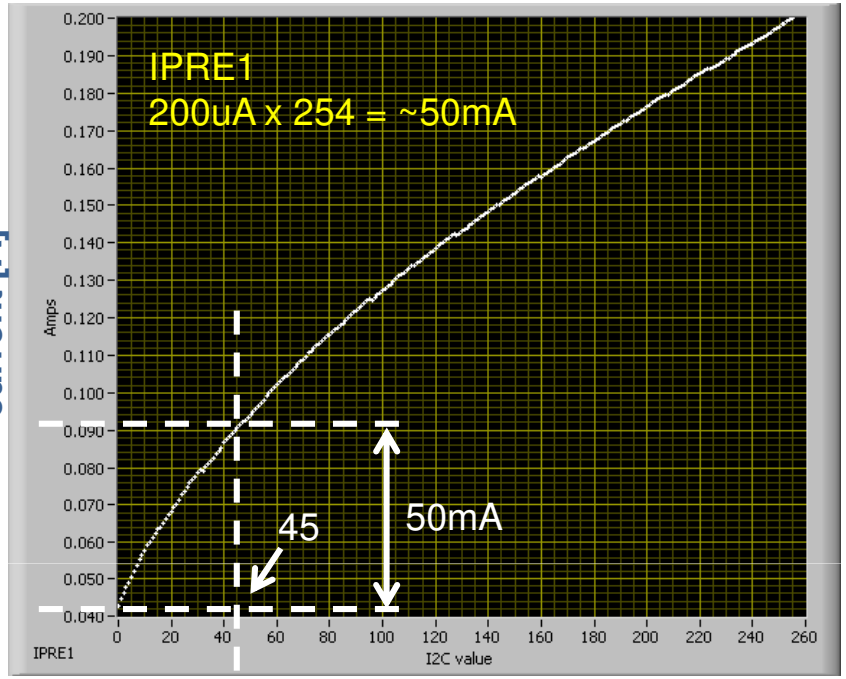
can add external capacitance and measure pulse shape
using internal test pulse

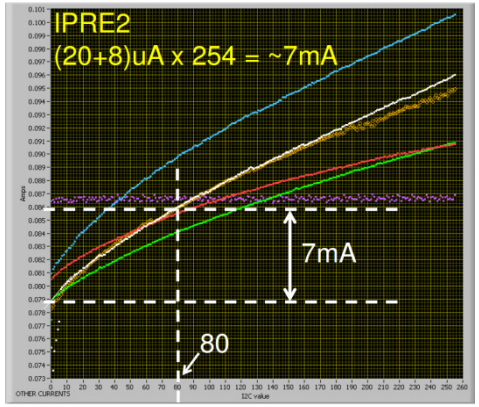
CBC3 front end

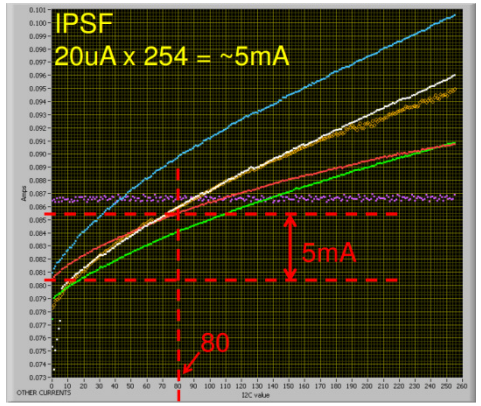


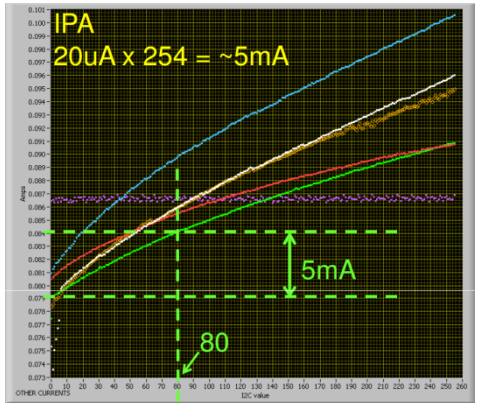
(for reference - choice of circled bias currents explained on next slide)

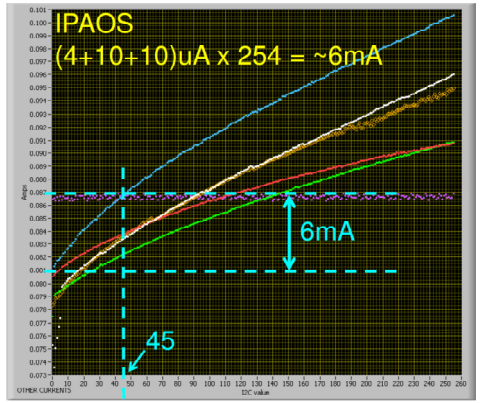
front end bias choices

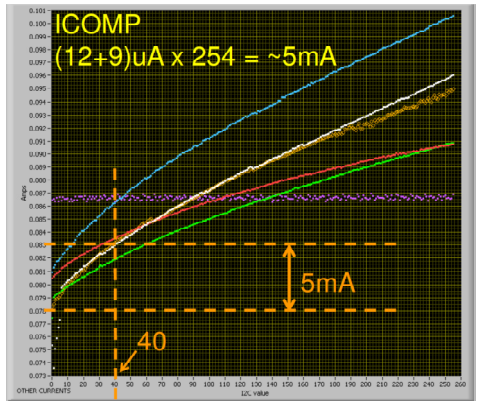










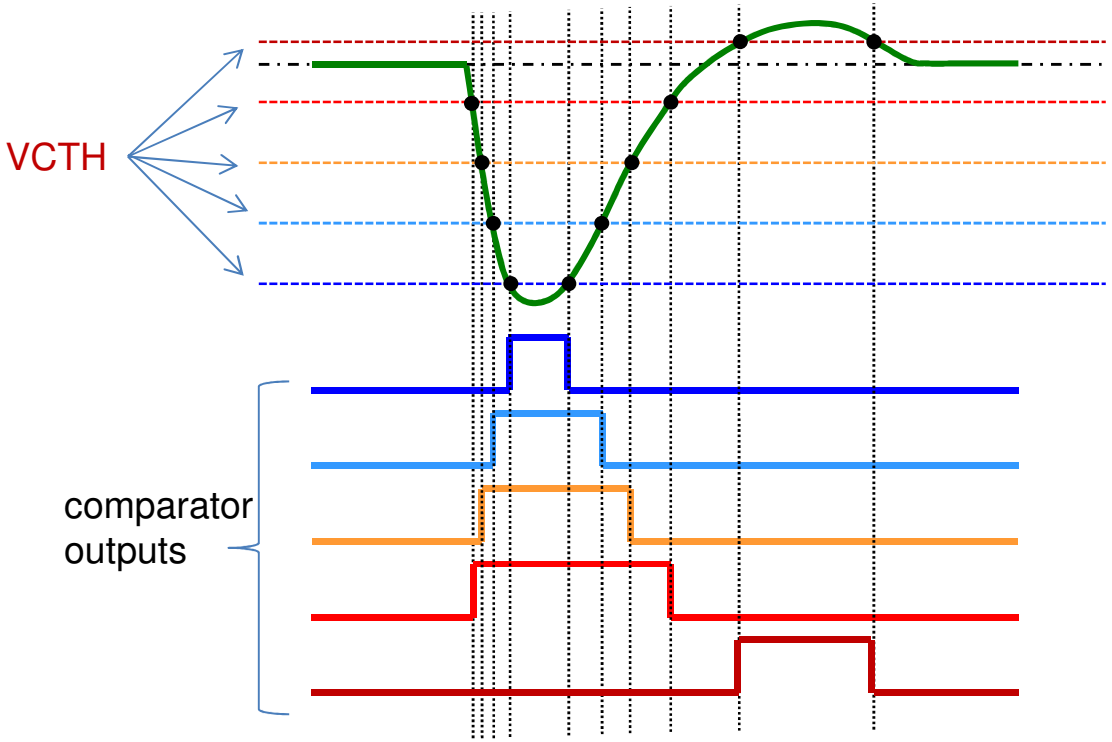


	I/chan [uA]	I/chip [mA]	I2C
IPRE1	200	50	45
IPRE2	28	7	80
IPSF	20	5	80
IPA	20	5	80
IPAOS	24	6	45
ICOMP	21	5	40
		~80 mA	

biases chosen from measurements to be equivalent to those used for simulation

analogue current ~80 mA

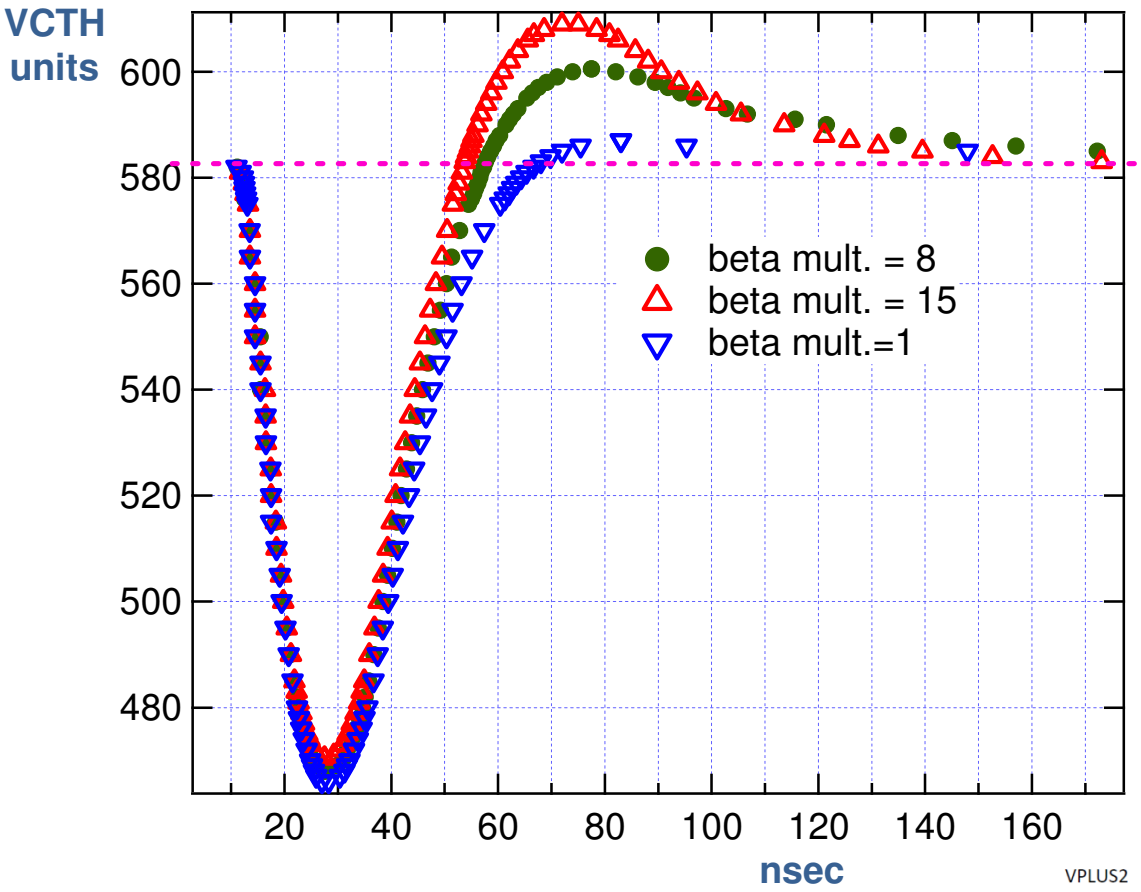
pulse shape measurement technique reminder



for each value of VCTH, sweep time of charge injection to get 2 points on the pulse shape

eventually can build up ~complete picture of the analogue pulse shape

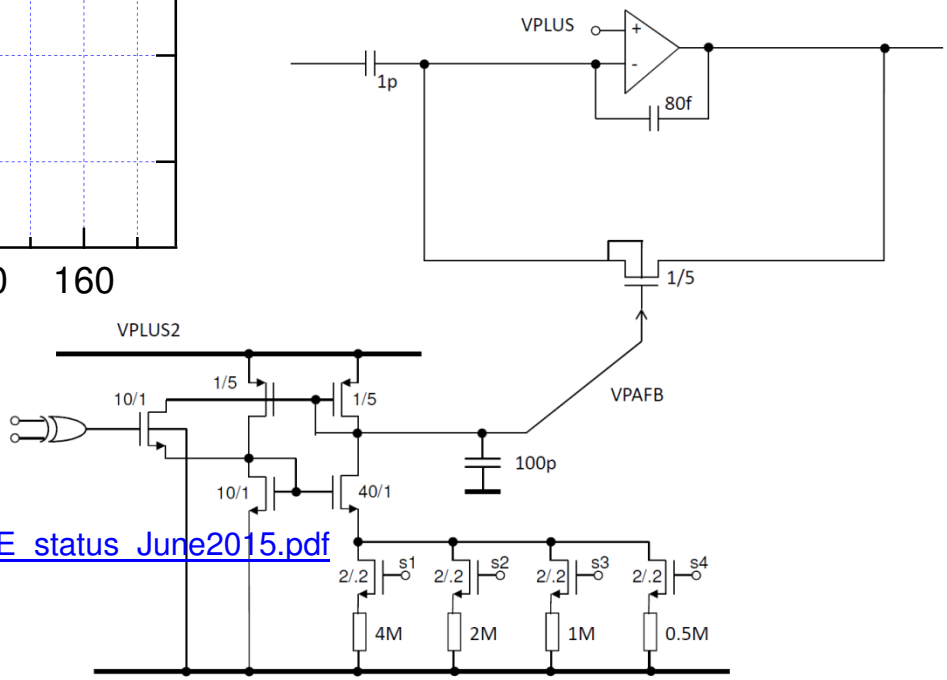
postamp feedback



~2.5 fC charge injected

varying 4-bit beta multiplier setting gives some control over amplifier output duration

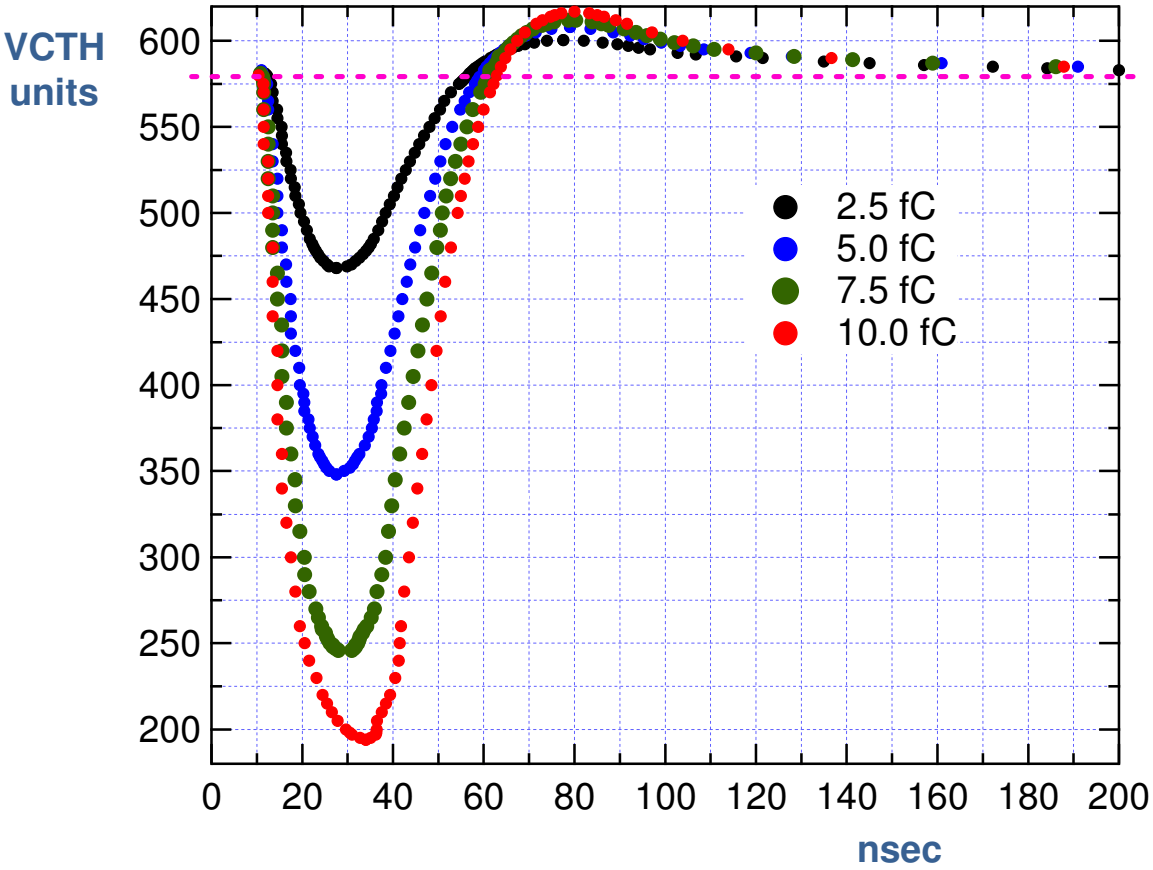
nominal (mid-range) setting is b1000



for comparison with simulations see:

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_FE_status_June2015.pdf

pulse shape vs. signal size



nominal (mid-range)
beta multiplier setting

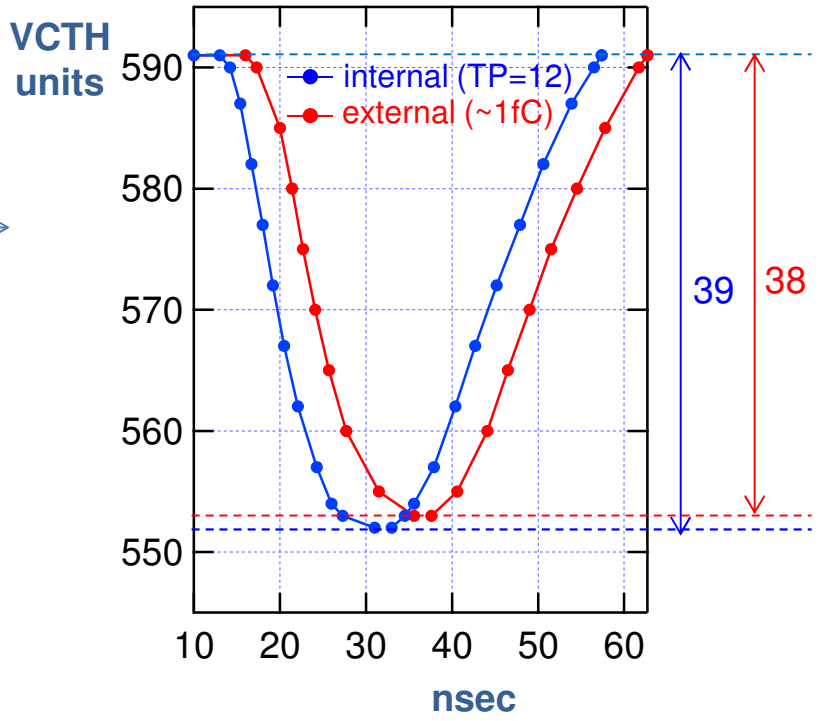
shows effective limiting of overshoot

(postamp feedback FET has high resistance for signal polarity, lower for overshoot polarity)

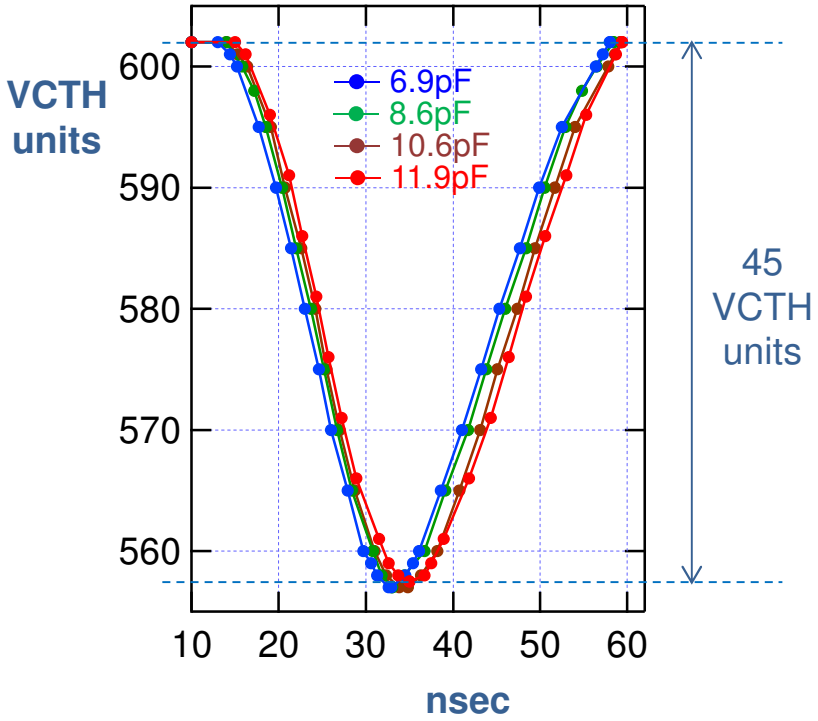
calibration & gain

compare external (known) charge injection with internal test pulse

get TP value 12 (for this channel) = 1.03 fC



pulse shapes for different external capacitance - internal test pulse



knowing VCTH unit = 1.07 mV (in this case)

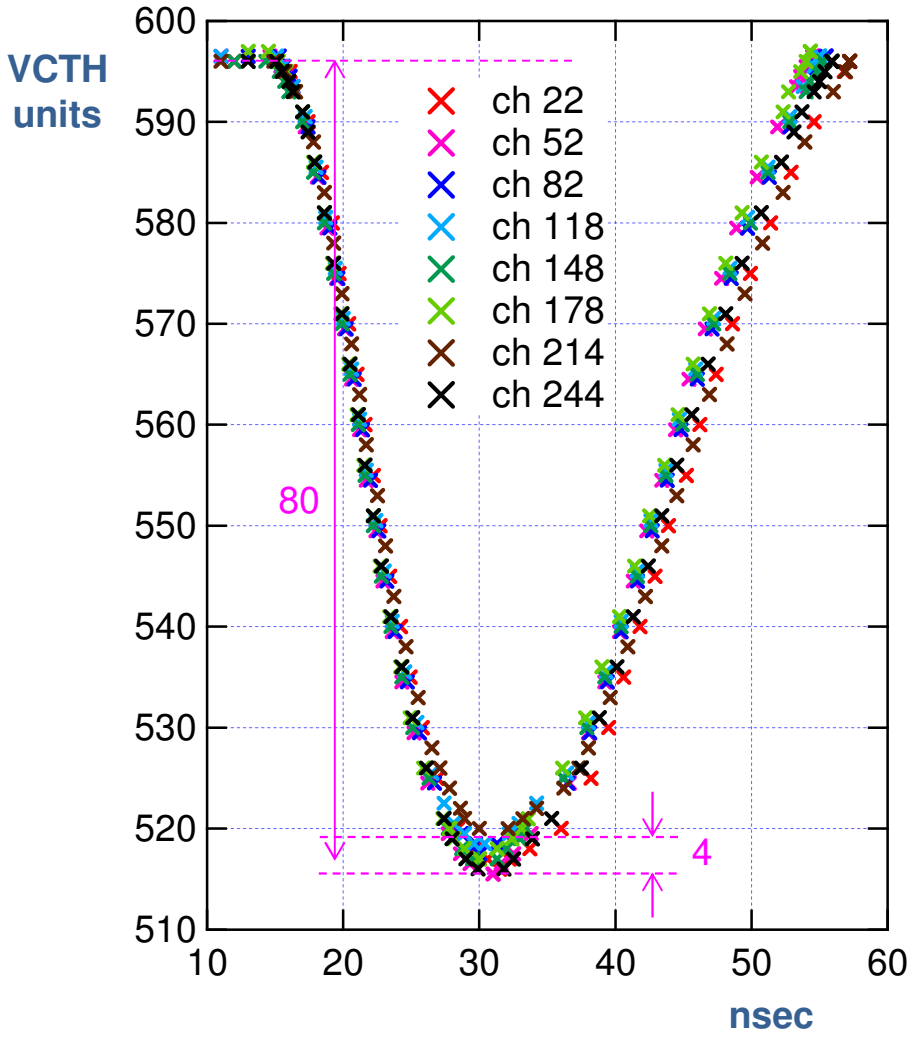
=> CBC3 gain for this channel = 47 mV/fC

(close to specification)

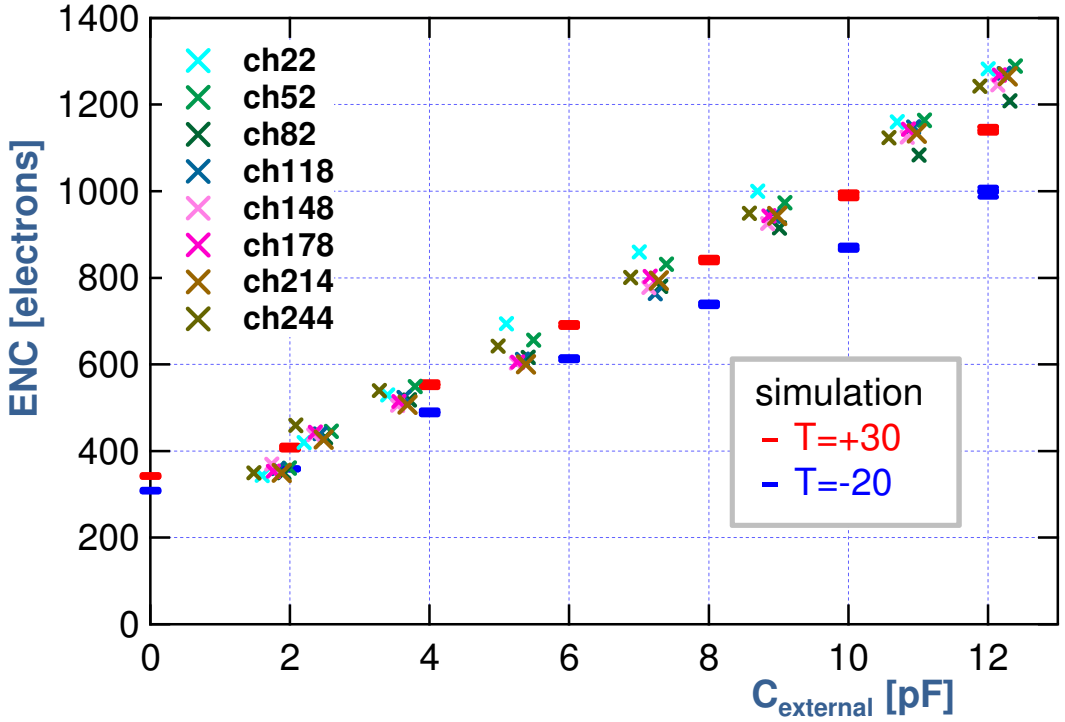
channel uniformity

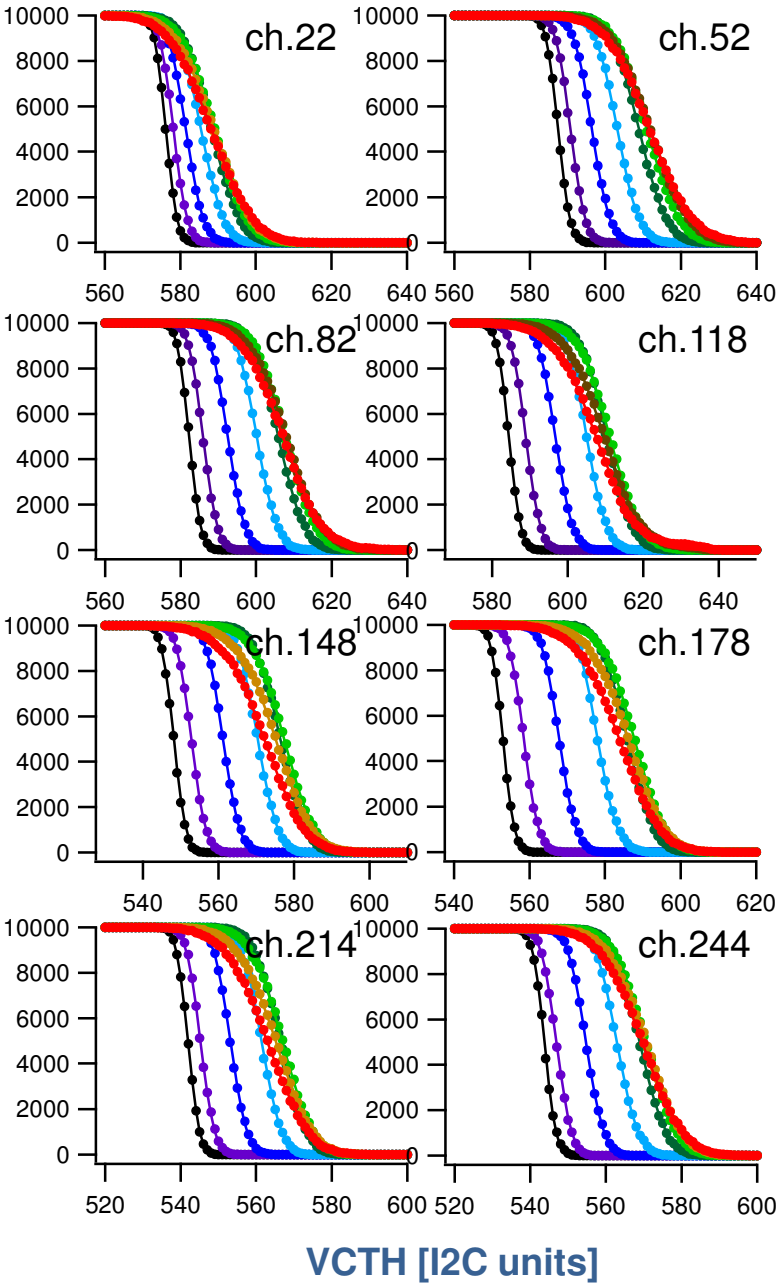
using external charge injection on
all 8 bonded out channels

~ 5% gain spread



noise





measured noise close to simulation

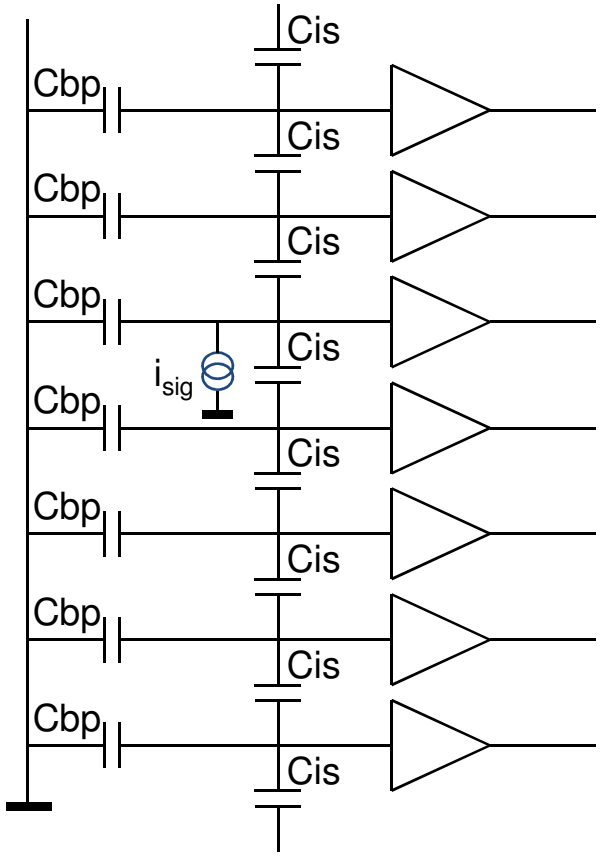
s-curves look ok, but shift with added capacitance

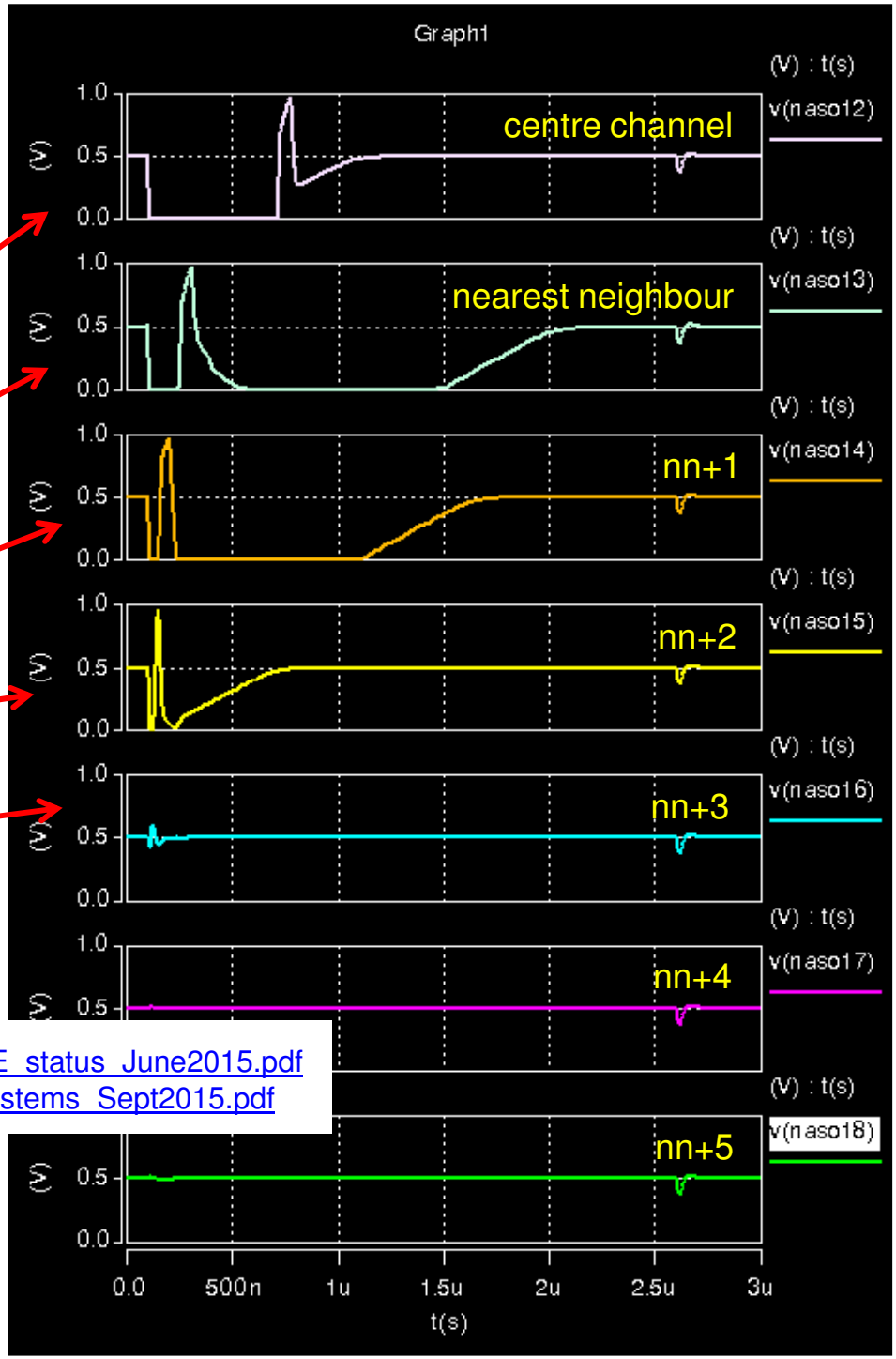
maybe charge injection due to non-perfect coupling between internal and external grounds?

if so, should improve with bump-bonding

hips

hips simulation reminder





for details see:

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_FE_status_June2015.pdf
http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2015/CBC3_systems_Sept2015.pdf

can do something a bit similar using single chip setup with external charge injection

technique

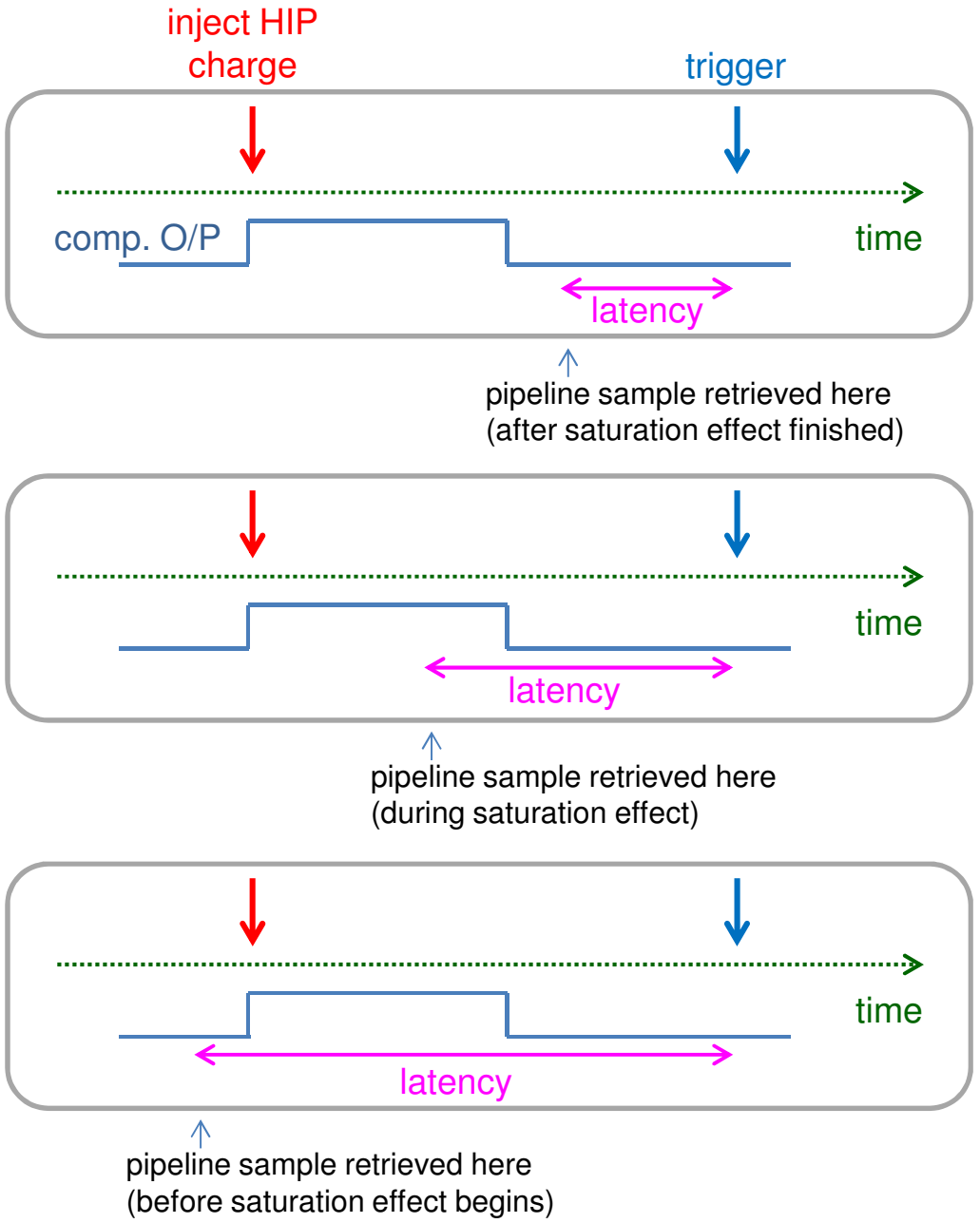
keep fixed separation between charge injection time and readout trigger

vary programmed latency in 25 nsec increments to sweep through full duration of signal saturation

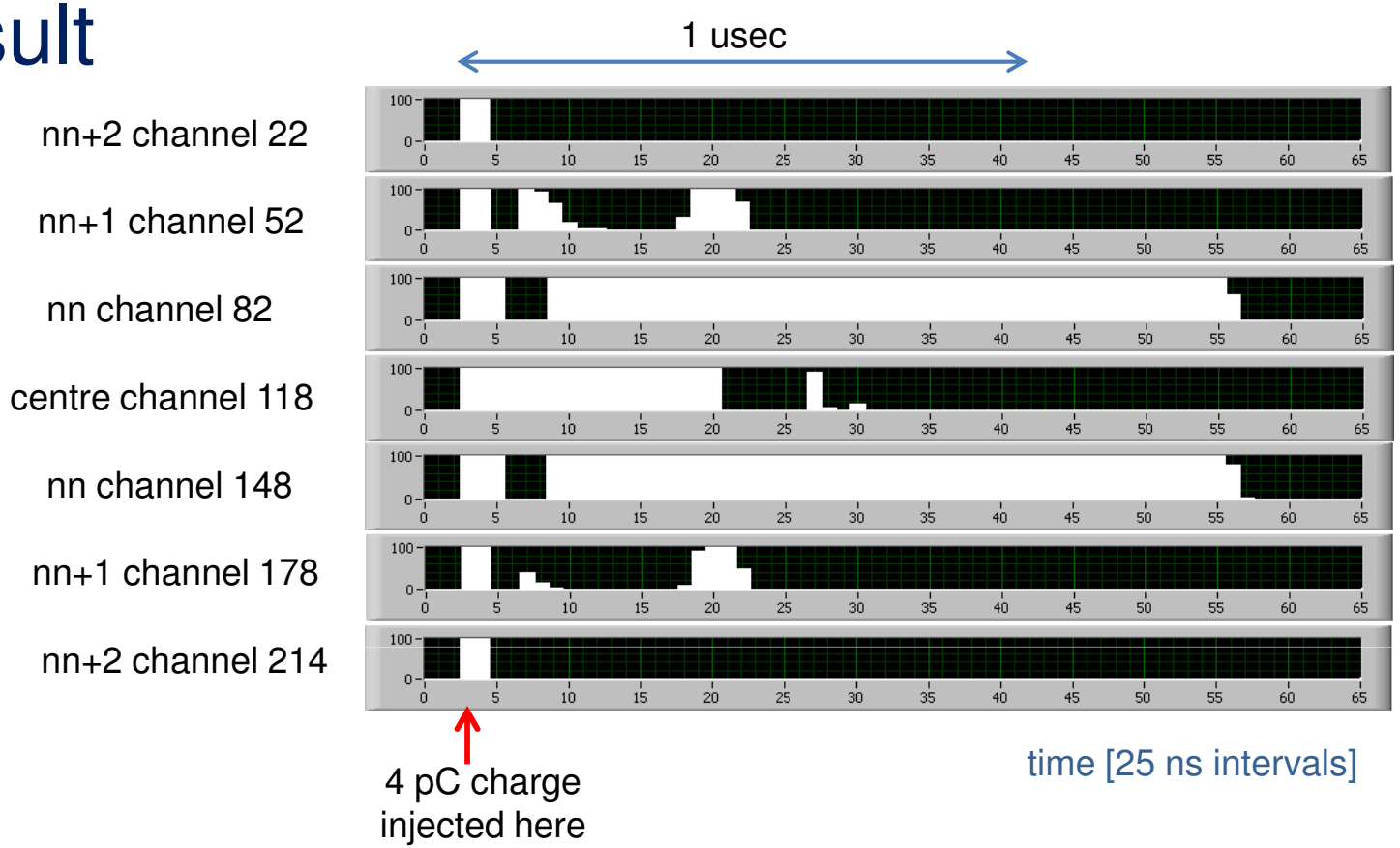
take 100 events at each programmed latency value

use worst case hips signal of 4 pC

VCTH set at ~0.5 fC



result



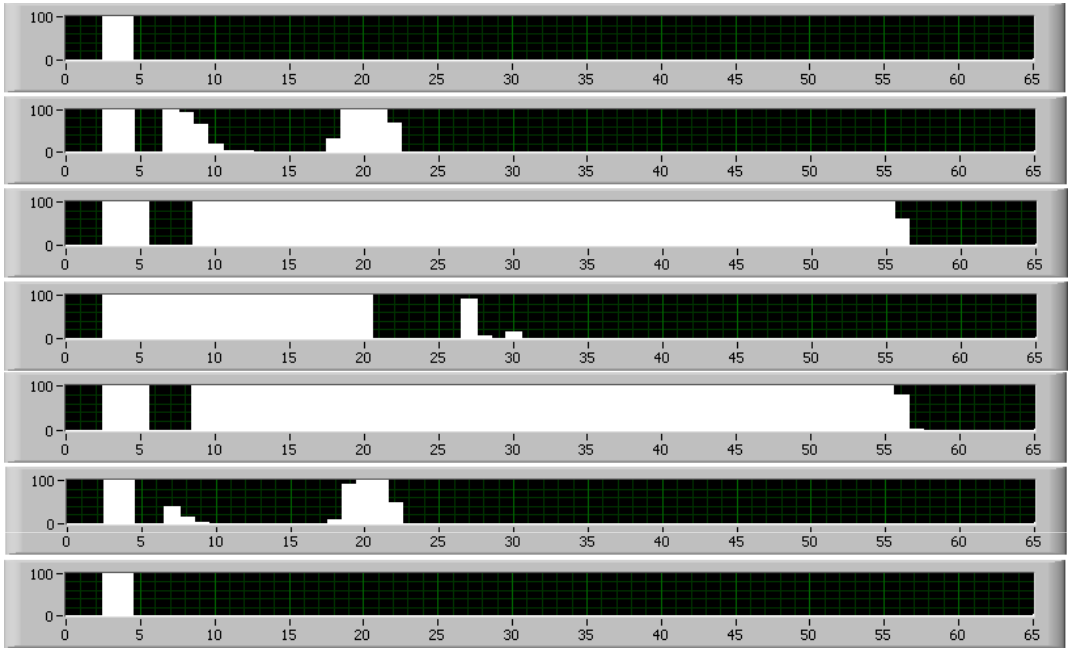
picture above shows the results for the bonded out channels
parasitic capacitances mimic interstrip couplings

behaviour qualitatively similar to simulation in terms of centre channel, nn, nn+1, etc..

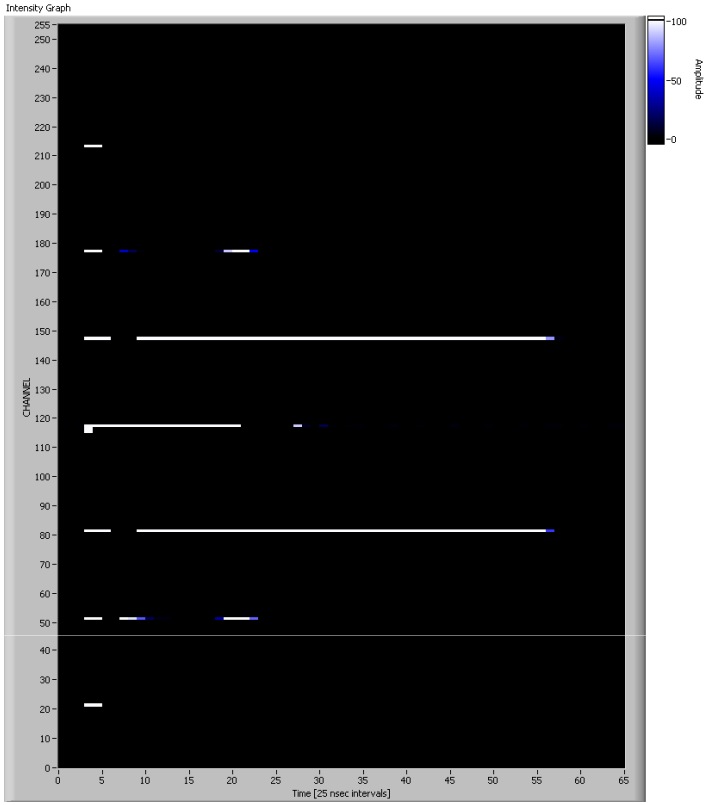
durations of saturation effects similar to simulation and within spec.

what about the channels that are not bonded out?

intensity plot view



picture from previous page

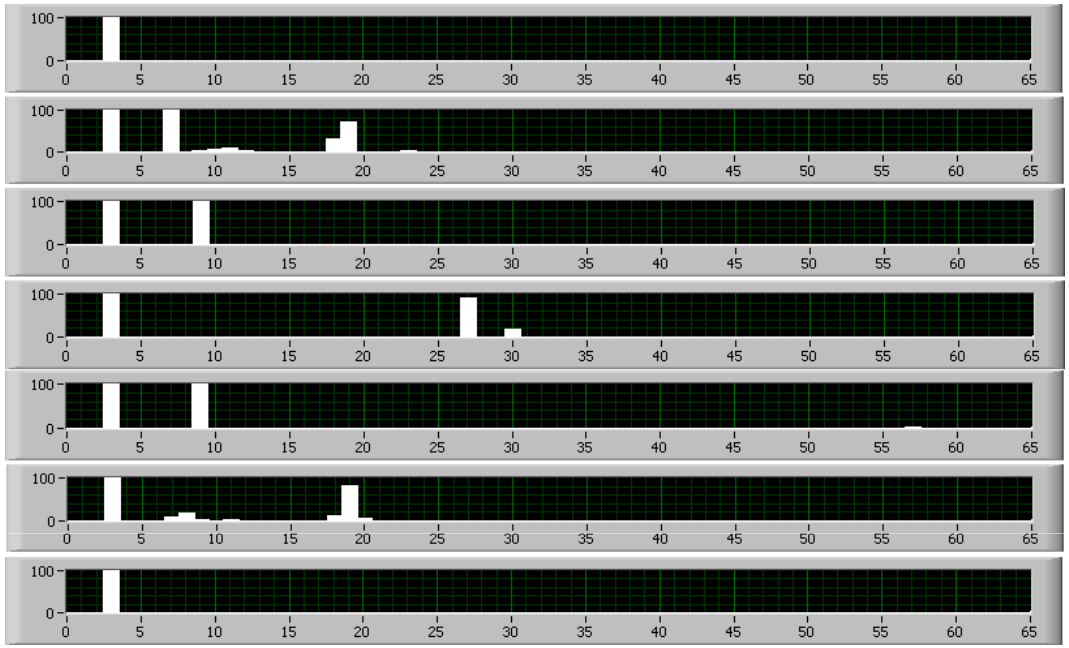


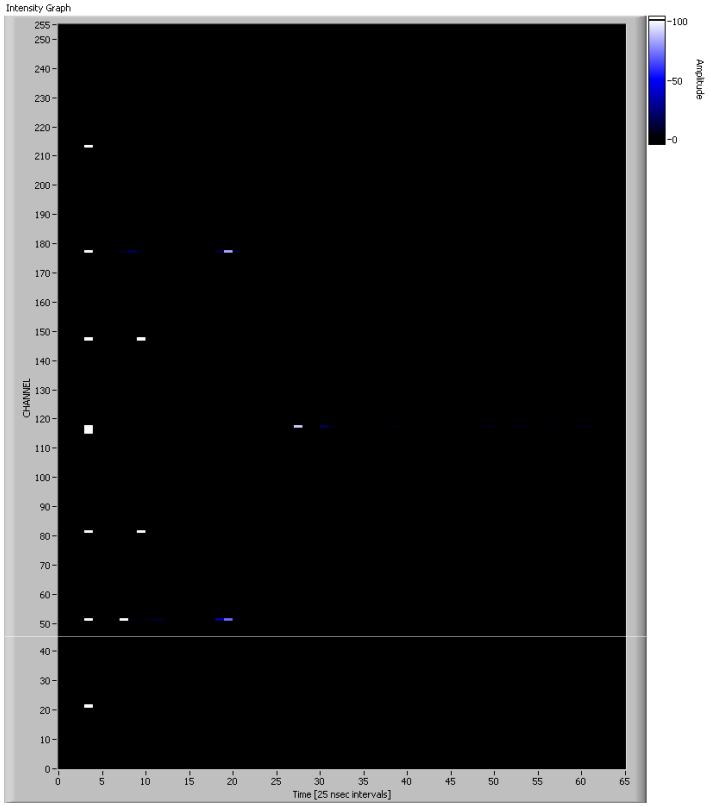
intensity plot shows results
for **all 254 channels**

intensity plot shows that only channels bonded out see signal

=> no significant interchannel coupling on chip

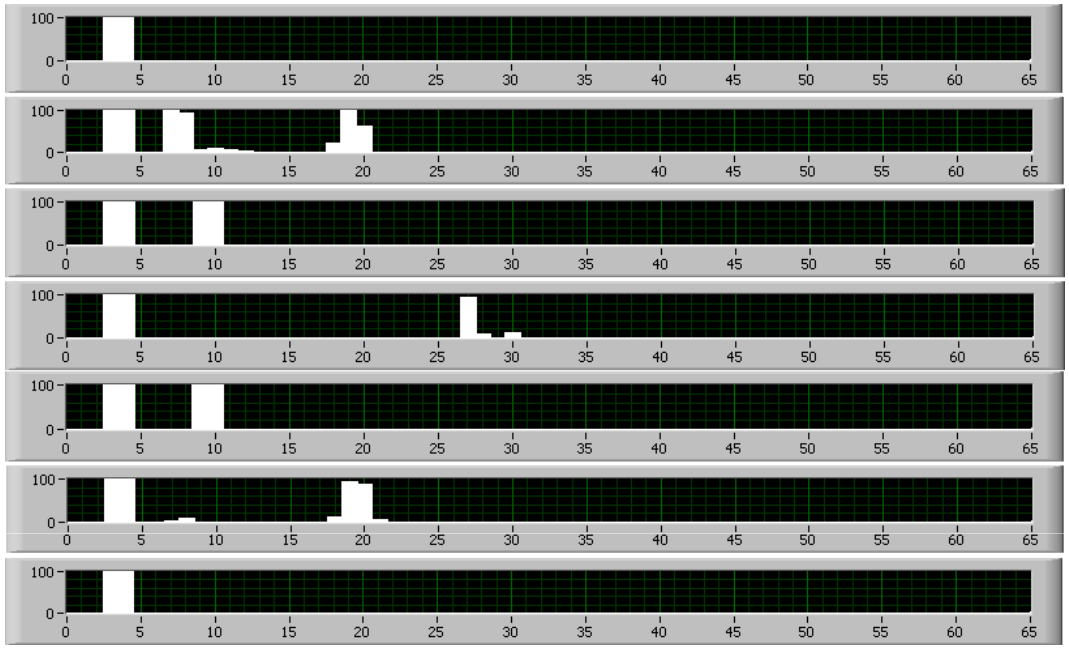
hip suppression on

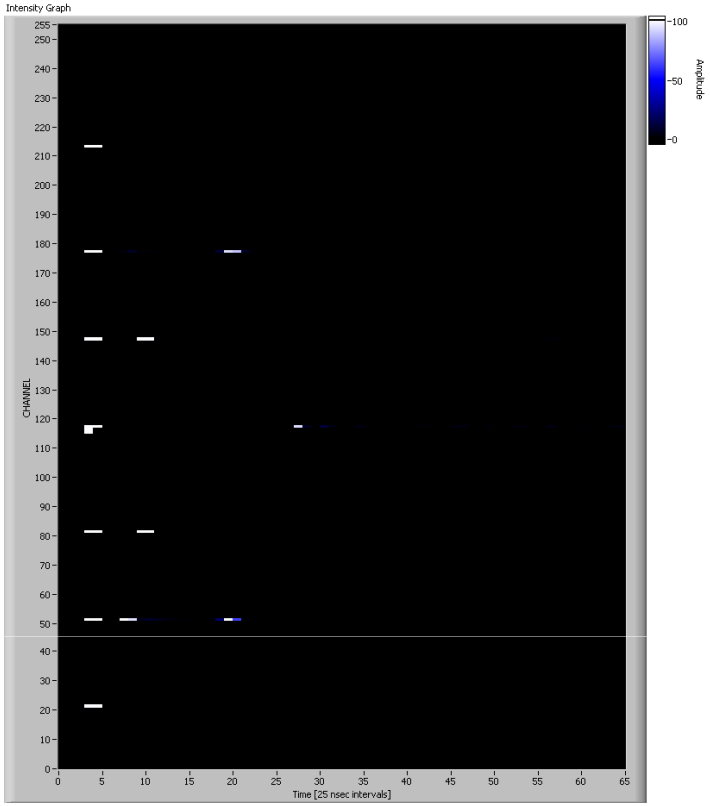




hip count = 1

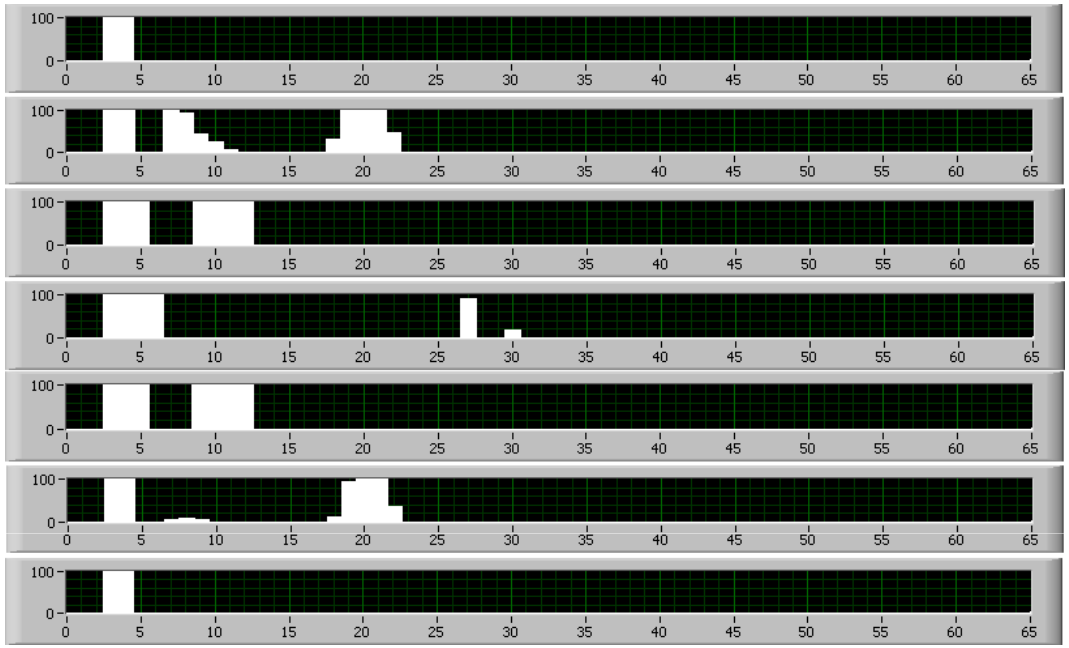
hip suppression on

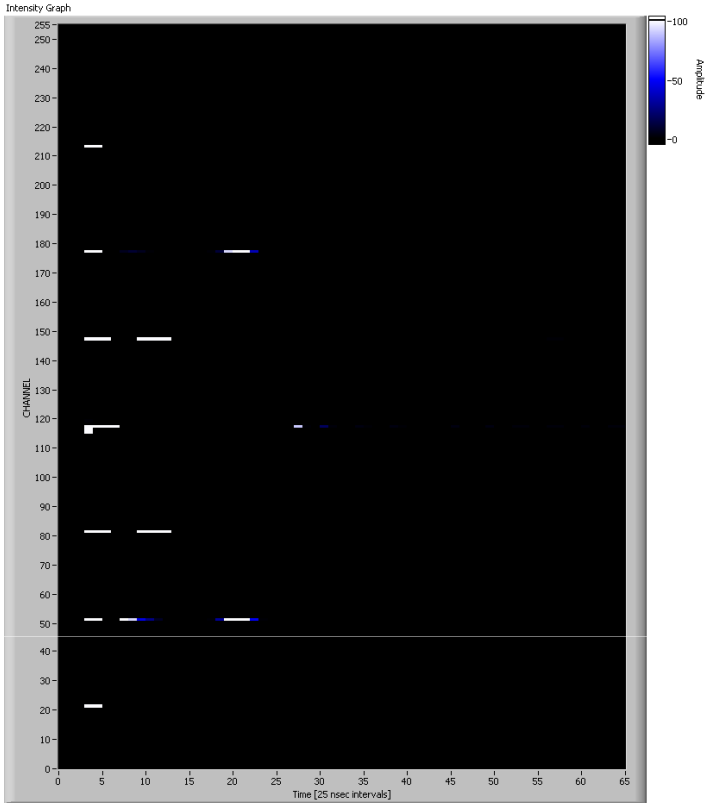




hip count = 2

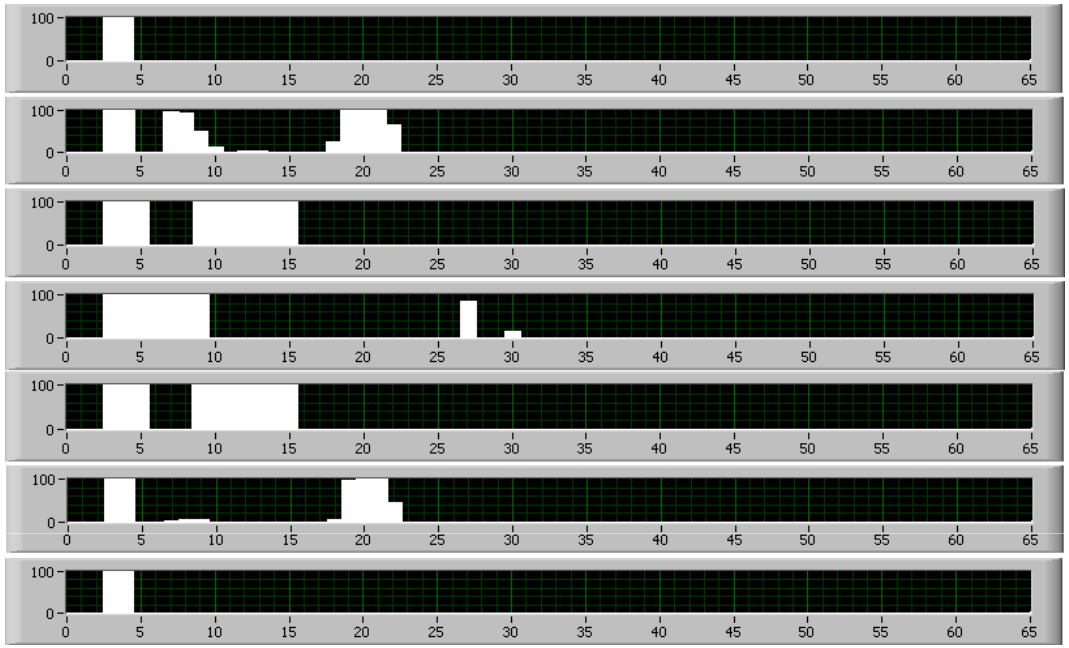
hip suppression on

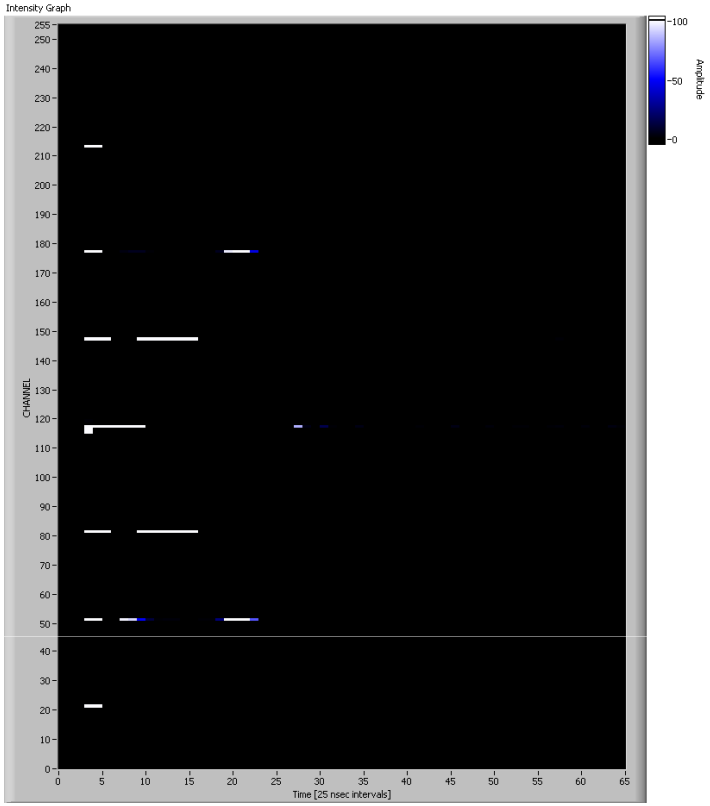




hip count = 4

hip suppression on





hip count = 7

so hip suppression works, but what about sensitivity to normal size signals?

technique

modify measurement to include a test pulse trigger

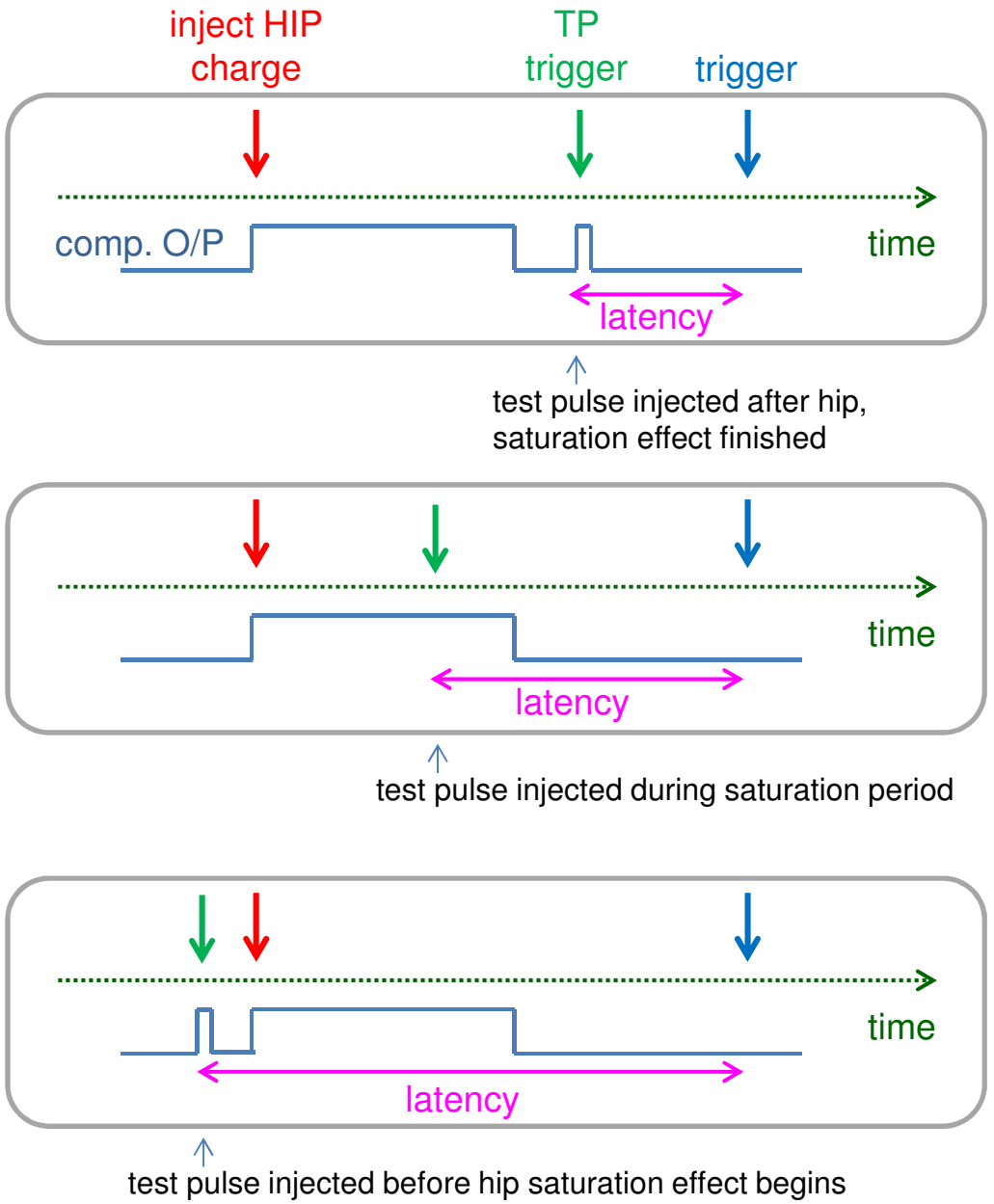
keep TP trigger time locked to varying latency

=> should always see test pulse unless HIP suppression or some other effect associated with HIP response blocks it

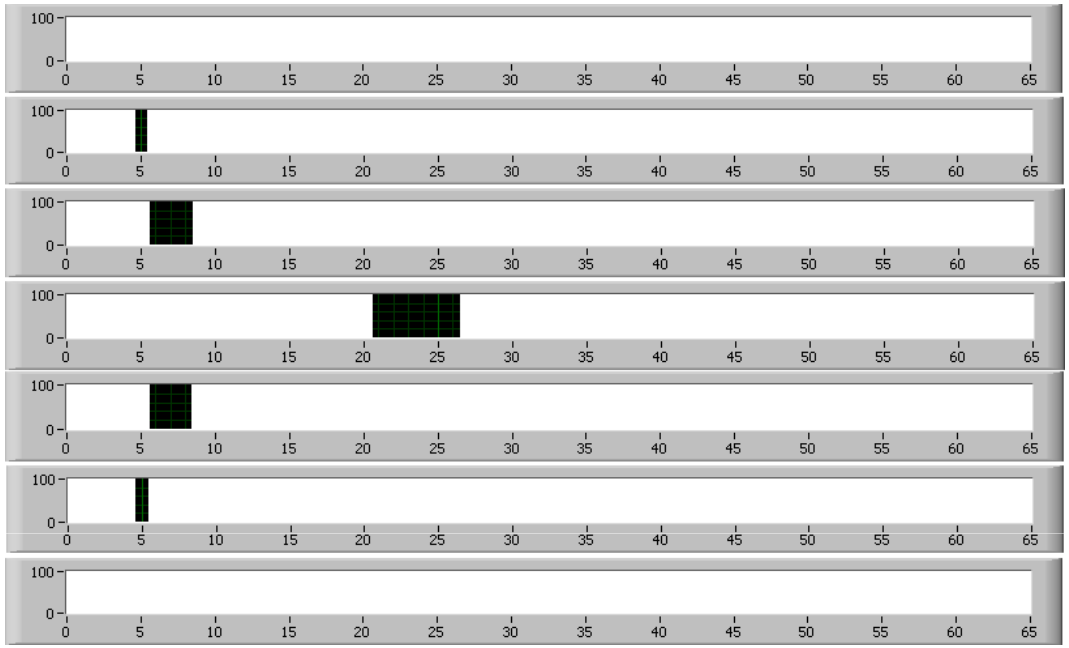
keep worst case hips signal of 4 pC

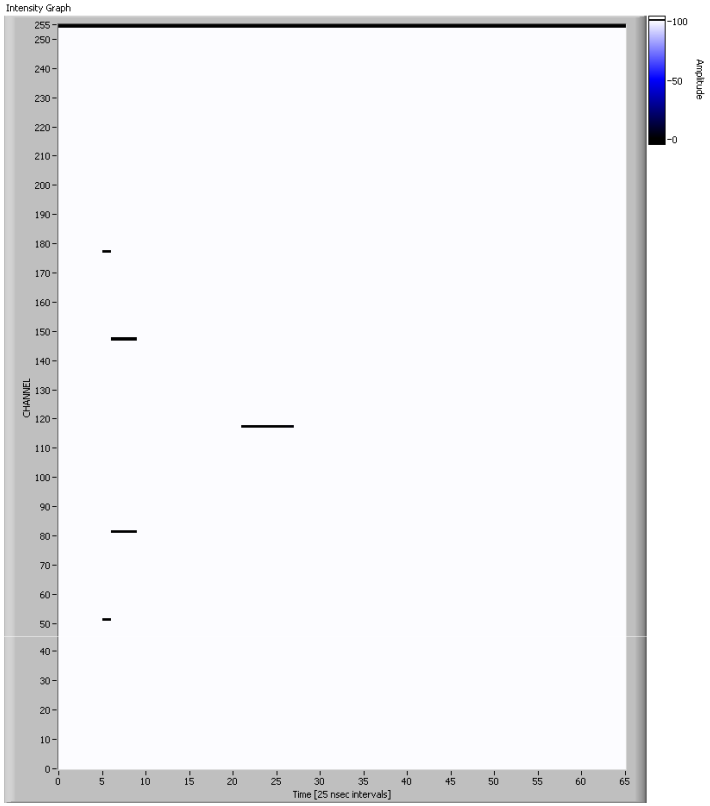
TP charge = 4 fC

VCTH = ~ 0.5 fC



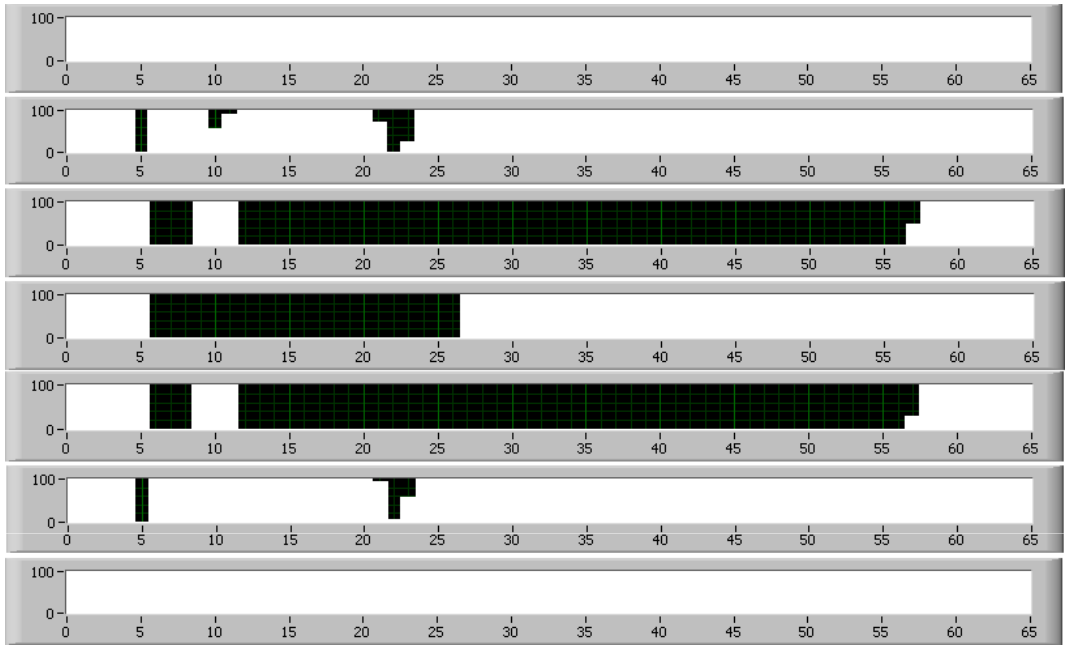
hip suppression off

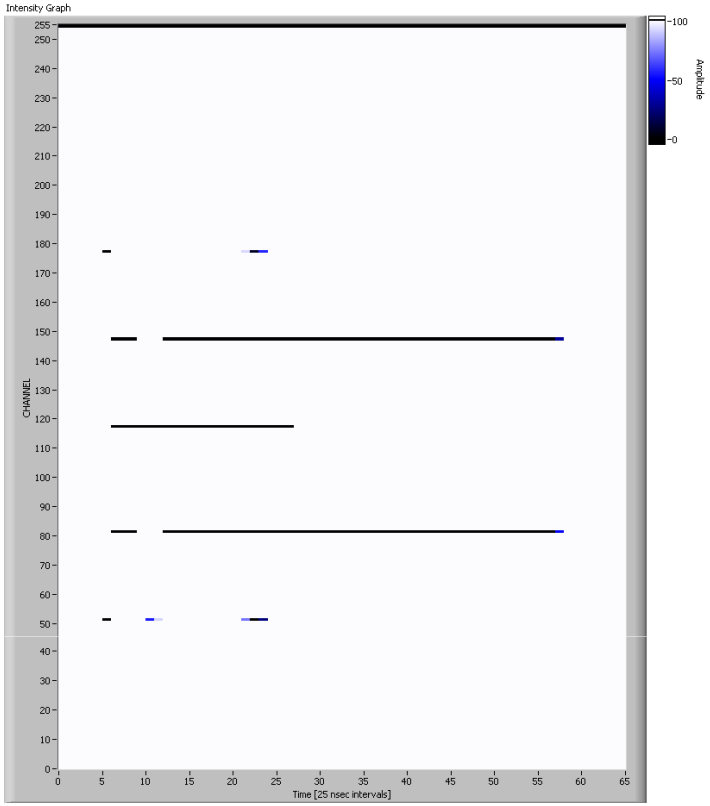




chip is sensitive to normal size signals most of the time, but HIP signals themselves are also present in this picture

hip suppression on





hip count = 3

chip is sensitive to normal size signals most of the time

hip affected channels insensitive until hip saturation has decayed away

summary

wire-bonded single chips studies of CBC3 show pulse shape, gain & noise close to expectation

can look forward to confirming performance with chips bump-bonded to hybrids and with sensors

large signal (hip) electrical charge injection confirms:

- duration of channel saturation effects within spec.
- effects confined to hip channel and neighbours (~no coupling on chip)
- hips suppression circuit functionality

response to real hips should also be confirmed with sensors in test beam