CBC3 status

wafer probe testing status LDO measurements some more digital problems discovered

systems meeting, 23rd February, 2017

wafer probe test setup



interface card mounted on standard Wentworth probecard

CBC3 chips glued on to ceramic disk on vacuum chuck

wafer probe tests

320 MHz full speed running of chip via probe-card seems to work - good news

will go through test procedure step-by-step



wafer probe tests: initialization & 1st tests

check all I2C registers for stuck bits (write & read back all 1's and all 0's)

mode and bias, offsets, bend LUTs, channel masks, ...

load nominal I2C setting and check power consumption

analogue and digital supplied separately

check SLVS<6> for presence of data frame (triggered output data)

check SLVS<5> for presence of tick mark

tune the bandgap, program the chip ID and blow the e-fuses

e-fuse functionality has now been verified on single chip test setup

wafer probe tests: tune the offsets





calculate average value, VCTH_{50%}

set VCTH to VCTH_{50%} and tune the offsets to align all the channel pedestals to that value

average offset value should be ~128



wafer probe tests: s-curves

acquire s-curves for pedestals and with test pulse for all channels

subtract pedestals from test pulse

any chip with a low or non-responsive channel can now be identified



wafer probe tests: pipeline check

1) sweep trigger time w.r.t. fast reset and check that all pipe address values appear

2) remove fast reset and apply triggers pseudo-randomly

check all pipe addresses and L1 counter values appear in the data (can't systematically observe every L1 counter value without very long test sequence)

simultaneous with above tests can check for no stuck bits in any pipeline cell by setting VCTH above or below pedestal level



wafer probe tests: buffer ram check

send 32 triggers and read out the 32 resulting frames for all 0's in the data, then all 1's

verify no stuck bits anywhere in the data region of buffer ram

run pseudo-randomly until each bit of pipe address region of buffer ram has returned at least one 0 and one 1



channel masking

verify all channels can be individually masked by setting VCTH so that all channels will fire unless masked

wafer probe tests: stub logic

check all stub addresses and bend information correctly reported

set VCTH so all channels firing all the time, then use channel mask to generate specific clusters

sweep seed cluster across chip, sweeping window cluster throughout window

repeat for all combinations of seed and window cluster widths

can do 3 stubs at a time, but still takes ~ 1 minute





wafer probe tests: CWD & layer swap logic

for all CWD values (1 to 4) check that clusters too wide are rejected

check for all cluster positions

check layer swap logic by looking at bend data

check for all cluster positions



this step takes ~ 15 secs

wafer probe tests: pT window width



but turns out that logic has been coded to generate stub address + invalid bend code (b1000)

bend codes example mapping reminder



invalid bend code b1000 does not appear

wafer probe tests: pT window width

example 2: cluster occurs outside programmed window
 but inside maximum possible window
 get stub address + invalid bend code (b1000)
this is not ideal, wastes off-chip stub address bandwidth
not a problem for CBC3 users

stub address from cluster outside window will need to be suppressed with logic change

CBC3 wafer probe test implemented by checking for invalid bend code from clusters outside programmed window

for all possible window widths and all window positions this step takes ~30 seconds



wafer probe tests: window offset

check all window offset possibilities, for all 4 window groups

can verify by always generating vertical stubs

if window is offset then expect bend code to change

all offset values (+/- 6 half strips), all window positions

test takes ~15 seconds

overall test procedure for stub logic takes 2 minutes

(would like to speed up)



wafer probe tests: Hit Detect & HIP suppression



can use channel mask to verify all routes through MUXes to pipeline and stub logic

no mechanism to generate HIPs, but can verify HIP suppression works since should get no output if channels firing all the time

wafer probe tests: Ck40 DLL

check that output data present for all programmable Ck40 DLL values

wafer probe tests: analogue bias measurements



bias voltages and currents swept and/or measured via power supply current or analogue mux output

will want to study chip-to-chip variations and reject significant outliers

bias measur	rements
0.6042	IPA
0.5924	IPRE2
0.2709	CAL_I
0.2440	Ibias
0.4232	VCTH
0.6854	VBGbias
0.5514	Bandgap
0.1933	VPAFB
0.5423	nc50
0.5706	IPRE1
0.3131	IPSF
0.7649	IPAOS
0.2645	ICOMP
0.0986	IHYST
0.3472	CAL_VCASC
0.5363	VPLUS2
0.5388	VPLUS

wafer probe tests: summary

running chip at 320 MHz on wafer appears viable

detailed set of tests prepared - should exclude most problems

note: nearest neighbour logic will need to be verified in hybrid tests

overall duration of test ~4 mins

for production would prefer less than ~3

(could maybe run I2C faster?)

plan to migrate from VME to FC7 based system eventually



L1 readout problem

have discovered problems in the L1 data readout

for some DLL settings, but only when multiple triggers are sent



the way it should work



active output data frame length 276 bits (22 header, 254 data)

extra 28 clock cycles introduced due to clock domain crossing issues

=> 304 clock cycles altogether => 950 nsec.

multiple triggers occurring with a spacing less than 950 nsec

expect consecutive output data frames with minimum 950 nsec spacing

the problem

Programmable Delay 40 MHz Region uses Ck40_DLL

programmable in 1 nsec steps

320 MHz Region uses 320 MHz and Ck40_ref (the input to the DLL)

for some values of DLL setting (1 nsec resolution) the L1 data readout logic malfunctions if two (or more) triggers are applied

but only if the trigger spacing is less than 950 nsec

symptoms

frame separation reduces to 925 nsec.

data, including header, from 1st frame is repeated in 2nd frame

multiple frames appear, not corresponding to triggers

.... (not a completely exhaustive list, not all symptoms appear simultaneously)



example

Ck40 DLL setting = 2

4 consecutive triggers sent

test pulse timed to be in 2nd frame

readout data looks ok

header spacing 950 nsec.

Ck40 DLL setting = 3

same triggering and test pulse conditions

header spacing reduced to 925 nsec.

2nd frame test pulse data only starts to appear ~ third way through second frame, and spills over into 3rd frame

more detailed look shows header pipe addresses not correct



the problem: results for 12 chips

📕 no problem observed

some problem observed



observations

problem DLL values depend on VDDD, and are not the same for all chips but appear to always occur at ~3 nsec spacings (probably related to 320 MHz clock) DLL values in between the 3 nsec problem spacings show no problems

the problem: results for 12 chips

no problem observedsome problem observed



clear "bands" of 2 DLL settings where problems don't appear

=> should choose one of these when operating the chip in conditions when trigger spacings less than 950 nsec

the problem: one chip, finer VDDD steps

problems migrate between DLL values as VDDD changes

"safe" DLL settings remain clear of problem



DLL value

summary of situation

for most DLL settings the triggered L1 data readout works as expected

for some DLL settings there is a logic malfunction following a trigger if one, or more, triggers are sent while data from the 1st trigger are being read out

the "safe" values appear to be the same across chips - related to Ck320 cycle

note: this only applies to the triggered data - the stub data are not affected

this problem needs to be understood and fixed

engineers are working - already found a timing issue in the triplicated control logic for the Buffer RAM to PISO interface



overall summary

wafer probe test setup ready - probing at 320 MHz looks feasible

need to get wafers to IC ~ now

should be able to ship tested wafers ~ mid March

LDO appears to be working well

some more digital bugs discovered

will need to be fully understood and fixed

can work around for this version of the chip

extra





CBC3 digital interfaces	\uparrow	S1<7>	S2<7>	S3<7>	B2<3>	Sync	R	
		S1<6>	S2<6>	S3<6>	B2<2>	Error	R	
output data: up to 3 stubs data transmitted to CIC/BX	\longrightarrow	S1<5>	S2<5>	S3<5>	B2<1>	OR254	R	
6 SLVS diff pairs @ 320 Mbps	25 ns	S1<4>	S2<4>	S3<4>	B2<0>	SoF	R	
		S1<3>	S2<3>	S3<3>	B1<3>	B3<3>	R	
		S1<2>	S2<2>	S3<2>	B1<2>	B3<2>	R	
		S1<1>	S2<1>	S3<1>	B1<1>	B3<1>	R	
roadout data		S1<0>	S2<0>	S3<0>	B1<0>	B3<0>	R	
readout data frame length 950 nsec => up to 1 MHz L1 triggering capability	R = L1 triggered readout data time flow <u>top</u> to <u>bottom</u> (e.g. S1<7> output first)							
MSB 1 st Total active fram	me length = 2	76 bits :	= 862.5	ns —		•		

2 start bits 9 bits pipe 9 bits L1 2 error bits address counter ch.254 1st 254 bits strip readout data (latency, buffer overflow) no - CBC3 actually transmits ch1 first

fast control 320 MHz clock 320 Mbps fast control line

40 MHz generated from fixed sync pattern in fast control data normal command structure can't be confused with sync pattern 40 MHz clock

