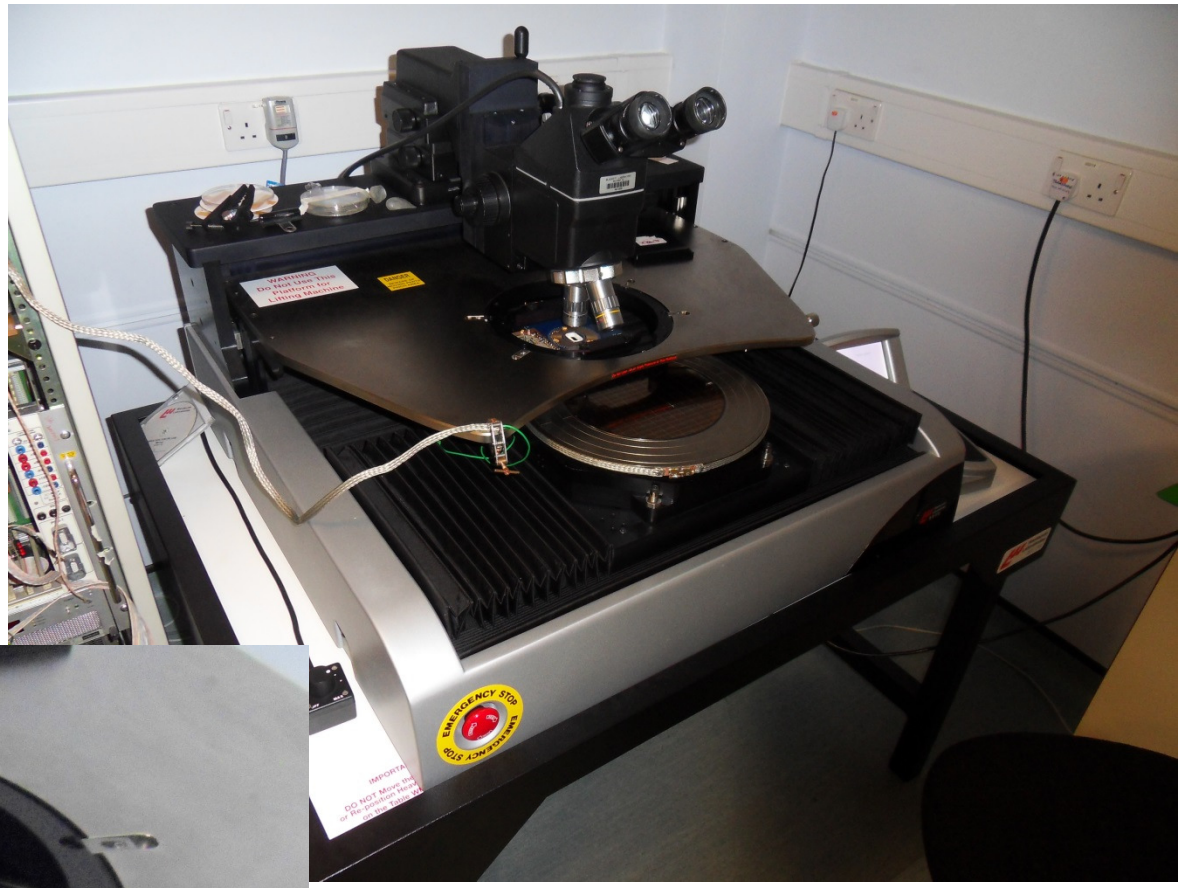
CBC3 wafer probe test status

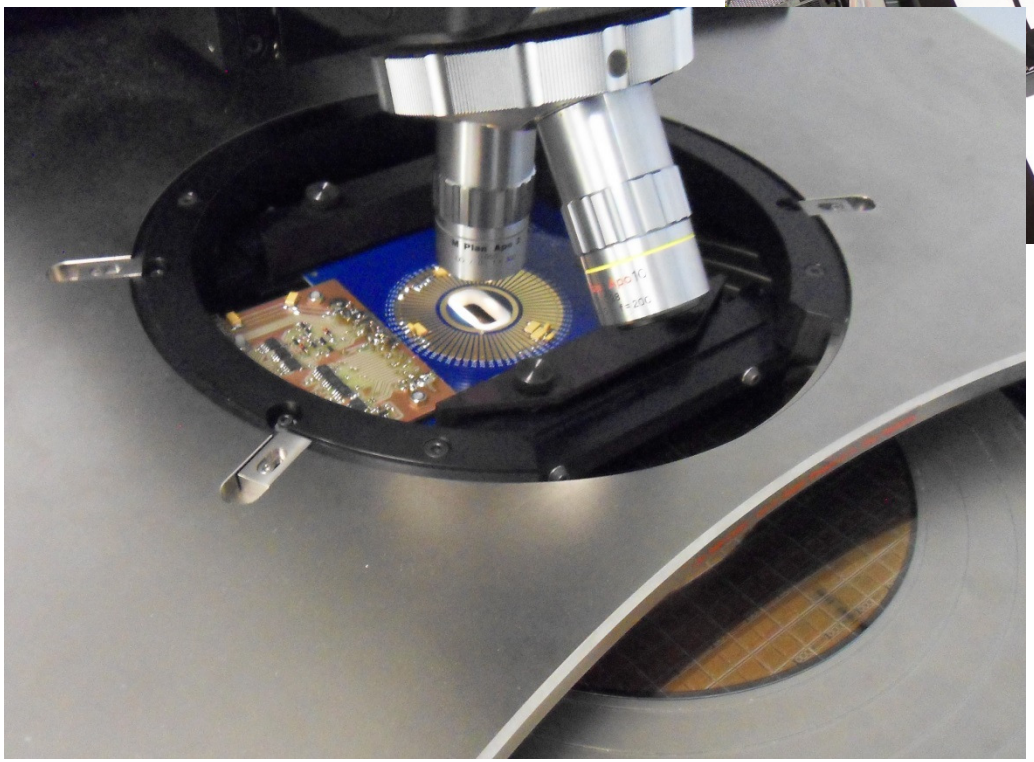
systems meeting, 4th April, 2017

wafer probing

some delay because of a fault with usual prober - had to switch to alternative 300 mm machine

different control instructions and setup procedure => software changes





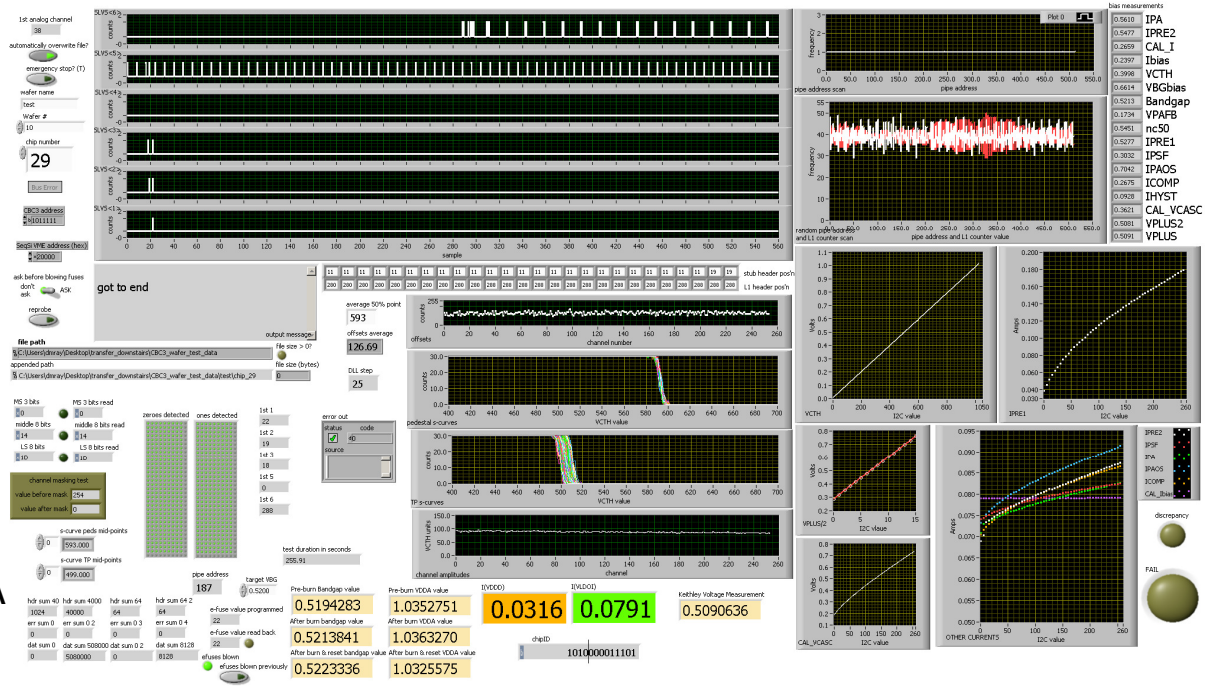
5 CBC3 wafers now tested and despatched to PacTech - delivered yesterday (3rd April)

wafer probe tests

all tests run at full speed (320 MHz)

categorize failures as:

- I2C failure
  - no response
  - stuck bits in registers
- power
  - current too high
    - I_{VDDD} > 50mA, I_{VDDA} > 200mA
- pipeline
  - any stuck bits
- stub logic
  - wrong address or bend info returned



← chip failed immediately if any test failed up to here

- channel
  - high/low or non-uniform gain (one or more channels)
  - large spread on offsets after tuning
- other
  - DLL, physical damage noticed, file not written, ….

for more details on tests see last time:

http://www.hep.ph.ic.ac.uk/~dmray/systems_talks/2017/CBC3_status_Feb_2017.pdf

e-fuses (1)

unique chip ID set by 19 bits:

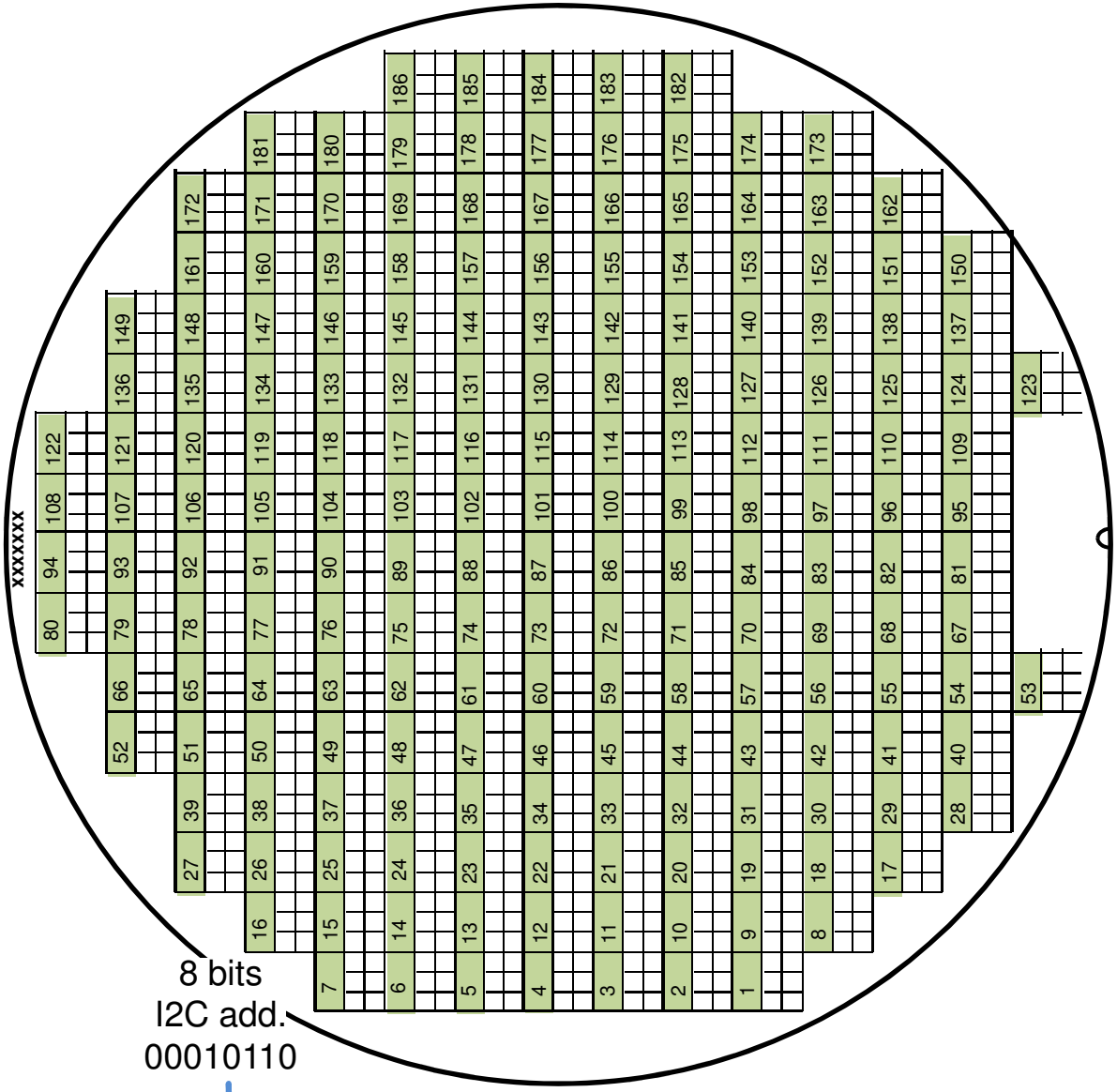
10 bits wafer ID
9 bits chip position on wafer

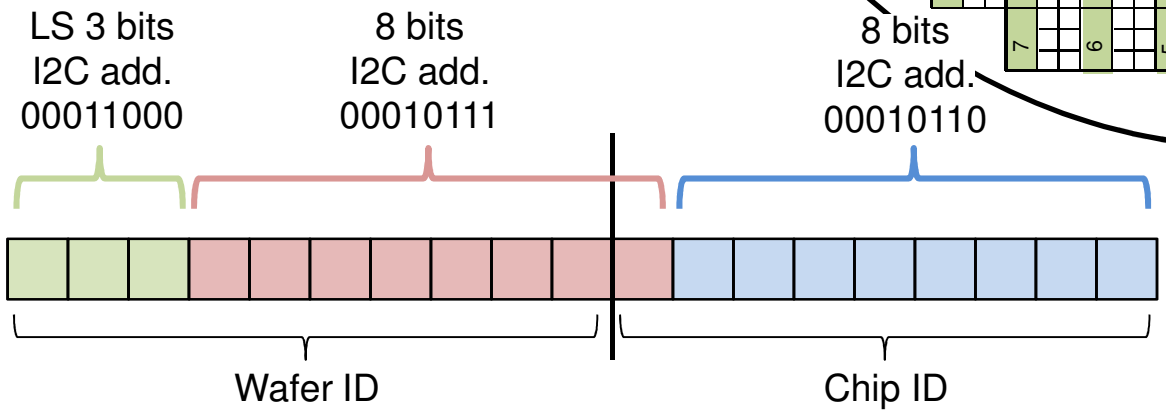
CBC3 wafer numbers start at 1

chips 1 -> 186

test results file kept for each chip

=> can check whether correct chips have been used, and if any anomalous behaviour on hybrid can be correlated with performance at probe test time





e-fuses (2)

bandgap tune register swept and BG voltage measured through analogue mux

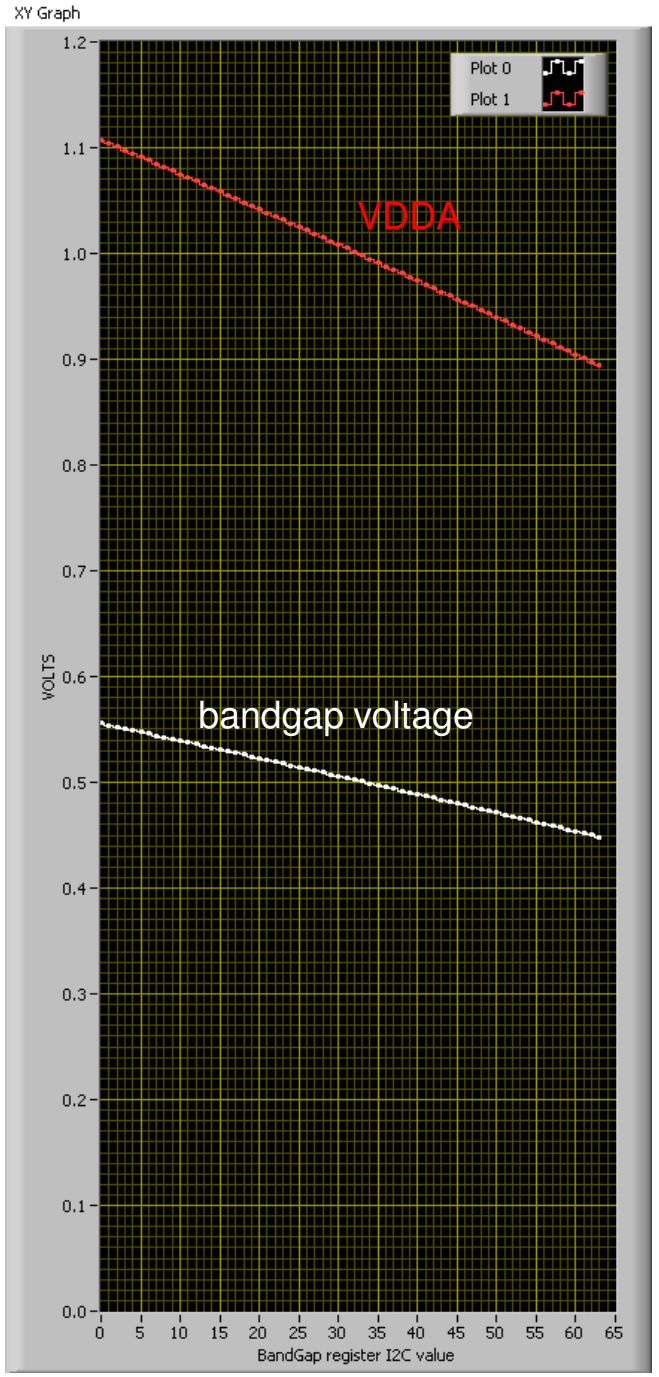
VDDA also measured - should be 2x bandgap

determine register setting which gives voltage closest to desired BG output

for now have chosen 0.52 V as target

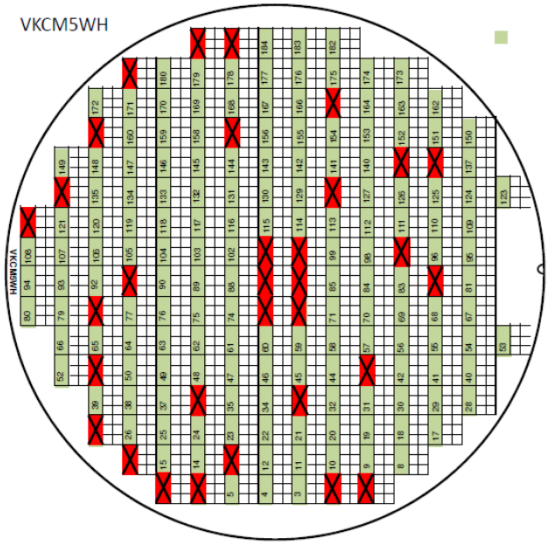
(bit arbitrary, decided no need to aim for absolute minimum VDDA)

can be overridden later if desired



results

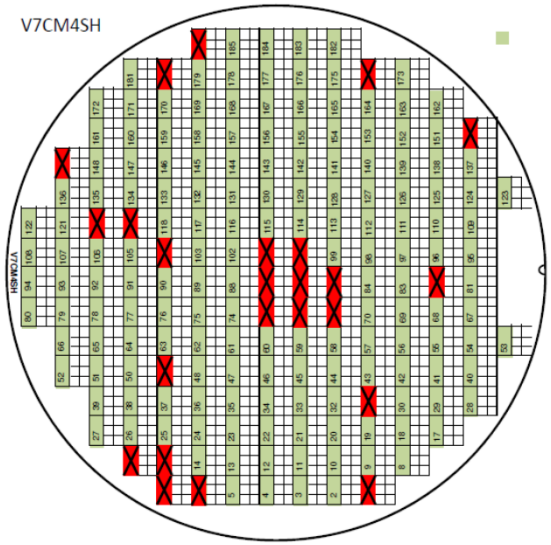
VKCM5WH



154 passes
32 failures
83% yield

failed chips

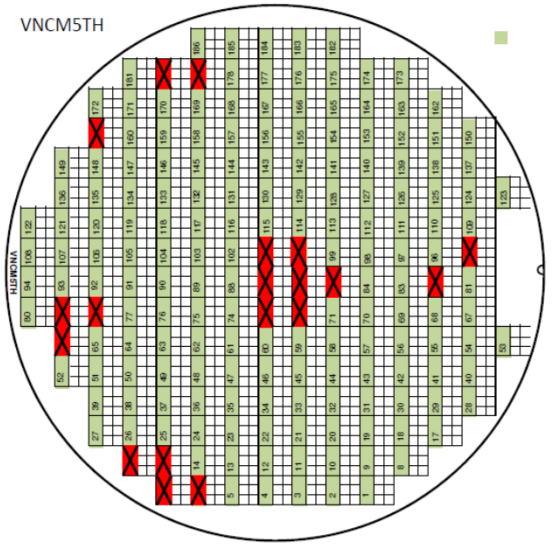
V7CM4SH



162 passes
24 failures
87% yield

failed chips

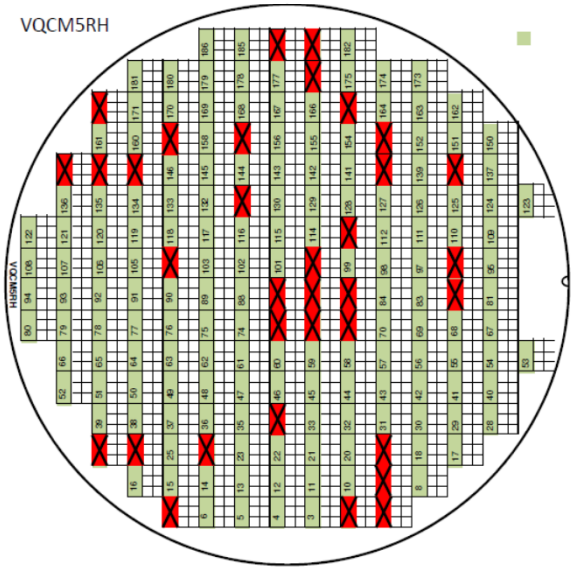
VNCM5TH



167 passes
19 failures
89% yield

failed chips

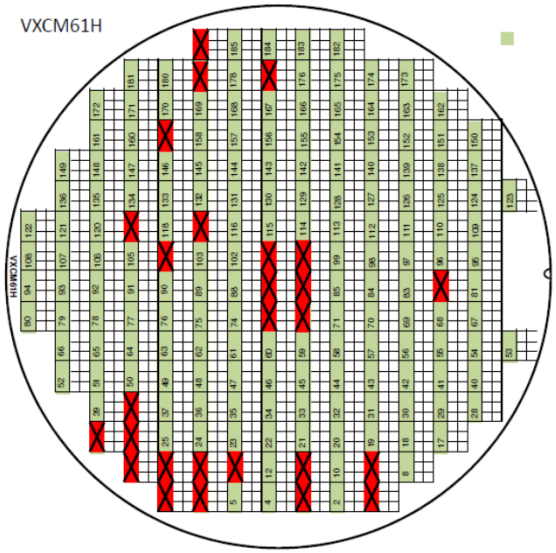
VQCM5RH



152 passes
34 failures
81% yield

failed chips

VXCM61H



159 passes
27 failures
85% yield

failed chips

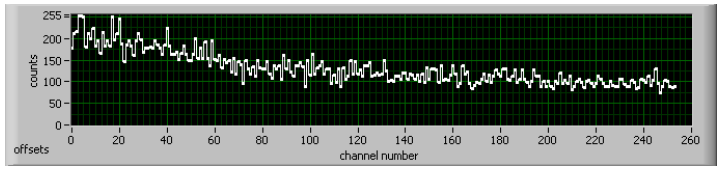
wafer probe failure summary

	VQCM5RH	VKCM5WH	VXCM61H	V7CM4SH	VNCM5TH
yield [%]	81	83	85	87	89
I2C failure	0	5	5	0	2
power	0	0	3	0	0
pipeline	5	4	0	0	3
stub logic	1	1	2	1	0
channel	20	18	14	19	14
other	8	3	2	4	1

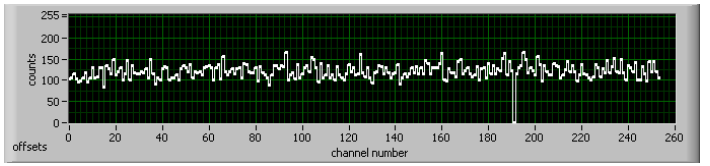
some chips fail in more than one category - first to occur is one listed in table
channel failure is largest category - some examples on next slide
channel failure if any channel shows gain > +/- 10% from the mean

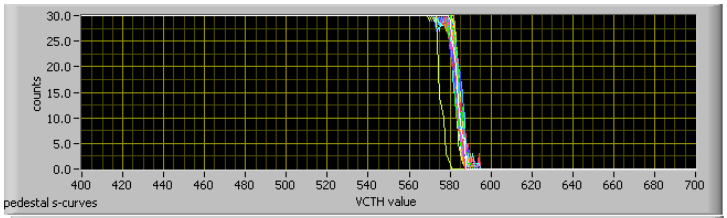
most (~all) of failures in centre of wafers are channel failures

types of channel failure

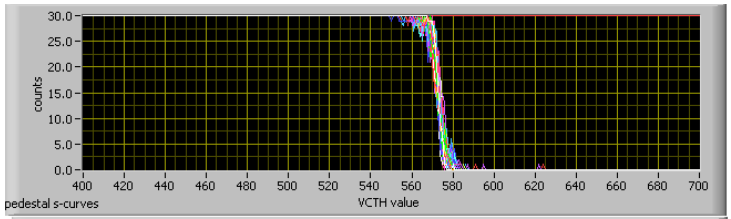


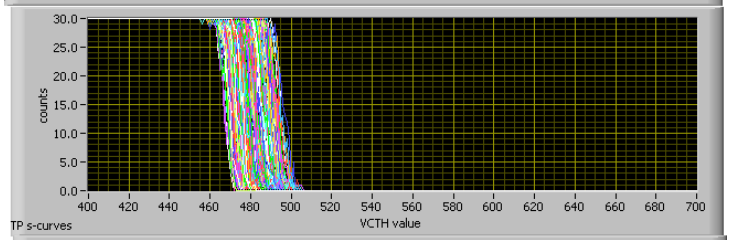
offset values after tuning



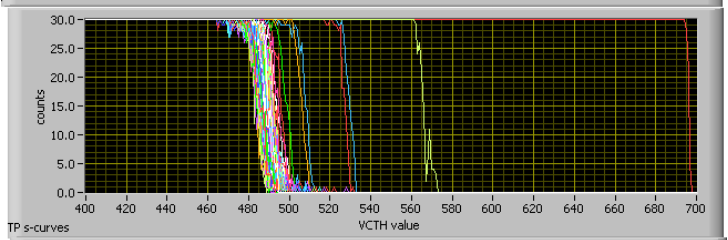


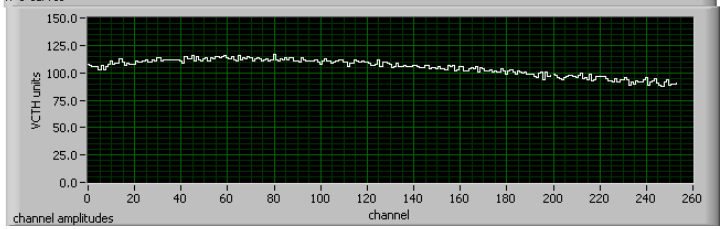
pedestal s-curves



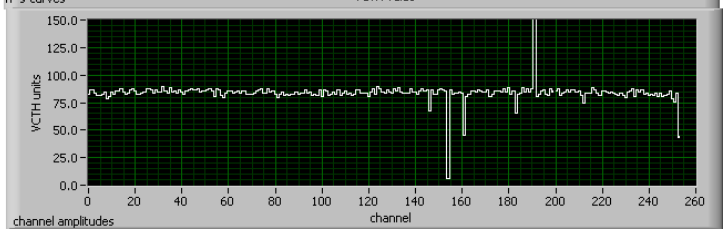


test pulse s-curves





test pulse - peds (= gain)



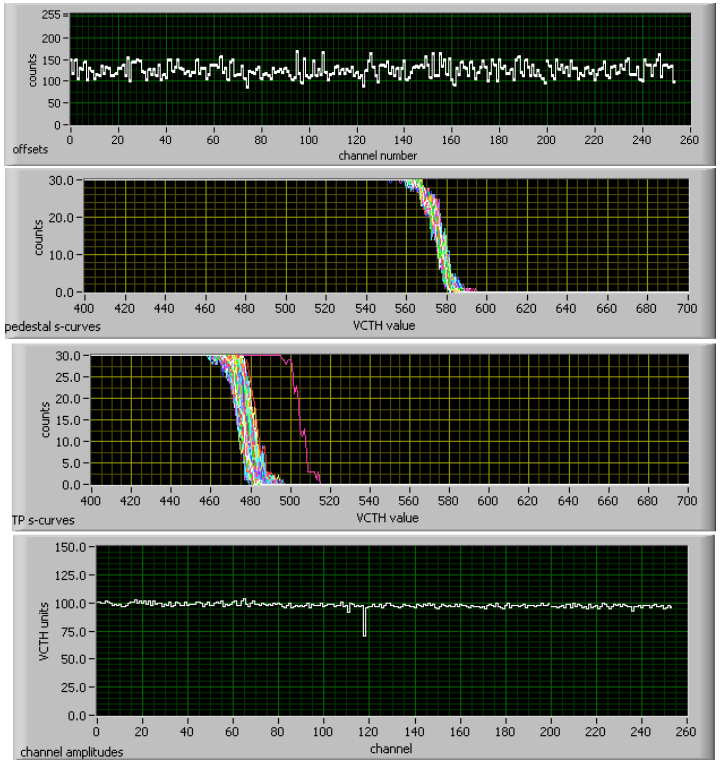
this chip shows an obvious trend across the chip in the gain picture, and also in the offsets after tuning

this problem more often observed on chips at the edge of the wafer

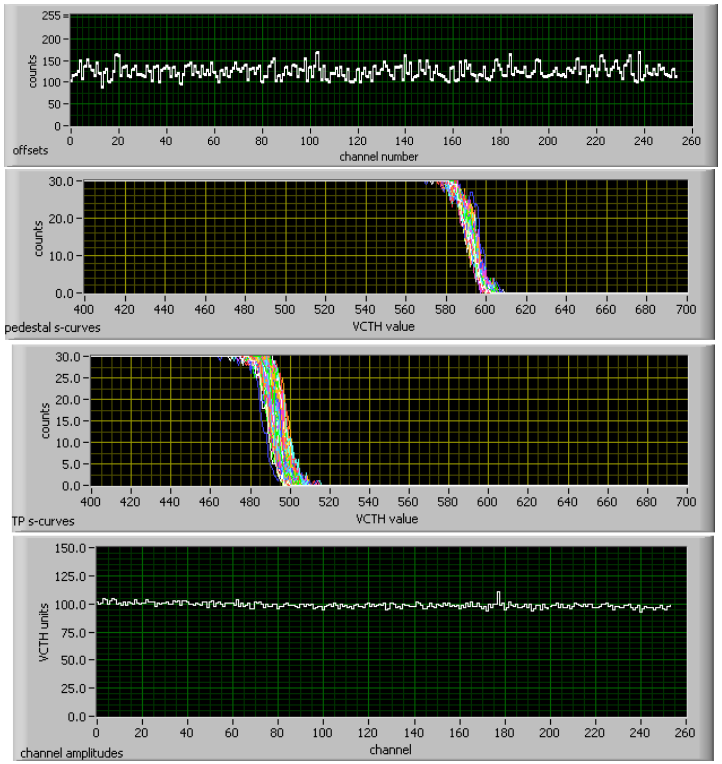
this chip shows a problem on several channels

problem typical of chip in centre of wafer

more types of channel failure



single channel with low gain



single channel with slightly high gain
but still a failure

post test data analysis

this first batch of wafer testing was a bit rushed - to get wafers quickly to bumping company

- aggravated by problem with usual probing machine

but test protocol was quite thorough, and all chips passed should work well

post test data analysis limited to visual scan through data - chip by chip

more automated post test data analysis can be developed

will be interesting to look for correlations between any bad behaviour observed on hybrids and probe test data

- chip ID enables this & also allows us to be certain what chip ends up where

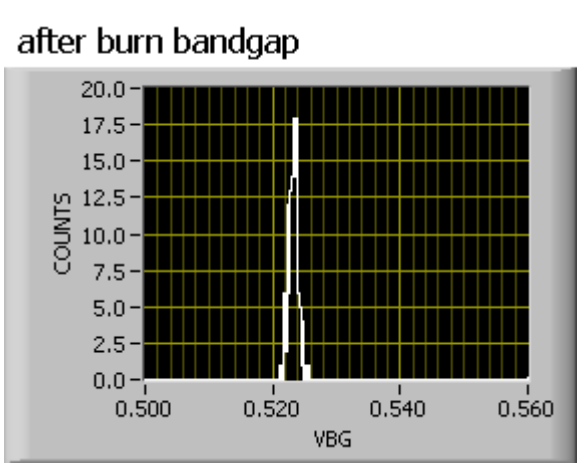
data examples

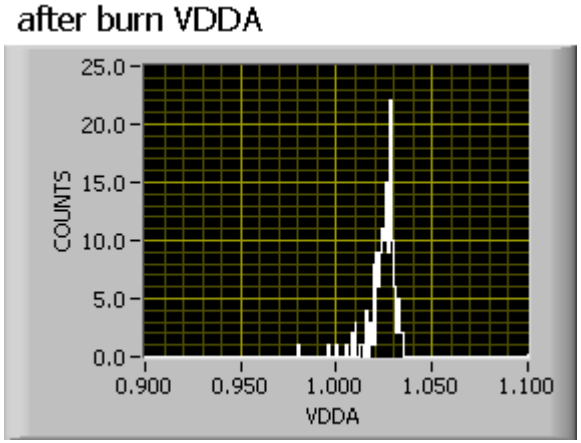
cumulative plots of data for one of the wafers illustrates across wafer spread

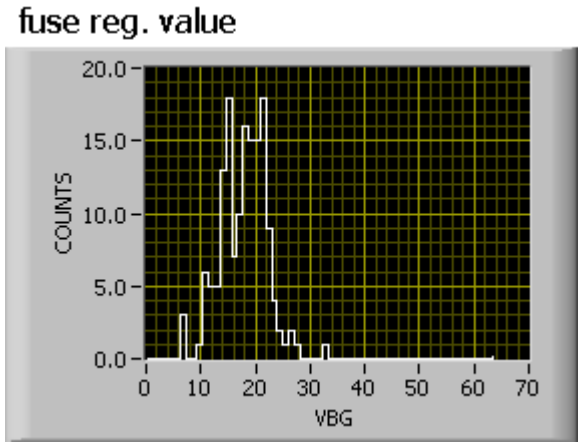
all these chips were passed

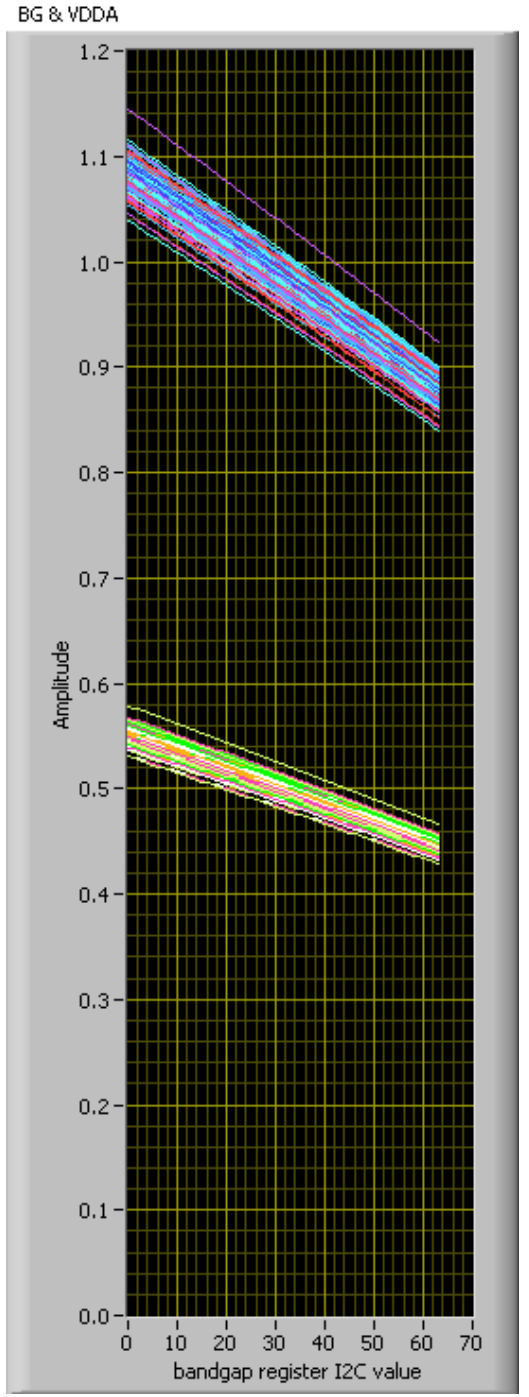
after fusing bandgap values distribution narrow

larger spread in VDDA values - suspect due to variable probe contact









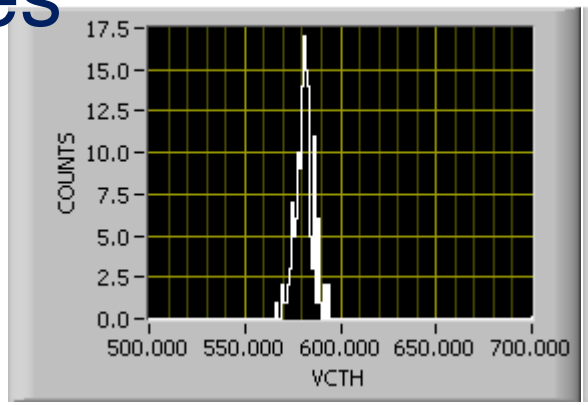
other data examples

all these chips were passed - no obvious performance issues

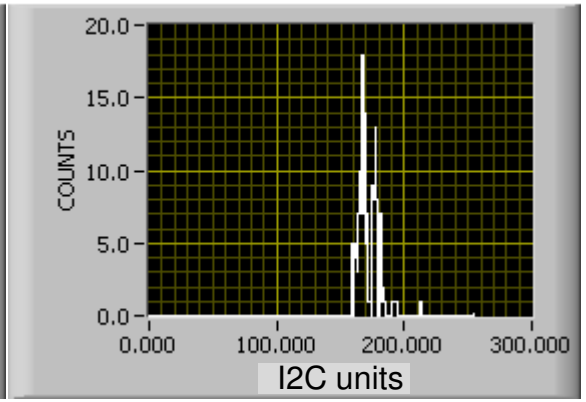
few chips with low VDDD current values - suspect measurement issue

maybe power supply current not given enough time to settle - needs further investigation

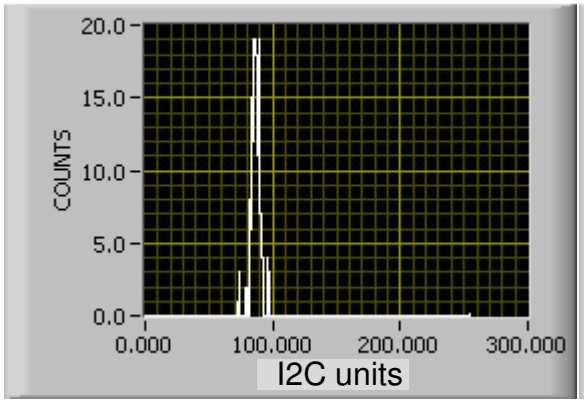
AVERAGE 50% POINT



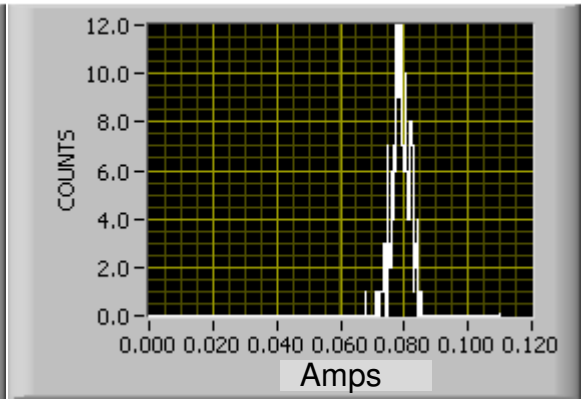
MAXIMUM OFFSET VALUE



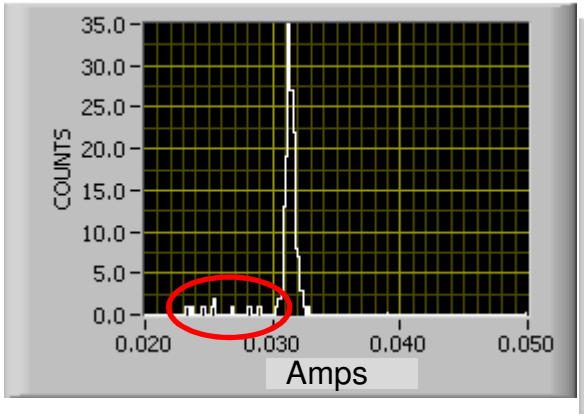
MINIMUM OFFSET VALUE



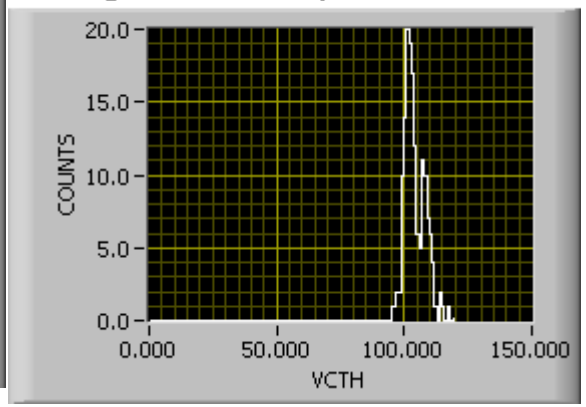
VLDOI current



VDDD current



average channel amplitude



summary

5 wafers probed and now with bumping company

ability to probe wafers at full speed now confirmed

yield quite high (> 80%) but noticeable pattern of failures in centre of wafers

will further refine probing tests and post test data analysis using remaining 3 wafers