CBC3 SEU BEAMTEST RESULTS

JOHAN BORG, MARK RAYMOND, KIRIKA UCHIDA

CBC 3 DESIGN FOR SEU TOLERANCE

- bit flips which do not go back to the correct values until reset or reloaded,
  - I2C registers - ***Whitaker latches***
  - Pipeline logic (read/write counters) controls - ***Whitaker Flip-Flops***
- Register bit flips in data (just like noise, other data are not affected)
  - 512 deep pipeline (12.8 us) – ***SRAM***
  - 32 deep buffer – ***SRAM***

Most SEU tolerant designs in CBC3 are the same as CBC2 except for the I2C registers where triple redundant logic was used in CBC2.

SEU test for CBC2 showed the vulnerability of the I2C registers but showed a good tolerance for pipeline logic and pipeline & buffer .

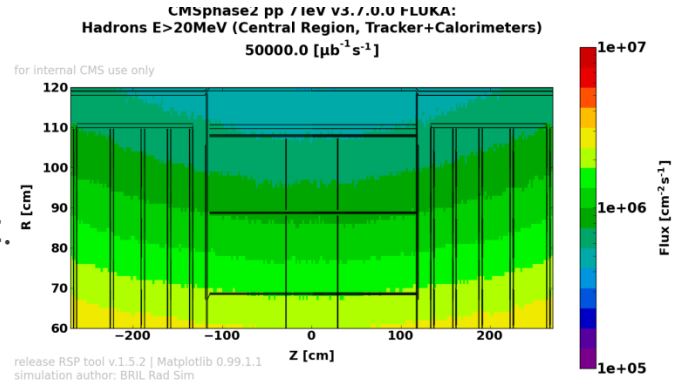
SEU TEST IN A PROTON BEAM

- HL-LHC
  - The large amount of light hadrons interact with materials by nuclear interaction. The recoil silicon nuclei inside or near the sensitive volumes can deposit enough charge to cause SEU events.
  - $3x10^{6}cm^{-2}s^{-1}$ is used to estimate the SEU rate at HL-LHC. (3 x the flux in the middle region by FLUKA simulation)
- LiF at Louvain
  - Proton beam from cyclotron with max. energy at 62 MeV and flux ~$2.3x10^{8}cm^{-2}s^{-1}$.

    Flux : ~75 times the HL-LHC.

    The SEU cross section at 62MeV corresponds to average cross section in the tracker at the HL-LHC.
  - 14.6 hours of beam.

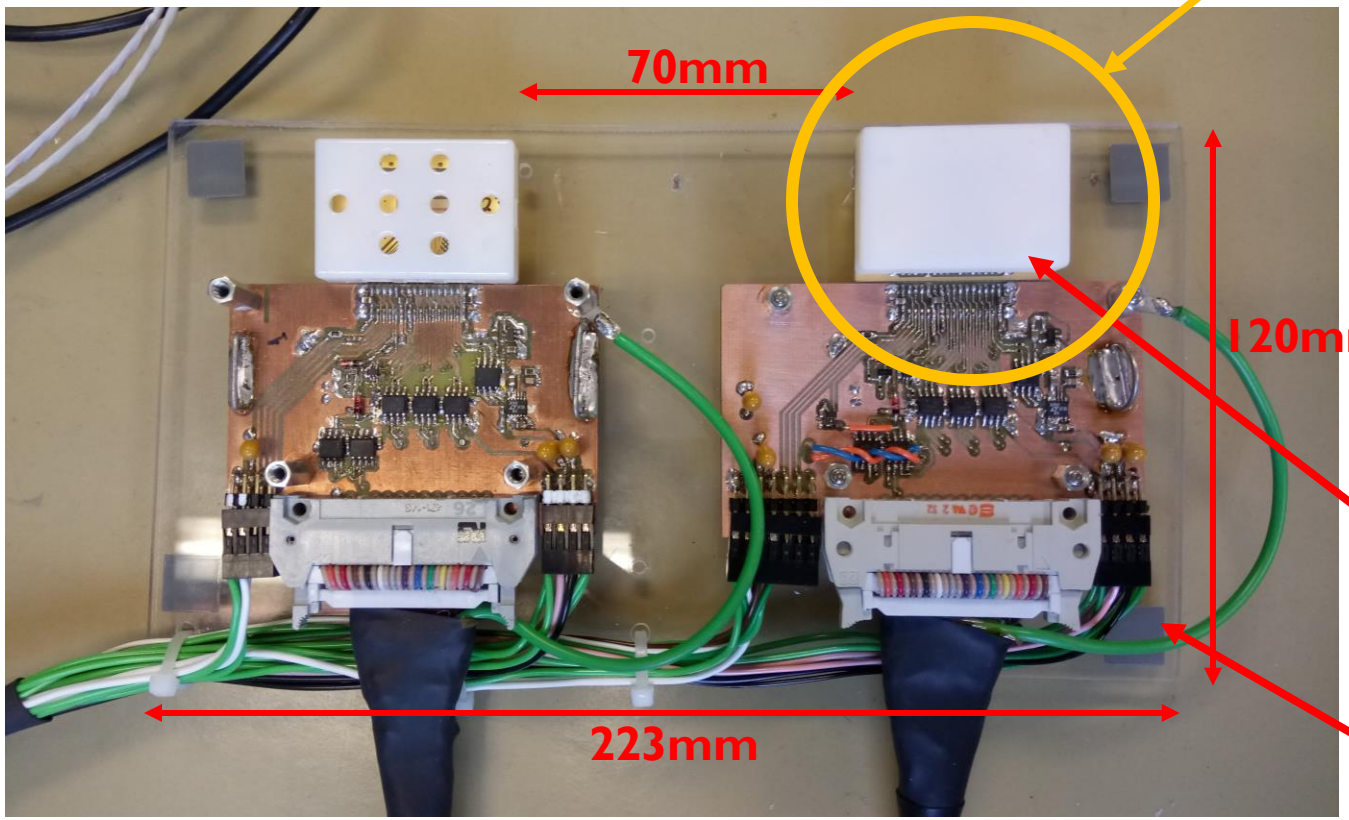
    Corresponds to 1000 hours (46.8 days) at the HL-LHC.

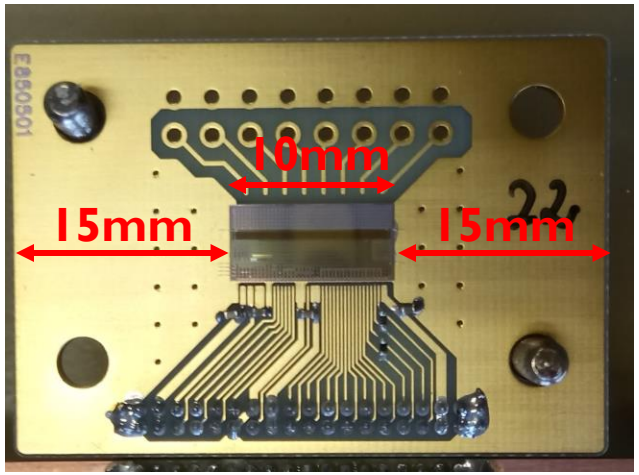


Main purpose is to check SEU tolerance of I2C. Expecting no SEU during 16 hours.

FRONTEND SETUP

- 2 CBCs, 1 in beam and one outside the beam.

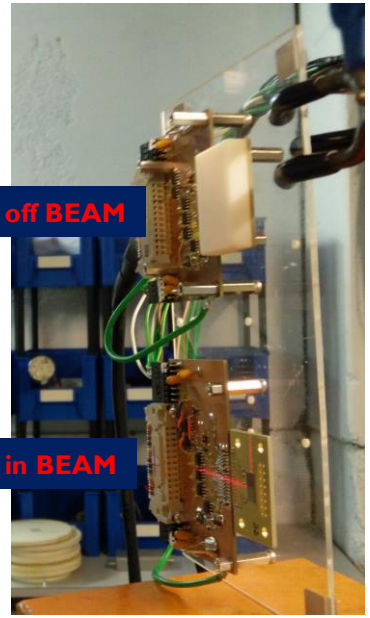


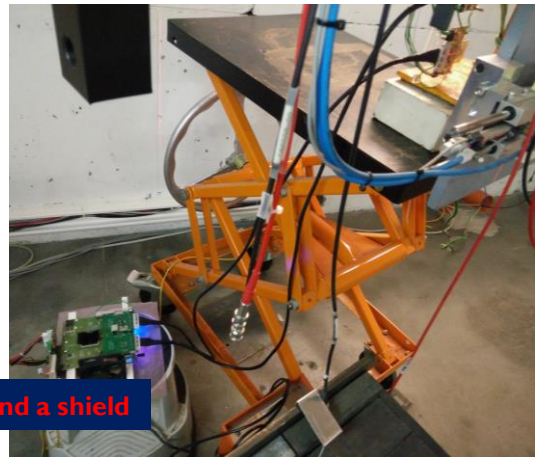


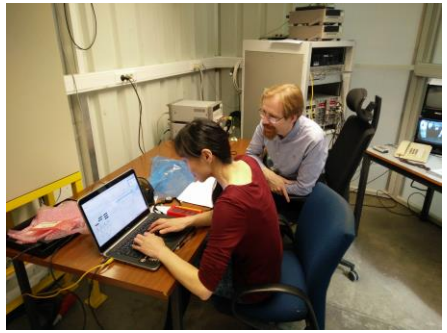
These white plastic covers will be taken away during the test

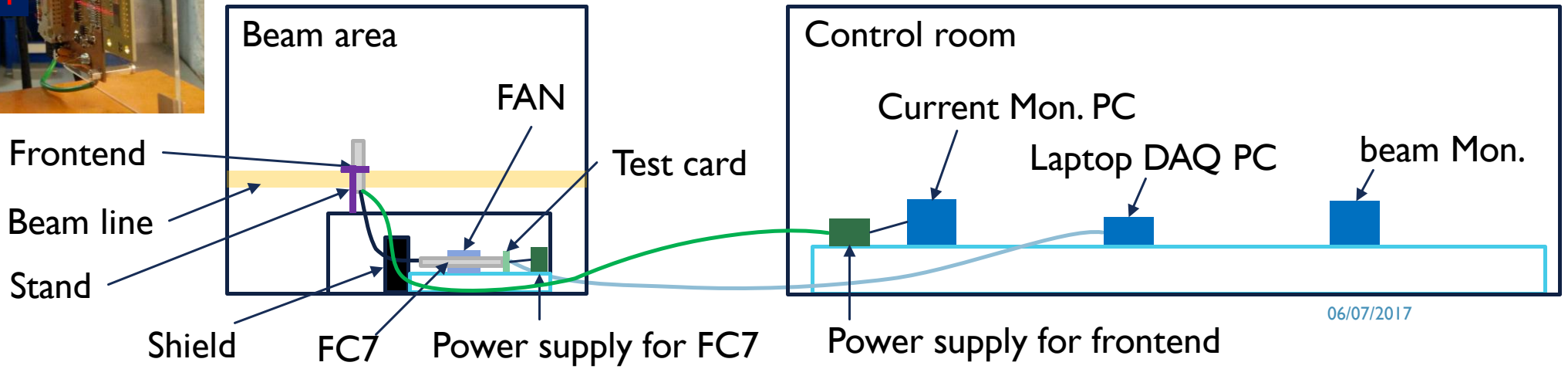
3mm thick acrylic plate : 223mm x 120mm

SETUP


CBC off BEAM
CBC in BEAM


FC7 behind a shield




Beam area
FAN
Frontend
Test card
Beam line
Stand
Shield
FC7
Power supply for FC7
Control room
Current Mon. PC
Laptop DAQ PC
beam Mon.
Power supply for frontend

CBC I2C SETTINGS AND OBSERVED BIT FLIPS IN THE BEAMTEST

Register settings

- page 1 registers (control registers & channel masks) are set to reasonable values for normal operation.
- Page 2 registers (254 channel offsets) are set to 0xff, 0x00, 0x0f, and 0x80/0x7f in settings A, B, C, and D respectively. (To see if any differences in the rate of 0 to 1 and 1 to 0 bit flips)

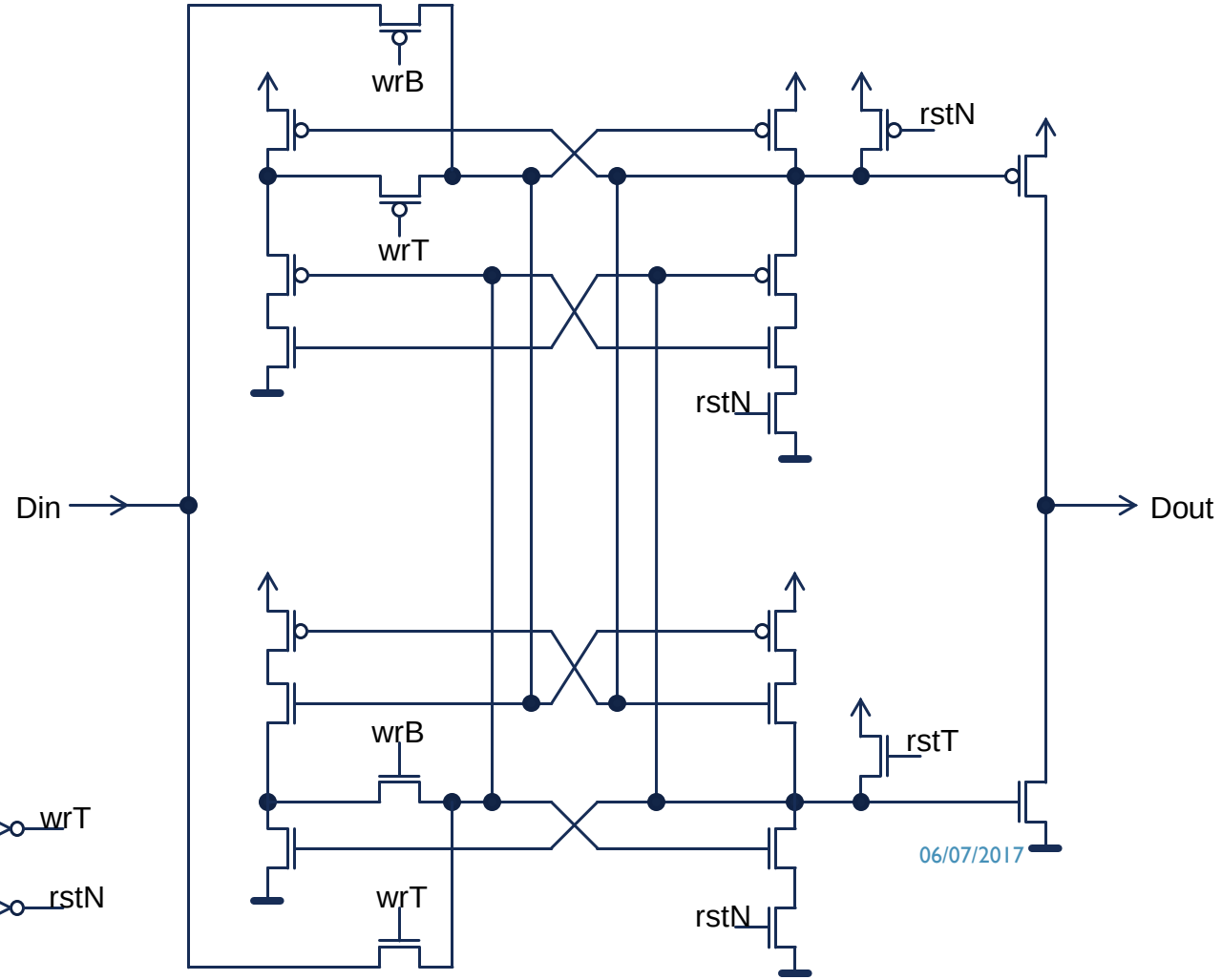
	Setting A (ofst:0xff)	Setting B (ofst:0x00)	Setting C (ofst:0x0f)	Setting D (ofst:0x80/0x7f)
Time (read every 5 mins)	16701 sec (04:38:21)	5815 sec (01:36:55)	10070 sec (02:47:50)	8981 sec (02:29:41) (4 flips)
Time (read every 5 secs)				1525 sec (00:25:25) (1 flip) *

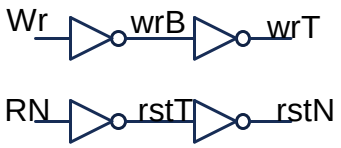
Result

- 25 bit flips in total in the CBC in the beam, while no bit flips in the CBC not in the beam.
  Bit flips are observed!

POSSIBLE NODES TO BE FLIPPED

- Write (Wr)
  - Causes the storage cell to flip to the last write transaction data left in the bus
- Reset (RN)
  - Causes the storage cell to flip to the default.





Bit flip details

Setting type	Page	Address	Set value	Value after bit-flip	Flipped bit	Default value	Type	Flip direction	Flipped to default	Flipped to the last write	Last write value	Last transaction
A	2	0x17	0xFF	0xFB	2	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x2D	0xFF	0xDF	5	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xC4	0xFF	0xFD	1	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x5D	0xFF	0xFD	1	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xD3	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x4F	0xFF	0xBF	6	0x80	Offset	1->0	Yes	No	0x41	Status reg. read
A	2	0x97	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x01	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0x08	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xAB	0xFF	0xDF	5	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	1	0x29	0xFF	0xFD	1	0xFF	Mask channel	1->0	No	Yes	0x41	Status reg. read
A	2	0x6D	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xA6	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
A	2	0xAB	0xFF	0xF7	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
B	1	0x1B	0x04	0x00	2	0x00	Layer swap & CW	1->0	Yes	Yes	0x41	Status reg. read
B	2	0x37	0x00	0x80	7	0x80	Offset	0->1	Yes	No	0x41	Status reg. read
C	2	0xC8	0x0F	0x0E	0	0x80	Offset	1->0	Yes	No	0x41	Status reg. read
C	2	0xEF	0x0F	0x0B	2	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
C	2	0xDC	0x0F	0x0D	1	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
C	2	0xFA	0x0F	0x07	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
D	2	0x99	0x7F	0x77	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
D	2	0xDA	0x7F	0x3F	6	0x80	Offset	1->0	Yes	No	0x41	Status reg. read
D	2	0xE6	0x7F	0x77	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
D	2	0xA0	0x7F	0x77	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
D	2	0xA4	0x7F	0x77	3	0x80	Offset	1->0	Yes	Yes	0x41	Status reg. read
Total									24	21		

The last written value is 0x41 to the front end control register to read the status register (this was checked periodically in the test).

SEU RATE AT HL-LHC

- 25 bit flips in the beam (total fluence during the register check =9.8 x 10^{12} cm^{-2})
- Rate estimation at HL-LHC (flux = 3 x 10^{6} $cm^{-2}s^{-1}$)
  - Overall flip rate : ~ 0.7 /chip/day and ~ 3 x 10^{-4} /bit/day
    70% of the chips can have a single upset bit in a day unless they are reconfigured.
  - *However, there are control, mask, offsets and unused registers which should be treated separately for the bit flip impacts on the data taking.*

Func.	data and stub ctr.	Data only ctrl.	Stub only ctrl.	Channel mask	Channel offsets	Not used in normal data taking	Total
# of bits	123	2	146	254	254 * 8	83	2632
Fraction [%]	4.66	0.08	5.53	9.62	76.97	3.14	100.00
Flip rate / day	0.032 ± 0.006	0.0005 ± 0.0001	0.038 ± 0.008	0.07 ± 0.01	0.5 ± 0.1	0.022 ± 0.004	0.7 ± 0.1

  - 3 % / day of chips will have bit flips which affect readout data in the chips (data and stub ctr. & data only ctrl. registers)
  - 7 % / day of chips will have bit flips which affect stub data in the chips (data and stub ctr. & stub only ctrl. registers)
  - 0.2 % /day of channels will have channel mask or offset register value changed

COMPARISON OF I2C BIT FLIPS IN CBC2 AND CBC3

I2C registers in CBC2 are triplicated with refresh signal to set triplicated cells to the majority.

For a simple comparison excluding complication caused by the refresh signal & the time dependent bit flip rate in CBC2, the # of bit flips in 10 mins without refresh signal observed in CBC2 is compared with the corresponding number obtained from the beamtest for CBC3.

CBC version	# of bit flip in 10 mins per chip	# of bits per chip	Average flux [$cm^{-2}s^{-1}$]
2	2.8 ± 0.5	2456	2.5E+08
3	0.36 ± 0.07	2640	2.2E+08

Compared to CBC2, the SEU tolerance has improved.

SOLUTIONS TO THE SEU RATE @ HL-LHC IN I2C REGISTERS

- No design change

  Reconfiguration of I2C registers regularly during a run. I2C register reconfiguration could be done without disturbing the data taking.
  It takes 158 ms to reconfigure all registers in a module (330 registers / chip x 16 chips x 30us = 158ms)

  - All modules could be reconfigured in ~158 ms, if all done at the same time.
    Once per hour with pausing the run is even realistic.
  - All modules could be reconfigured in 20 mins, if do one at a time (7500 modules).
    Without pausing the run. Even if the reconfiguration disturbs the data taking, ~0.013 % of data are affected.
- Minor modifications under study if reloading the registers is not an option
  - RAL has identified some nodes that are vulnerable to SEU.

ERRORS ON DATA FOR 10.7 HOURS (1.4 FOR PIPELINE LOGIC TEST)

Data taken with 1 kHz trigger to check pipeline logic, synchronization of the two chips, chip error, stub & hit information.

- Errors on CBC in beam
  - 1 hit (0 expected) at 17:03 (15/05)
  - 1 hit (0 expected) at 18:01 (15/05)
  - Stubs are found (0 expected) at 23:00 (15/05) until the end of the run at 23:25 (15/05)
    (*bit flip on the cluster width setting on i2c register happened during 22:58 to 23:03 (15/05)*)
  - Error on slvs5 at 09:38 (16/05)
- Errors on CBC out of beam
  - Error on slvs5 at 08:56 (16/05) L1A counter did not match with the other CBC after this.
  - 6 hits were found (0 expected) at 12:11 (16/05)
  - sync lost bit was set in i2c register at 15:52 (16/05). Fixed by a fast reset at 15:56 (16/05)

All the observed errors on CBC in beam were also seen on CBC off beam except for the stub error due to I2C register bit flip.

Pipeline logic error upper limit at HL-LHC : 5.9×10^{-6} sec^{-1}/chip

SUMMARY

- The results show good SEU tolerance of CBC3 except for I2C registers.
- The SEU tolerance in I2C registers improved from CBC2, but may not be safe for 24 hours.
  (The estimation is done with the flux in the centre of the 2S detector from FLUKA simulation x 3)
  - Reconfiguration during the run or minor modifications in the chip design need to be considered.

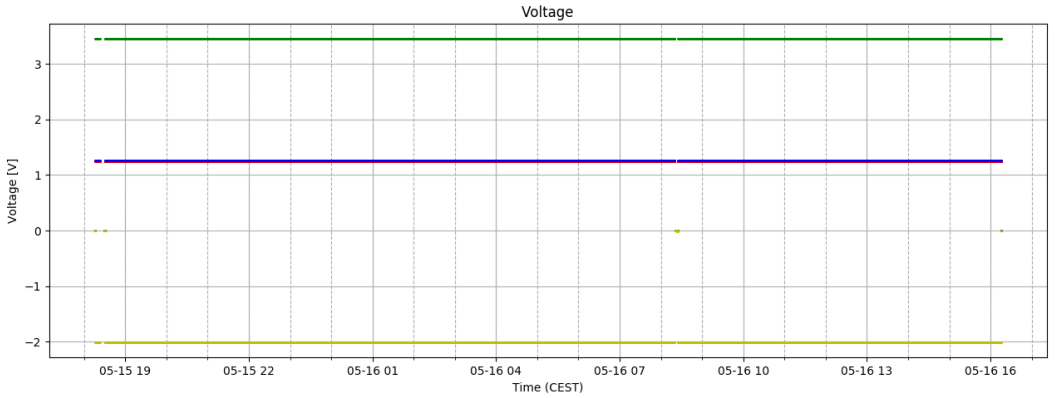
BACKUPS

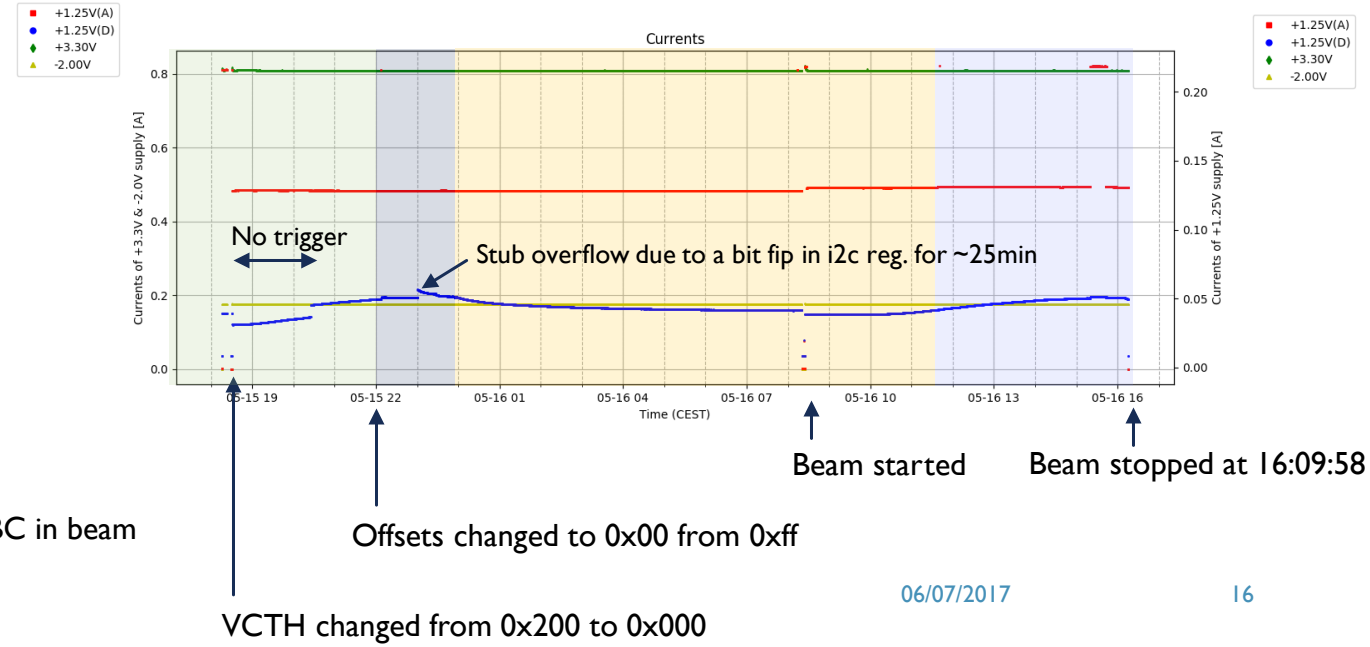
BACKEND SETUP

- The equipment provided by Louvain
  - Power supplies for frontend electronics 2.2V(~174mA), 3.3V(~800mA), 1.25(34mA), 1.25(~130mA)
    - E3631A (3 outputs) & E3633A (1 output)
  - Power supply for backend electronics. ATX 24-pin P1 motherboard connector.
  - A stand to support frontend board.
- The equipment we brought
  - Frontend and the 1m cable to FC7.
  - FC7 with the test card with fan connected.
  - A Laptop PC.
  - Ethernet cable to connect the FC7 test card and the PC.
  - 4 cable set (5m) to connect the frontend and power supplies.

BEAM PARAMETERS, STATISTICS, VOLTAGE & CURRENT READINGS, AND CBC3 SETTINGS

Start time	Irradiation time [sec]	Energy [MeV]	Fluence [cm^{-2}]	TID [rad]	Mean flux [$cm^{-2}s^{-1}$]	CBC ID in beam
15.05.17 16:52:52	25130	62	5.79E+12	7.77E+05	2.30E+08	22
16.05.17 08:35:08	27290	62	6.11E+12	8.21E+05	2.24E+08	23





+1.25V(D) : power supply to digital circuit of CBC in beam
+1.25V(A) : power supply to analogue circuit of 2 CBCs and digital circuit of CBC in beam
+3.3V, -2.00V : power supply to support boards.

CBC I2C SETTINGS AND OBSERVED BIT FLIPS IN THE BEAMTEST

(14 REGISTERS WERE FORGOTTEN TO BE CHECKED, SO THOSE ARE EXCLUDED IN THIS SLIDE)

Registers in page 1 is set to reasonable values for the normal operation. Registers in Page 2 are set to different values in the setting A, B, and C.
Experiment started with Setting A,. Setting B from 22:00 (15/05), Setting C from 23:56 (15/05), Setting D from 11:38 (16/05)
VCTH value changed from 512(default) to 0 at 18:30 (15/05)

	Default
# of 0	1957 (1778 in page 2)
# of 1	571 (254 in page 2)

	Setting A (ofst:0xff)			Setting B (ofst:0x00)			Setting C (ofst:0x0f)			Setting D (ofst:0x80/0x7f)			
Time (read every 5 mins)	16701 sec (04:38:21)			5815 sec (01:36:55)			10070 sec (02:47:50)			8981 sec (02:29:41) (4 flips)			
Time (read every 5 secs)										1525 sec (00:25:25) (1 flip) *			
Set logic type	# of bits	# of flips	Flip rate	# of bits	# of flips	Flip rate	# of bits	# of flips	Flip rate	# of bits	# of flips	Flip rate	Flip rate *
0	172	0	< 8.0	2194	1	0.8 +/- 0.8	1188	0	< 1.9	1188	0	< 2.2	< 12.7
1	2356	14	3.6 +/- 1.0	334	1	5.1 +/- 5.1	1340	4	3.0 +/- 1.5	1340	5	3.3 +/- 1.7	4.9 +/- 4.9
0 the same as default	150	0	< 9.2	1919	0	< 2.1	912	0	< 2.5	1039	0	< 2.5	< 15
1 the same as default	549	1	1.1 +/- 1.1	296	0	< 13	295	0	< 68	422	0	< 6.1	< 36
0 different from default	22	0	< 63	275	1	6.3 +/- 6.3	276	0	< 8.3	149	0	< 17	< 101
1 different from default	1807	13	4.3 +/- 1.2	38	1	45 +/- 45	1045	4	3.8 +/- 1.9	918	5	4.9 +/- 2.4	7.1 +/- 7.1

It looked like that there was a tendency to go back to the default values, but it is actually statistically not very significant. There were just many registers with logic 1 different from the default value 0.

Flip rate : # flips / Time / # of bits [x10^{-7}/sec/bit]

There are 25 bit flips at CBC in the beam. (CBC chips are swapped in the last half beam). No bit flip is observed at CBCs off the beam except for one sync lost status bit.

CBC I2C SETTINGS AND OBSERVED BIT FLIPS IN THE BEAMTEST

Set logic type	# of bits x time	# of flips	Flip rate / bit
0	40306770	1	0.2 ± 0.2
1	68402581	24	3.5 ± 0.7
0 the same as default	32822784	0	< 0.7
1 the same as default	17877946	1	0.6 ± 0.6
0 different from default	7483986	1	1.3 ± 1.3
1 different from default	49167385	23	4.7 ± 1.0

It looked like that there was a tendency to go back to the default values, but it is actually statistically not very significant. There were just many registers with logic 1 different from the default value 0.

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There are 25 bit flips at CBC in the beam. (CBC chips are swapped in the last half beam). No bit flip is observed at CBCs off the beam except for one sync lost status bit.